Semiconductors for Television and Video Systems

SAA7199B to TDA4680

DATA HANDBOOK

BOOK IC02b 1992

Philips Semiconductors

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Semiconductors for Television and Video Systems

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TDA2543	AM sound IF circuit for French standard
TDA2556	quasi-split-sound circuit with dual FM sound demodulators
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TDA2795	TV stereo/dual sound identification decoder
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TDA4660P	64 µs baseband delay line
TDA4660T	64 µs baseband delay line
TDA8370	synchronization processor for TV receivers
TDA8420	hi-fi stereo audio processor; I²C-bus
TDA9045	video processor and input selector
TDA9080	video control combination circuit with automatic cut-off control
TEA2000	PAL/NTSC colour encoder

DEVICE DATA

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1992

SAA7199B

Digital video encoder, GENLOCK-capable

FEATURES

- Monolithic integrated CMOS video encoder circuit
- Standard MPU (12 lines) and I²C-bus interfaces for controls
- Three 8-bit signal inputs PD(7-0) for RGB respectively YUV or indexed colour signals (Tables 10 to 17)
- Square pixel and CCIR input data rates
- Band-limited composite sync pulses
- Three 256X8 colour look-up tables (CLUTs) e. g. for gamma-correction
- External subcarrier from a digital decoder (SAA7151B or SAA7191B)
- Multi-purpose key for real-time format switching
- Autonomous internal blanking
- Optional GENLOCK operation with adjustable horizontal sync timing and adjustable subcarrier phase
- Stable GENLOCK operation in VCR standard playback mode
- Optional still video capture extension
- Three suitable video 9-bit digital-to-analog converters
- Composite analog output signals CVBS, Y and C for PAL/NTSC

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pins 2, 21 and 41)	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage range (pins 64, 66, 70 and 72)	4.75	5.0	5.25	V
I_P	total supply current	-	-	200	mA
V_I	input signal levels	TTL-compatible			
V_o	analog output signals Y, C and CVBS without load (peak-to-peak value)	-	2	-	V
R_L	output load resistance	90	-	-	Ω
ILE	LF integral linearity error in output signal (9-bit DAC)	-	-	±1	LSB
DLE	LF differential linearity error in output signal (9-bit DAC)	-	-	±0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA7199B encodes digital base-band colour/video data into analog Y, C and CVBS signals (S-Video included). Pixel clock and data are line-locked to the horizontal scanning frequency of the video signal. The circuit can be used in a square pixel or in a consumer TV application. Flexibility is provided by programming facilities via MPU-bus (parallel) or I²C-bus (serial).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7199B	84	PLCC	plastic	SOT189CG

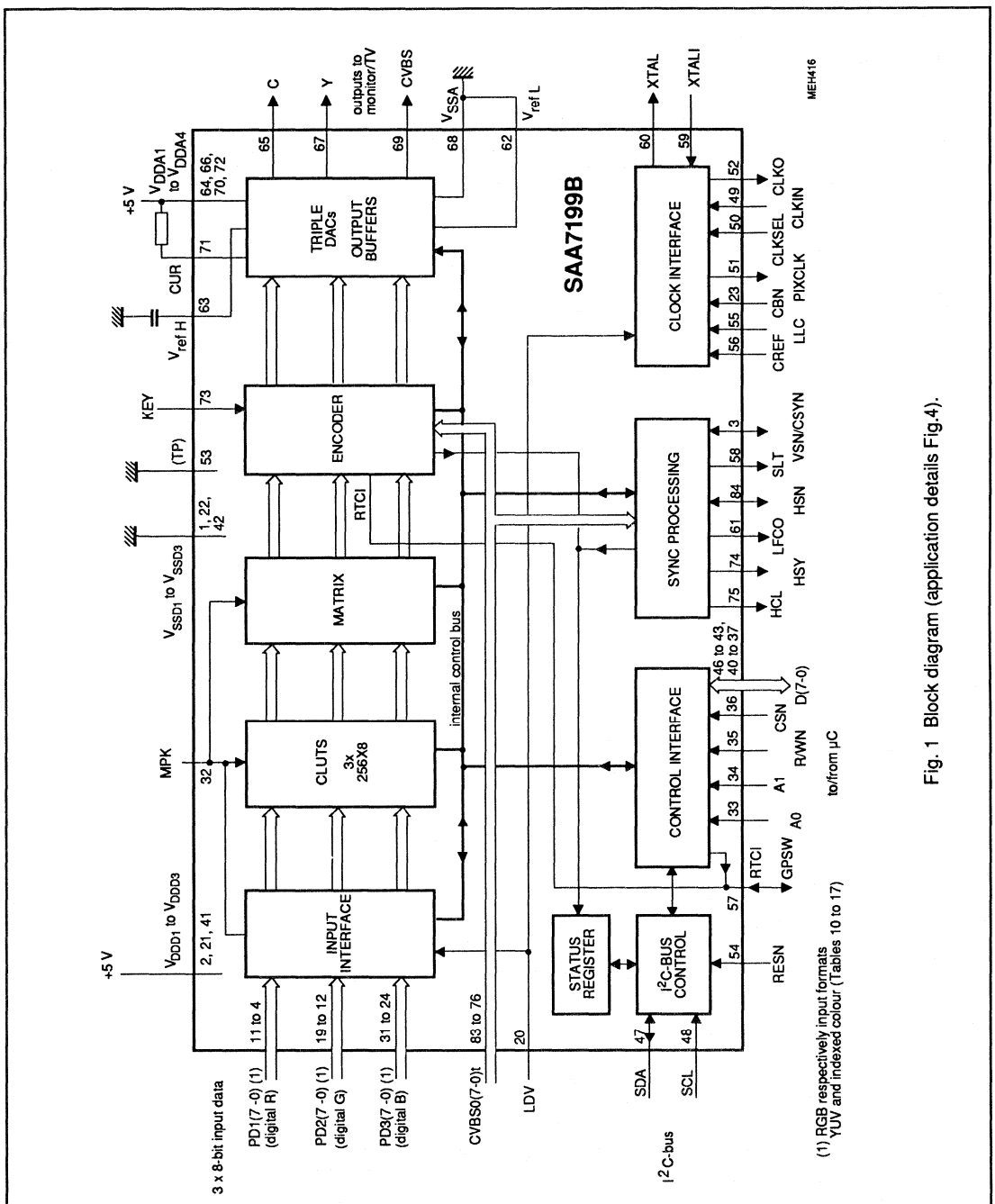


Fig. 1 Block diagram (application details Fig.4).

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD1}	1	digital ground 1 (0 V)
V_{DDD1}	2	+5 V digital supply 1
VSN	3	vertical sync output (3-state), conditionally composite sync output; active LOW or active HIGH
PD1(0)	4	data 1 input: digital signal R (red) respectively V signal (formats in Table 6)
PD1(1)	5	
PD1(2)	6	
PD1(3)	7	
PD1(4)	8	
PD1(5)	9	
PD1(6)	10	
PD1(7)	11	
PD2(0)	12	data 2 input: digital signal G (green) respectively Y signal or indexed colour data (formats in Table 6)
PD2(1)	13	
PD2(2)	14	
PD2(3)	15	
PD2(4)	16	
PD2(5)	17	
PD2(6)	18	
PD2(7)	19	
LDV	20	load data clock input signal to input interface (samples PDn(7-0), CBN, MPK, KEY and RTCI)
V_{DDD2}	21	+5 digital supply 2
V_{SSD2}	22	digital ground 2 (0 V)
CBN	23	composite blanking input; active LOW
PD3(0)	24	data 3 input: digital signal B (blue) respectively U signal (formats in Table 6)
PD3(1)	25	
PD3(2)	26	
PD3(3)	27	
PD3(4)	28	
PD3(5)	29	
PD3(6)	30	
PD3(7)	31	
MPK	32	multi-purpose key; active HIGH
A0	33	subaddress bit A0 for microcomputer access (Table 3)
A1	34	subaddress bit A1 for microcomputer access (Table 3)

SYMBOL	PIN	DESCRIPTION
R/WN	35	read/ write not input signal from microcontroller
CSN	36	chip select input for parallel interface; active LOW
D0	37	bidirectional port from/to microcontroller (bits D3 to D0)
D1	38	
D2	39	
D3	40	
V_{DDD3}	41	+5 V digital supply 3
V_{SSD3}	42	digital ground 3
D4	43	bidirectional port from/to microcontroller (bits D7 to D4)
D5	44	
D6	45	
D7	46	
SDA	47	I^2C-bus data line
SCL	48	I^2C-bus clock line
CLKIN	49	external clock signal input (maximum 60 MHz)
CLKSEL	50	clock source select input
PIXCLK	51	CLKO/2 or conditionally CLKO output signal
CLKO	52	selected clock output signal (LLC or CLKIN)
TP	53	connect to ground (test pin)
RESN	54	reset input; active LOW
LLC	55	line-locked clock input signal from external CGC
CREF	56	clock qualifier of external CGC
GPSW / RTCI	57	general purpose switch output (set via I^2C-bus or MPU-bus); real-time control input, defined by I^2C or MPU programming
SLT	58	GENLOCK flag (3-state): HIGH = sync lost in GENLOCK mode; LOW = otherwise
XTALI	59	crystal oscillator input (26.8 or 24.576 MHz)
XTAL	60	crystal oscillator output
LFCO	61	line frequency control output signal for external CGC
$V_{ref\,L}$	62	reference LOW voltage of DACs (resistor chains)
$V_{ref\,H}$	63	reference HIGH voltage of DACs (resistor chains)
V_{DDA4}	64	+5 V analog supply 4 for resistor chains of the DACs
C	65	chrominance analog output signal C
V_{DDA1}	66	+5 V analog supply 1 for output buffer amplifier of DAC1
Y	67	luminance analog output signal Y
V_{SSA}	68	analog ground (0 V)

SYMBOL	PIN	DESCRIPTION
CVBS	69	CVBS analog output signal
V_{DDA2}	70	+5 V analog supply 2 for output buffer amplifier of DAC2
CUR	71	current input for analog output buffers
V_{DDA3}	72	+5 V analog supply 3 for output buffer amplifier of DAC3
KEY	73	key signal to insert CVBS input signal into encoded CVBS output signal; active HIGH
HSY	74	horizontal sync indicator output signal; active HIGH (3-state output to ADC)
HCL	75	horizontal clamping output; active HIGH (3-state output)
CVBS0	76	digital CVBS input signal
CVBS1	77	
CVBS2	78	
CVBS3	79	
CVBS4	80	
CVBS5	81	
CVBS6	82	
CVBS7	83	
HSN	84	horizontal sync output; active LOW or active HIGH for 64 x PIXCLK (3-state output)

FUNCTIONAL DESCRIPTION

The SAA7199B is a digital video encoder that translates digital RGB, YUV or 8-bit indexed colour signals into the analog PAL/NTSC output signals Y (luminance), C (4.43/3.58 MHz chrominance) and CVBS (composite signal including sync).

Four different modes are selectable (Table 9):

- stand-alone mode (horizontal and vertical timings are generated)
- slaver mode (stand-alone unit that accepts external horizontal and vertical timing), and optional real-time information for subcarrier/clock from a digital colour decoder
- GENLOCK mode (GENLOCK capabilities are achieved in conjunction with determined ICs).
- test mode (only clock signal is required)

The input data rate (pixel sequence) has an integer relationship to the number of horizontal clock cycles (Table 1). A sufficient stable external clock signal ensures correct encoding. The generated clock frequency in the GENLOCK mode may deviate by ±7 % depending on the reference signal which is corresponding to its input sync signal. The clock will be nominal in the GENLOCK mode when the reference signal is absent (nominal with crystal oscillator accuracy for TV time constants, and nominal ±1.4 % for VCR time constants).

The on-chip colour conversion matrix provides CCIR 601 code-compatible transcoding of RGB to YUV data. RGB data out of bounds, with respect to CCIR 601 specification, can be clipped to prevent over-loading of the colour modulator. RGB data input can be either in linear colour space or in gamma-corrected colour space. YUV data must be gamma-corrected according to CCIR 601. This circuit operates primarily in a 24-bit colour space (3 x 8-bit) but can also accomodate different data formats (4:1:1, 4:2:2 and 4:4:4) as well as 8-bit indexed pseudo-colour space operations (FMT-bits in Table 6).

RGB CLUTs on chip provide gamma-correction and/or other CLUT functions. They consist of programmable tables to be loaded

Table 1 Pixel relationships

ACTIVE PIXELS PER LINE	FIELD RATE	MULTIPLES OF LINE FREQUENCY	PIXCLK OUTPUT SIGNAL (MHz)	XTAL (MHz)
640 (square)	60 Hz	780	12.272727	26.8
720	60 Hz	858	13.5	24.576
768 (square)	50 Hz	944	14.75	26.8
720	50 Hz	864	13.5	24.576

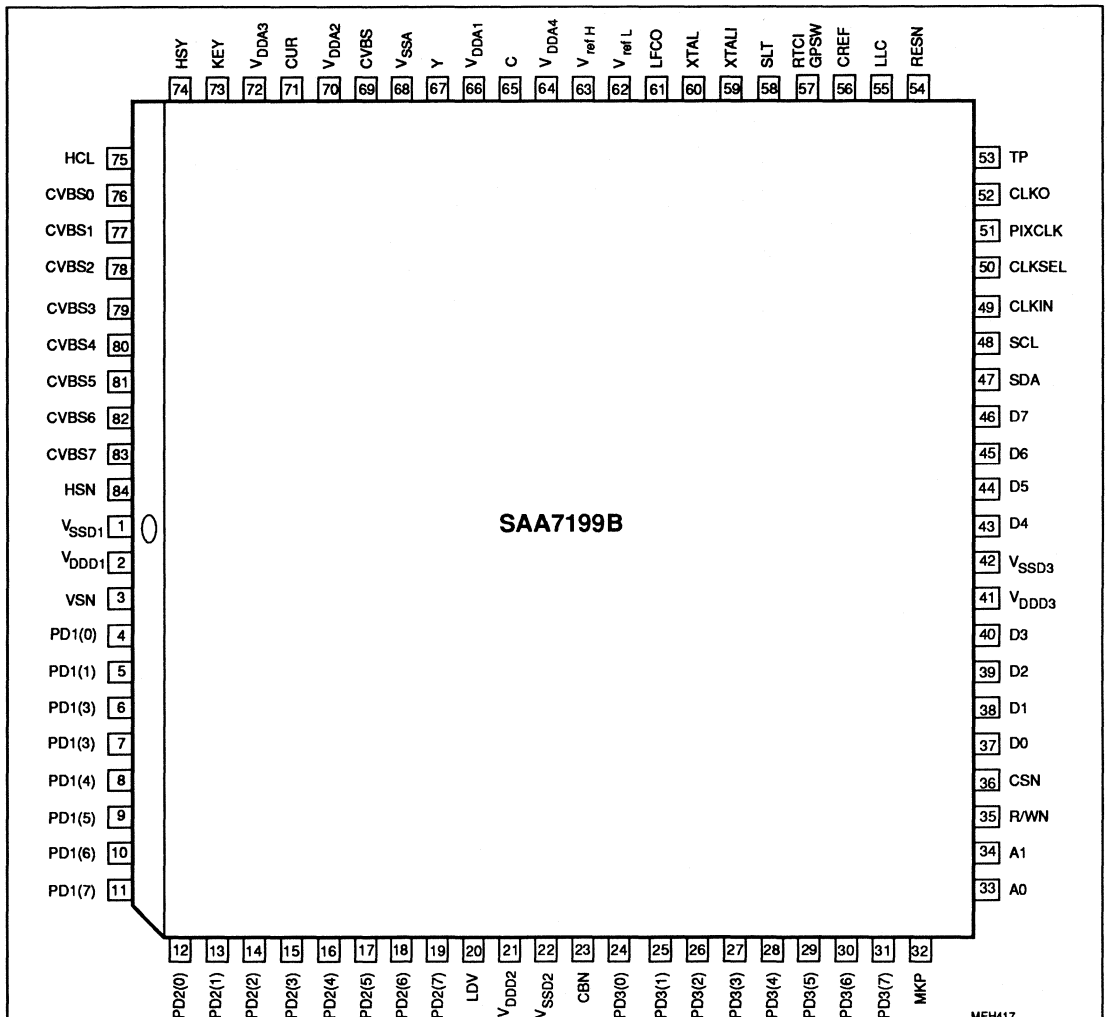


Fig.2 Pin configuration.

independently, and they generate 24-bit gamma-corrected output signals from 24-bit data of one of the input formats or from 8-bit indexed pseudo-colour data.

Required modulation is performed. The digital YUV data is encoded according to standards RS-170A (composite NTSC) and CCIR 624-4 (composite PAL-B/G). S-Video output signal is available (Y/C) as well as some sub-standard output signals (STD-bits in Table 6). A 7.5 IRE set-up level is automatically selected in the 60 Hz mode – there is none in 50 Hz mode.

The analog signal outputs can drive directly into terminated 75 Ω coaxial lines, a passive external filter is recommended (Figures 3 and 13). Analog post-filtering is required (LP in Fig.3).

GENLOCK to an external reference signal is achieved by addition of a video ADC and a clock generator combination. Thus, the system is enabled to lock on a stable video source or to a stable VCR source (normal playback). The SAA7199B, the ADC and the clock generator

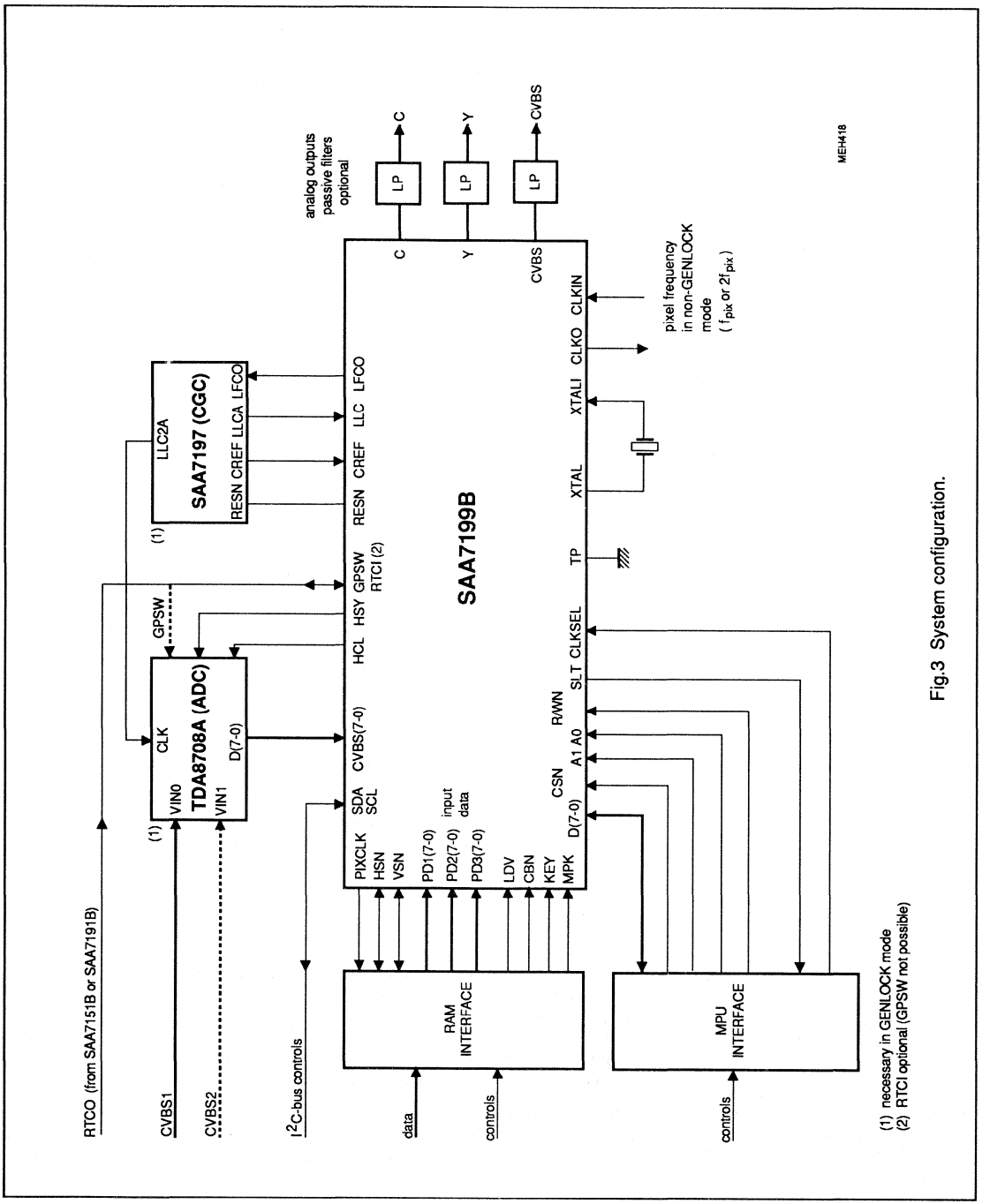


Fig.3 System configuration.

combination (Fig.3) form a control loop achieving a highly stable line-locked clock. The clock has to be generated by a crystal oscillator without this possibility.
The GENLOCK mode is not available in a single device set-up.

Control interface

The SAA7199B supports a standard parallel MPU interface as well as the serial I²C-bus interface. The MPU has a direct access to internal control registers and colour tables. Update is possible at any time, excluding coincident internal reading and external writing of the same cell (the current pixel value could be destroyed).
The two interfaces of Table 2 are selected automatically. However, the I²C control is inactive when the MPU interface is selected by CSN = LOW. No simultaneous access must occur. I²C-bus and MPU control complement each other and have access to common registers controlled via a common internal bus. The programmer can use virtually identical programs.
The internal memory space is devided into the look-up table and the control table, each with its own 8-bit address register is used as a pointer for specific location. This address register is provided with auto-incrementation and can be written by only one addressing.

The look-up table contains three banks of 256 bytes. Therefore, each read or write cycle must access to all three banks in a determined order. The support logic is part of the control interface.

Timing (Fig.3).

The reference to generate internal clocks from LLC in GENLOCK operation with SAA7197 is CREF (CREF = LLC/2). In this case input CLKSEL is HIGH and the SRC-bit is 1.

In non-GENLOCK operation the signal from CLKIN is used and LDV is clock reference (input CLKSEL = 0; SCR-bit = CPR-bit = 0).

Table 2 Access to the control interface

SYMBOL	DESCRIPTION
SDA (I²C-bus)	serial data line (bi-directional)
SCL	clock line
A1, A0 (MPU-bus)	address inputs
R/WN	read/write control
CSN	chip select; I²C-bus disabled (at LOW)
GPSW	general purpose switch output (bit of control register)
RESN	reset signal (active-LOW)

Table 3 Address assignment

ADDRESS INPUTS A1	A0	I²C-BUS SUBADDRESS	SELECTION
0	0	00	ADR-CLUT (address register of look-up tables)
0	1	01	DATA-CLUT
1	0	02	ADR-CTRL (index register of control table)
1	1	03	DATA-CTRL

Pins LLC and CLKIN are tied together when no switching between LLC and CLKIN is applied. In Fig.3 it is assumed that LLC and CLKIN are double the pixel clock frequency of CREF respectively LDV.
CREF must be at the same frequency (or constant HIGH or LOW) when LLC is at pixel clock frequency.
CPR-bit = 1 if CLKIN is at pixel clock frequency.
Buffered CLKO signal is always delayed. LLC or CLKIN signals are according to CLKSEL

Mapping

Mapping of external control signals onto internal bus. The method is simple. The MPU- bus contains the signals of Table 4 (names in chip-internal nomenclature).

Bit allocation

The Bit Allocation Map (BAM) shows the individual control signals, used to control the different operational modes of the circuit. The I²C-bus is normally used for control. The SAA7199B additionally has a MPU-bus interface for direct microprocessor connection.

The following BAM resembles the I²C-bus type but can be also used for the parallel bus. The control registers of Table 5 are indexed from 00 to 0F (hex). Auto-incrementation is applied.

Digital-to-analog converters

The converters use a combination of resistor chains with low-impedance output buffers. The bottom output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V. Fig.15 shows the application for 1.23 V/ 75 Ω outputs, using the serial 25 Ω + 22 Ω resistors.

Each digital-to-analog converter has its own supply pin for purpose of decoupling. V_{DDA4} is the supply voltage for the resistor chains of the three DACs. The accuracy of this supply voltage influences directly the output amplitudes.
The current CUR into pin 71 is 0.3 mA (V_{DDA4} = 5 V, $R_{64\text{-}71}$ = 20 kΩ); a larger current improves the bandwidth but increases the integral non-linearity.

Table 4 Signals on the internal bus

SYMBOL	DESCRIPTION	
R-WN	Select read/write (read = 1; write = 0)	
C-TN	Control table/look-up table (control table = 1; look-up table = 0)	
D-AN	Select data/address (data = 1; address = 0)	
DI/DO(0-7)	Data bus on port inputs/outputs D7 to D0	
EN	Enable from control interface to synchronize data transfer	
INTERNAL PARALLEL BUS	**PARALLEL INTERFACE**	**I²C-BUS INTERFACE**
R-WN	R/WN (pin 35)	LSB of slave address byte (read = HIGH; write = LOW)
C-TN	A1 (pin 34)	X) 4 subaddresses after decoding
A-TN	A0 (pin 33)	X)
DI/DO(0-7)	D7 to D0	Data bits D7 to D0 for each subaddress
EN	CSN and R/WN	Enable by every 9th clock of sample of SCL (control of serial-to-parallel conversion)

Table 5 Bit allocation map (I²C-bus access in Table 8)

INDEX BINARY	INDEX HEX	DATA BYTE D7	D6	D5	D4	D3	D2	D1	D0	DF**
Input processing										
0000 0000	00	VTBY	FMT2	FMT1	FMT0	SCBW	CCIR	MOD1	MOD0	5C
0000 0001	01	TRER7	TRER6	TRER5	TRER4	TRER3	TRER2	TRER1	TRER0	XX
0000 0010	02	TREG7	TREG6	TREG5	TREG4	TREG3	TREG2	TREG1	TREG0	XX
0000 0011	03	TREB7	TREB6	TREB5	TREB4	TREB3	TREB2	TREB1	TREB0	XX
Sync processing										
0000 0100	04	SYSEL1	SYSEL0	SCEN	VTRC	NINT	HPLL	HLCK*	OEF*	10
0000 0101	05	0	0	GDC5	GDC4	GDC3	GDC2	GDC1	GDC0	21
0000 0110	06	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0	52
0000 0111	07	0	0	PSO5	PSO4	PSO3	PSO2	PSO1	PSO0	32
Control, clock and output formatter										
0000 1000	08	DD	KEYE	SRC	CPR	COKI	IM	GPSW	SRSN	64
0000 1001	09	0	BAME	MPKC1	MPKC0	IEPI	RTSC	RTIN	RTCE	02
0000 1010+	0A+	0	0	0	0	0	0	0	0	00
0000 1011+	0B+	0	0	0	0	0	0	0	0	00
Encoder control										
0000 1100	0C	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0	XX++
0000 1101	0D	FSCO7	FSCO6	FSCO5	FSCO4	FSCO3	FSCO2	FSCO1	FSCO0	00
0000 1110	0E	0	0	0	CLCK*	STD3	STD2	STD1	STD0	0C
0000 1111+	0F+	0	0	0	0	0	0	0	0	

* read only bits + reserved ++ adjust as required.

** DF is the default value for a typical programming example: GENLOCK mode for a VCR; non-gamma-corrected RGB data (realtime keying is possible). SLT will be set if there is no horizontal lock. NTSC-M standard with normal colour bandwidth and 12.2727 MHz pixel rate. CSYN signal will be provided, coming 8 pixel clocks earlier, to compensate pipeline delay in the previous RAM interface. The encoded CVBS is 12 clocks earlier than the CVBS reference on the input of the previous ADC. The CLUTs are bypassed at MPK = HIGH in real-time.

Table 6 Function of register bits of Table 5

Index "00" VTBY	Video look-up table by-pass: 0 = not bypassed; 1 = bypassed (OR connectable with MPK)
FMT2 to FMT0	Input formats: FMT2 FMT1 FMT0 format 0 0 0 YUV 4:1:1 format; DMSD2 compatible 0 0 1 YUV 4:1:1 format; customized 0 1 0 YUV 4:2:2 format; DMSD2 compatible 0 1 1 YUV 4:2:2 format; customized 1 0 0 YUV 4:4:4 format 1 0 1 RGB 4:4:4 format 1 1 0 reserved 1 1 1 8-bit indexed colour
SCBW	Chrominance bandwidth: 0 = enhanced; 1 = standard
CCIR	Select level: 0 = DMSD2 levels; 1 = CCIR levels
MOD1 to MOD0	Select mode: MOD1 MOD0 mode 0 0 GENLOCK mode 0 1 stand-alone mode 1 0 slave mode 1 1 test mode
Index "01" TRER7 to TRER0	Test register Red (read/write via MPU-bus; write only via I²C-bus)
Index "02" TREG7 to TREG0	Test register Green (read/write via MPU-bus; write only via I²C-bus)
Index "03" TREB7 to TREB0	Test register Blue (read/write via MPU-bus; write only via I²C-bus)
Index "04" SYSEL1 to SYSEL0	Sync select: SYSEL1 SYSEL0 synchronized from 0 0 CSYN (active LOW; pin 3) 0 1 HSN and VSN (active LOW; pins 84 and 3) 1 0 CSYN (active HIGH; pin 3) 1 1 HSN and VSN (active HIGH; pins 84 and 3)
SCEN	Sync/clamping (HSY/HCL) enable: 0 = disabled (set to HIGH); 1 = enabled
VTRC	Select TV/VTR mode: 0 = 0 TV mode (slow); 1 = VTR mode (fast)
NINT	Select interlace of encoded signal: 0 = interlaced (262.5/262.5 or 312.5/312.5) 1 = non-interlaced (262/262 or 312/312 in modes 1 and 3 only)

HPLL	Select horizontal lock: 0 = lock enabled; 1 = lock disabled (crystal reference)
OEF	Status bit field organization (to be read): 0 = even field; 1 = odd field
HLCK	Status bit sync indication (to be read): 0 = locked to external sync 1 = external sync lost
Index "05" GDC5 to GDC0	GENLOCK delay compensation, note 1: data 00 to 3F equals timing of CVBS output signal is (46 – GDC) pixel clocks = t_{ofs} earlier with respect to reference point t_{REF1}. (t_{REF1} corresponds to the falling edge of the horizontal sync pulse of CVBS input signal; t_{ofs} is designated for propagation delay of extern GENLOCK source, Fig.10).
Index "06" IDEL7 to IDEL0	Increment delay: update of line-locked clock frequency (Table 5, data "52" hex recommended)
Index "07" PSO7 to PSO0	Phase sync in output signal, note 1: data 00 to 3F equals to active slope of HSN, VSN/CSYN is (58 – PSO) pixel clocks = t_{Rint} earlier with respect to reference point t_{REF2}. (t_{REF2} corresponds to PSO = 58; t_{Rint} is designated for pipeline delay of the feeding RAM interface, Fig.10).
Index "08" DD	Digital video encoder disable: 0 = enabled; 1 = disabled
KEYE	Keying enable: 0 = disabled; 1 = enabled (logically AND-connected with KEY)
SRC	Clock source: 0 = external system clock; 1 = DTV2 system clock
CPR	Clock phase reference: 0 = LDV is (pin 20); 1 = LDV is not
COKI	Colour-killer: 0 = colour on; 1 = colour off (subcarrier is switched off)
IM	Interrupt mask: 1 = interrupt not masked at sync lost (pin 58) 0 = interrupt masked.at sync lost (pin 58)
GPSW	General purpose switch at bit RTIN = 1: 0 = pin 57 LOW; 1 = pin 57 HIGH
SRSN	Software reset: 0 = no reset; 1 = reset (see reset procedure)
Index "09" BAME	Burst amplitude indication: 0..= burst amplitude measurement is overridden; colour lock always assumed 1 = burst amplitude is used to control the CLCK status bit, recommended for reference signal without subcarrier burst (pure black and white) in order to avoid PLL hunting.

<table>
<tr><td>MPKC1 to MPKC0</td><td>Multi-purpose key control: At MKP = LOW (pin 32) are all functions as given by software programming;
MKP = HIGH sets in real-time with respect to PDn(7-0).
<table>
<tr><th colspan="2">Set by bits</th><th colspan="4">in function blocks</th></tr>
<tr><th>MPKC1</th><th>MPKC0</th><th>input formatter</th><th>CLUTs</th><th>matrix</th><th>level matching</th></tr>
<tr><td>0</td><td>0</td><td>control via CCIR bit and FMT bits</td><td>bypass</td><td>control via FMT bits</td><td>control via CCIR bit</td></tr>
<tr><td>0</td><td>1</td><td>Format 5 (RGB) CCIR level</td><td>active, no indexed colour</td><td>active</td><td>CCIR level</td></tr>
<tr><td>1</td><td>X</td><td>Format 7 (indexed colour) CCIR level</td><td>active, indexed colour</td><td>active</td><td>CCIR level</td></tr>
</table></td></tr>
<tr><td>IEPI</td><td>Polarity of external PAL-ID signal (H/2 signal) from RTCI input (pin 57):
0 = not inverted; 1 = inverted</td></tr>
<tr><td>RTSC</td><td>Real-time select control: 0 = Real-time control HPLL increment is selected, that means, information about actual clock frequency from the digital colour decoder is received (SAA7151B or SAA7191B); the corresponding subcarrier frequency is calculated.
1 = Real-time control FSC increment with PAL-ID is selected, that means, information about actual subcarrier frequency and PAL-ID from the digital colour decoder is received (SAA7151B or SAA7191B).</td></tr>
<tr><td>RTIN</td><td>Select real-time control input: 0 = pin 57 is input for RTCI signal
1 = pin 57 is port output GPSW.</td></tr>
<tr><td>RTCE</td><td>Real-time control enabled: 0 = disabled; 1 = enabled (RTIN = 0)</td></tr>
<tr><td>Index "0C"
CHPS7 to CHPS0</td><td>Phase adjustment between chrominance output signal and reference:
00 to FF equals 0° to 358.59375° in steps of 1.40625°.</td></tr>
<tr><td>Index "0D"
FSC7 to FSC0</td><td>Fine adjustment of subcarrier frequency in non-GENLOCK modes:
00 to 7F increasing and FF to 80 decreasing equal approximately ±450 x 10^{-6} of the subcarrier frequency in 256 steps.</td></tr>
<tr><td>Index "0E"
CLCK</td><td>Lock to external chrominance (to be read): 0 = possible; 1 = not possible.</td></tr>
</table>

STD3 to STD0	Colour encoding standards:				
	STD3	STD2	STD1	STD0	standard
	0	0	0	0	NTSC 4.43; 60 Hz; SQP (12.27 MHz)
	0	0	0	1	NTSC 4.43; 50 Hz; SQP (14.75 MHz)
	0	0	1	0	PAL-B/G 4.43; 50 Hz; SQP (14.75 MHz)
	0	0	1	1	NTSC 4.43; 60 Hz; CCIR (13.5 MHz)
	0	1	0	0	NTSC 4.43; 50 Hz; CCIR (13.5 MHz)
	0	1	0	1	PAL-B/G 4.43; 50 Hz; CCIR (13.5 MHz)
	0	1	1	0	reserved
	0	1	1	1	reserved
	1	0	0	0	PAL-M; 60 Hz; SQP (12.27 MHz)
	1	0	0	1	PAL-M; 60 Hz; CCIR (13.5 MHz)
	1	0	1	0	PAL-N; 50 Hz; CCIR (13.5 MHz)
	1	0	1	1	PAL-N; 50 Hz; SQP (14.75 MHz)
	1	1	0	0	NTSC-M; 60 Hz; SQP (12.27 MHz)
	1	1	0	1	NTSC-M; 60 Hz; CCIR (13.5 MHz)
	1	1	1	0	reserved
	1	1	1	1	reserved
Status bits to be read via I²C-bus:					Table 7
Status bits to be read by microcontroller :					All registers from 00 up to 0F can be read via MPU-bus. Read-only bits are OEF, HCLK (index "04") and CLCK (index "0E")

Note to Table 6

1. Field blanking (Figures 11 and 12): normally, video to be encoded should not become active after the active edge of VSN or CSYN before line 22.5 at 50 Hz (line 18 at 60 Hz). Total field blanking is 25 lines at 50 Hz (21 lines at 60 Hz).

Colour look-up tables (CLUTs)

The CLUTs consist of RAM tables. The RAM tables can be loaded – with X = 0 to 255 according to equation 1 – for the signals R, G and B . Gamma-correction (pre-distortion) by following equation:

$$Y = NINT(b + a \times X1^{1/g}); \quad Y(X \leq 16) = 16; \quad Y(X \geq 235) = 235 \quad \text{(equation 1)}$$

with g = 2.2 is

$$a = 219 / (235^{-2.2} - 16^{-2.2})$$

$$b = 16 - a \times 16^{-2.2}$$

The RAM tables are loaded via MPU-bus or via I²C-bus (Table 8).

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 000X**
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress
DATA = data byte
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 7 I²C-bus status byte (address byte "B1")

FUNCTION		STATUS BYTE D7	D6	D5	D4	D3	D2	D1	D0
Read status		0	0	0	0	0	OEF	CLCK	HLCK

Function of the bits:

OEF	field organization: 0 = even field; 1 = odd field
CLCK	possibility of lock to external chrominance: 0 = possible; 1 = not possible
HLCK	sync indication: 0 = locked to external sync; 1 = external sync lost.

Table 8 I²C-bus write bytes (address byte "B0")

ACCESS TO CONTROL REGISTERS Address byte "B0" — subaddress byte "02" — index byte (00 to 0F, Table 5) — data bytes (auto-increment)
ACCESS TO CLUTS REGISTERS Address byte "B0" — subaddress byte "00" — CLUT address bytes (00 to FF) — 3 data bytes for one RGB sequence (auto-increment)

Table 9 Four different modes

STAND-ALONE MODE
The SAA7199B receives a line-locked clock CLKIN and generates CSYN or HSN/VSN output signals, which trigger the RGB respectively the YUV source signal to provide data and composite blanking CBN.
SLAVE MODE
The SAA7199B receives the line-locked clock CLKIN, CSYN or HSN/VSN, CBN and data from an RGB respectively YUV source. The sync inputs are edge-sensitive; the minimum active length is 1 PIXCLK. Optionally, a real-time control signal RTCI is received from a digital colour decoder.
GENLOCK MODE
Horizontal and vertical sync as well as colour are locked on a received CVBS reference signal. The CVBS reference signal generates also a line-locked clock by the SAA7197 clock generator. Auxiliary signals HCL and HSY as well as CSYN or HSN/VSN are generated to trigger the RGB respectively the YUV source providing data and composite blanking CBN.
TEST MODE
Like stand-alone mode, but data to be encoded are the contents of the test registers TRER, TREGand TREB. VSN/CSYN and HSN outputs are in 3-state condition.

Relationship between horizontal frequency and colour subcarrier frequency in non-GENLOCK mode

a) Internal subcarrier frequency with n = integer:

PAL: $f_{SC} = f_H (n/4 + 1/625)$ respectively $f_H (n/4 + 1/525)$ NTSC: $f_{SC} = f_H (n/2)$

Necessary conditions: Non-GENLOCK mode; RTCE = 0, FSCO = 00h; phase coupling of the two frequencies is given by definite phase reset every 8th fields at PAL (4th fields at NTSC).

FSCO $\neq$ 00h adjusts the subcarrier frequency, phase reset is disabled and phase between f_{SC} and f_H is not constant.

b) External subcarrier frequency:

f_{SC} is given by RTCI real-time input from a digital colour decoder.

Necessary conditions: Slave mode; RTCE = 1, RTSC = 1. The 8th respectively 4th field reset is enabled at FSCO = 00h (disabled at FSCO $\neq$ 00h). The subcarrier frequency itself is not influenced by FSCO bits, it is given by real-time increment.

c) External HPLL increment:

f_{SC} is calculated by means of RTCI real-time input signal from a digital colour decoder. The frequency of f_{SC} depends on the absolute crystal frequency value used by the digital colour decoder.

Necessary conditions: Slave mode; RTCE = 1, RTSC = 0. The 8th respectively 4th field reset is enabled at FSCO = 00h (disabled at FSCO $\neq$ 00). The subcarrier frequency itself is influenced by FSCO bits.

The absolute phase relationship between sync and subcarrier (colour burst out) can be influenced in all three cases by CHPS(7-0) register byte (index "0C").

Data input formats

One clock cycle equals 12.27 MHz, 13.5 MHz or 14.75 MHz (Cb = (B-Y) equals U; Cr = (R-Y) equals V; (n) = number of pixel).

Table 10 Format 0: DMSD2-compatible YUV 4:1:1 format (FMT-bits in index "00"= 000)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	Cb5(0)	Cb3(0)	Cb1(0)	Cb7(4)	Cb5(4)	Cb3(4)	Cb1(4)
PD3(6)	Cb6(0)	Cb4(0)	Cb2(0)	Cb0(0)	Cb6(4)	Cb4(4)	Cb2(4)	Cb0(4)
PD3(5)	Cr7(0)	Cr5(0)	Cr3(0)	Cr1(0)	Cr7(4)	Cr5(4)	Cr3(4)	Cr1(4)
PD3(4)	Cr6(0)	Cr4(0)	Cr2(0)	Cr0(0)	Cr6(4)	Cr4(4)	Cr2(4)	Cr0(4)
PD3(3-0)	not used							
PD1(7-0)	not used							

Table 11 Format 1: Customized YUV 4:1:1 format (FMT-bits in index "00" = 001)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	-	Cr7(0)	-	Cb7(4)	-	Cr7(4)	-
PD3(6)	Cb6(0)	-	Cr6(0)	-	Cb6(4)	-	Cr6(4)	-
PD3(5)	Cb5(0)	-	Cr5(0)	-	Cb5(4)	-	Cr5(4)	-
PD3(4)	Cb4(0)	-	Cr4(0)	-	Cb4(4)	-	Cr4(4)	-
PD3(3)	Cb3(0)	-	Cr3(0)	-	Cb3(4)	-	Cr3(4)	-
PD3(2)	Cb2(0)	-	Cr2(0)	-	Cb2(4)	-	Cr2(4)	-
PD3(1)	Cb1(0)	-	Cr1(0)	-	Cb1(4)	-	Cr1(4)	-
PD3(0)	Cb0(0)	-	Cr0(0)	-	Cb0(4)	-	Cr0(4)	-
PD1(7-0)	not used							

Table 12 Format 2: DMSD2-compatible YUV 4:2:2 format (FMT-bits in index "00" = 010)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	Cr7(0)	Cb7(2)	Cr7(2)	Cb7(4)	Cr7(4)	Cb7(6)	Cr7(6)
PD3(6)	Cb6(0)	Cr6(0)	Cb6(2)	Cr6(2)	Cb6(4)	Cr6(4)	Cb6(6)	Cr6(6)
PD3(5)	Cb5(0)	Cr5(0)	Cb5(2)	Cr5(2)	Cb5(4)	Cr5(4)	Cb5(6)	Cr5(6)
PD3(4)	Cb4(0)	Cr4(0)	Cb4(2)	Cr4(2)	Cb4(4)	Cr4(4)	Cb4(6)	Cr4(6)
PD3(3)	Cb3(0)	Cr3(0)	Cb3(2)	Cr3(2)	Cb3(4)	Cr3(4)	Cb3(6)	Cr3(6)
PD3(2)	Cb2(0)	Cr2(0)	Cb2(2)	Cr2(2)	Cb2(4)	Cr2(4)	Cb2(6)	Cr2(6)
PD3(1)	Cb1(0)	Cr1(0)	Cb1(2)	Cr1(2)	Cb1(4)	Cr1(4)	Cb1(6)	Cr1(6)
PD3(0)	Cb0(0)	Cr0(0)	Cb0(2)	Cr0(2)	Cb0(4)	Cr0(4)	Cb0(6)	Cr0(6)
PD1(7-0)	not used							

Table 13 Format 3: Customized YUV 4:2:2 format (FMT-bits in index "00" = 011)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7-0)	Cb (0)	-	Cb (2)	-	Cb (4)	-	Cb (6)	-
PD1(7-0)	Cr (0)	-	Cr (2)	-	Cr (4)	-	Cr (6)	-

Table 14 Format 4: YUV 4:4:4 format (FMT-bits in index "00" = 100)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7-0)	Cb (0)	Cb (1)	Cb (2)	Cb (3)	Cb (4)	Cb (5)	Cb (6)	Cb (7)
PD1(7-0)	Cr (0)	Cr (1)	Cr (2)	Cr (3)	Cr (4)	Cr (5)	Cr (6)	Cr (7)

Table 15 Format 5: RGB 4:4:4 format (FMT-bits in index "00" = 101)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD1(7-0)	R(0)	R(1)	R(2)	R(3)	R(4)	R(5)	R(6)	R(7)
PD2(7-0)	G(0)	G(1)	G(2)	G(3)	G(4)	G(5)	G(6)	G(7)
PD3(7-0)	B(0)	B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	B(7)

Table 16 Format 7: Indexed colour format (FMT-bits in index "00" = 111). Input codes 0 to 255 are allowed, output code of CLUTs should preferably be the same as given in Format 5

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	INC(0)	INC(1)	INC(2)	INC(3)	INC(4)	INC(5)	INC(6)	INC(7)

Table 17 Input data levels for formats 0 to 4 and 5; EBU colour bar: 100 % white equals 100 IRE intensity; 75 % colour saturation for formats 1 to 4, 100 % for format 5

INPUT CHANNEL	LEVEL	DIGITAL LEVEL	CODE	CCIR-BIT	FORMAT
Y channel	0 IRE 100 IRE	12 230	offset binary	0	formats 0 to 4
Cb channel	bottom peak colourless top peak	–101 0 100	two's complement	0	formats 0 to 4
Cr channel	bottom peak colourless top peak	–106 0 105	two's complement	0	formats 0 to 4
Y channel	0 IRE 100 IRE	16 235	offset binary	1	formats 0 to 4
Cb channel	bottom peak colourless top peak	44 128 212	offset binary	1	formats 0 to 4
Cr channel	bottom peak colourless top peak	44 128 212	offset binary	1	formats 0 to 4
R, G and B	0 IRE 100 IRE	16 235	offset binary	1	format 5

GENLOCK input data

Table 18 Format 7: CVBS GENLOCK input data format has 8-bit word length. The input data come from an analog-to-digital converter (TDA8708) with gain-controlled and clamped CVBS or VBS signals

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
CVBS7 to CVBS0	CVBS(0)	CVBS(1)	CVBS(2)	CVBS(3)	CVBS(4)	CVBS(5)	CVBS(6)	CVBS(7)

CONDITIONS OF CVBS INPUT SIGNAL	TWO'S COMPLEMENT REPRESENTATION	
sync bottom	coresponding to binary code	–128
0 IRE (black)	coresponding to binary code	–64*
100 IRE (white)	coresponding to binary code	95
top peak of 75 % colour	coresponding to binary code	95
bottom peak of 75 % colour	coresponding to binary code	–100

* If exactly matched levels are wanted in the internal multiplexer, the value 0 IRE should correspond to –68 and 100 IRE to 82.

Encoding data levels

Input data levels are transformed in three stages:

- in the matrix when RGB or indexed colour is applied (formats 5 and 7)
- in the normalizing amplifier depending on 50/60 Hz mode and CCIR-bit (index "00")
- in the modulator

Table 19(a) Y and C output levels in **50 Hz** mode (PAL) for RGB input levels (100/100 colour bar)

SIGNAL	INPUT DATA			MATRIX OUTPUT DATA			NORMALIZER OUTPUT DATA			MODULATOR OUTPUT DATA	
	R	G	B	(R-Y)	Y	(B-Y)	V*	Y	U	Y	C**
white	235	235	235	128	235	128	0	421	0	421	0
yellow	235	235	16	146	210	16	29	387	−132	387	±135
cyan	16	235	235	16	170	166	−184	332	44	332	±189
green	16	235	16	34	145	54	−155	297	−87	297	±178
magenta	235	16	235	221	107	202	152	245	86	245	±175
red	235	16	16	240	82	90	183	211	−45	211	±188
blue	16	16	235	110	41	240	−30	154	131	154	±134
black	16	16	16	128	16	128	0	120	0	120	0
blanking	X	X	X	X	X	X	X	X	X	120	0
burst	X	X	X	X	X	X	45	X	−45	X	±63
top sync	X	X	X	X	X	X	X	X	X	0	X

Table 19(b) Y and C output levels in **60 Hz** mode (NTSC) for RGB input levels (100/100 colour bar)

SIGNAL	INPUT DATA			MATRIX OUTPUT DATA			NORMALIZER OUTPUT DATA			MODULATOR OUTPUT DATA	
	R	G	B	(R-Y)	Y	(B-Y)	V	Y	U	Y	C**
white	235	235	235	128	235	128	0	416	0	416	0
yellow	235	235	16	146	210	16	29	385	−132	385	±135
cyan	16	235	235	16	170	166	−184	335	44	335	±189
green	16	235	16	34	145	54	−155	303	−87	303	±178
magenta	235	16	235	221	107	202	152	256	86	256	±175
red	235	16	16	240	82	90	183	225	−45	225	±188
blue	16	16	235	110	41	240	−30	173	131	173	±134
black	16	16	16	128	16	128	0	142	0	142	0
blanking	X	X	X	X	X	X	X	X	X	120	0
burst	X	X	X	X	X	X	0	X	−64	X	±64
top sync	X	X	X	X	X	X	X	X	X	0	X

X = not defined; * the V component is inverted in the PAL line; ** the ± figures are peak values of the subcarrier signal.

Chrominance filtering in the encoder

1. Decimation for 4:4:4 formats input data (Formats 4, 5 and 7; Fig.4).
2. Interpolation for 4:1:1 input data into 4:2:2 data – also suitable to reduce the bandwidth of 4:2:2 data. This filter is controlled by SCBW-bit (SCWB = 1 means active).
3. Interpolation at 13.5 MHz for 4:2:2 input data into 4:4:4 data before modulating baseband signals onto the colour subcarrier. Figures 5, 6 and 7 show the overall transfer characteristics of chrominance in "standard bandwidth condition" (SCBW = 1). Figures 8 and 9 show the overall transfer characteristics of chrominance in "enhanced bandwidth condition" (SCBW = 0), which is not possible for 4:1:1 input data. The transfer curves are slightly different at 12.27 and 14.75 MHz.

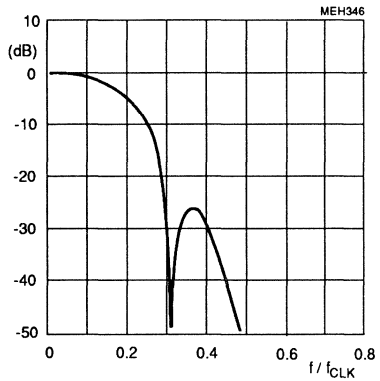


Fig.4 Transfer characteristics of 4:4:4 to 4:2:2 decimator.

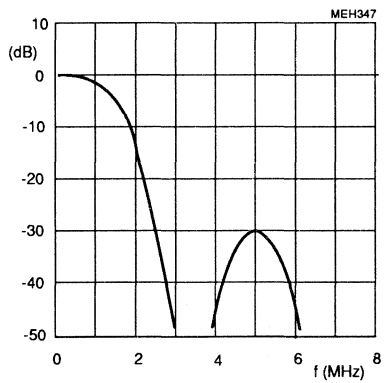


Fig.5 Overall transfer characteristics 4:1:1 input data.

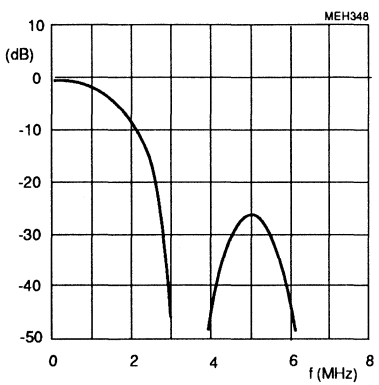


Fig.6 Overall transfer characteristics 4:2:2 input data (SCBW-bit = 1).

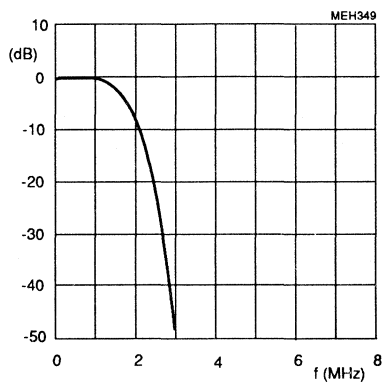


Fig.7 Overall transfer characteristics 4:4:4 input data (SCBW-bit = 1).

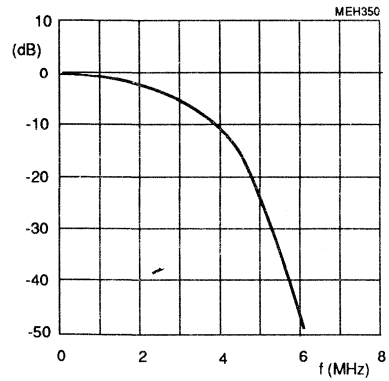


Fig.8 Overall transfer characteristics 4:2:2 input data (SCBW-bit = 0).

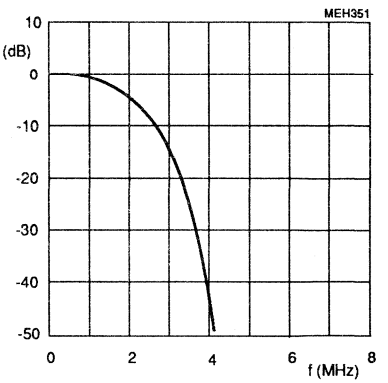


Fig.9 Overall transfer characteristics 4:4:4 input data (SCBW-bit = 0).

Accuracy of matrix

Evaluation of quantization errors.

The RGB to YUV matrix is realized according to the following algorithm:

$$Y = INT((NINT(R \times 2 \times 0.299) + NINT(G \times 2 \times 0.587) + NINT(B \times 2 \times 0.114)) / 2)$$

$$U = NINT((B-Y) \times 0.57722)$$

$$V = NINT((R-Y) \times 0.72955)$$

Errors can occur in the calculation of Y, which in consequence influence the U and V outputs.
The greatest positive error occurs, if in all of the three for Y calculation used ROMs the values are rounded up to 0.5 LSB, and no truncation error of 0.5 LSB is generated after summation:

(3 x 0,5 LSB) / 2 = +0.75 LSB;
with truncation "error": (3 x 0,5 LSB) / 2 – 0.5 LSB = +0.25 LSB.

The greatest negative error occurs at rounding off in all the three ROMs and by consecutive truncation:

3 x (–0,5 LSB) / 2 – 0.5 LSB = –1.25 LSB.

As a result, the matrix error can be ±1 digit, which corresponds to approximately ±0.5% differential non-linearity.

Estimation of noise by quantization

The sum of all sqared quantization errors is SS normalized to 220^3 input combinations (3-dimensional colour scale).

$$SS = 0.187545\ LSB^2.$$

Compared with noise energy for ideal quantization, $SSI = 1/12\ LSB^2$ results in a deterioration by the conversion matrix of

$$D = 10 \log (0.187545 \times 12) = 3.5\ dB \text{ (equals 0.5 bit).}$$

If SS is the sum of all sqared quantization errors, normalized to 220 input combinations of a grey-scale (R = G = B), then is

$$SS = 0.12273\ LSB^2.$$

Compared with noise energy for ideal quantization, $SSI = 1/12\ LSB^2$ results in a deterioration by the conversion matrix of

$$D = 10 \log (0.12273 \times 12) = 1.7\ dB \text{ (equals 0.25 bit).}$$

Normalizing amplifiers in luminance channel

The absolute amplification error for 50 Hz non-set-up signals is 0.375 %; differential non-linearity is –0.333 % (equals –1 LSB).
The absolute amplification error for 60 Hz set-up signals is –1.5 %; differential non-linearity is –0.365 % (equals –1 LSB).

Normalizing amplifiers in chrominance channel

The absolute amplification error is approximately ±0.5 % with a truncation error of –0.5 LSB.

The subcarrier amplitude for standards with luminance set-up is the same as for the standards without luminance set-up.

Modulator

The absolute amplification error is –0.39 %; there is no truncation error.

Functional timing

GENLOCK mode:
The encoded signal can be generated earlier with respect to CVBS(7-0) bits (offset t_{ofs} set by GDC-bits; index "05"). The HSN output signal can be generated early by PSO-bits (index "07") with respect to CBN to compensate for pipelining delay t_{Rint} of the RAM interface (valid also in stand-alone mode).

The horizontal timing is independent of active video at data inputs PDn(7-0). The line blanking period on the outputs is set to approximately 12 µs in 50 Hz standards (11 µs in 60 Hz standards).

Slave mode:
HSN pin is used as an input. The active edge of the input signal is assumed to fit to the incoming CBN signal. Deviations can be compensated in the range of the GCD-bits (index "05").

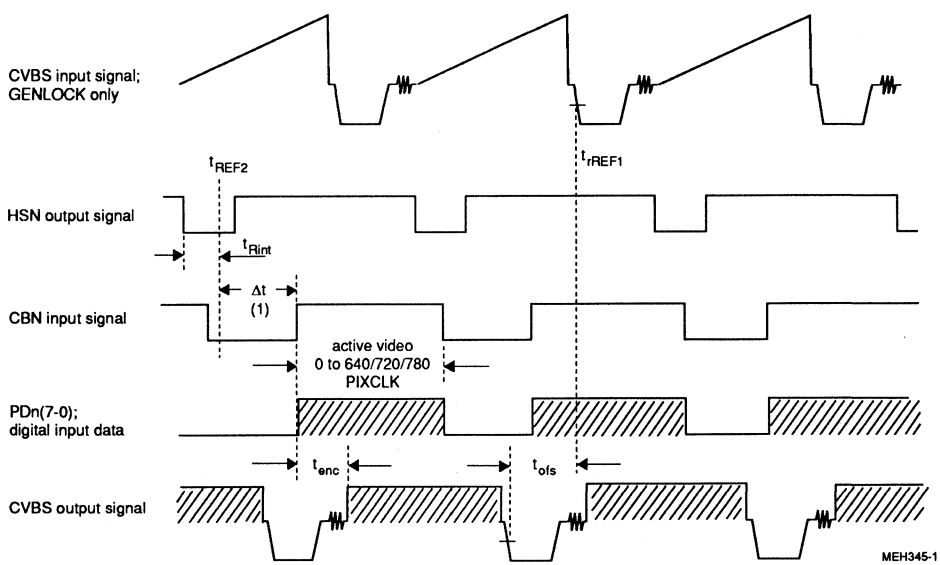


Fig.10 Horizontal timing. t_{Rint} = pipeline delay of RAM interface adjustable from –5 to +58 pixel clocks (PIXCLK); t_{ofs} = propagation delay of external GENLOCK line adjustable from –17 to +46 pixel clocks.

(1) Δt = 125 x PIXCLK at 12.27 MHz
Δt = 163 x PIXCLK at 14.75 MHz
Δt = 134 x PIXCLK at 13.50 MHz / 50 Hz mode
Δt = 122 x PIXCLK at 13.50 MHz / 60 Hz mode

The t_{enc} time is the total delay from data input to analog CVBS output; it is 55 pixel clock periods long (PIXCLK) plus the propagation delay of the LDV input register regardless of mode and colour standard.
The key input signal is delay-compensated with respect to PDn(7-0)data input.
The generated vertical field and burst blanking sequences are shown in Fig.11 (50 Hz PAL) and Fig.12 (60 Hz NTSC).

Reset

Prior to a reset all outputs are undefined. RESN = LOW sets the circuit into the slave mode: MOD1 bit = 1; MOD0-bit = 0. All other control register bits are set to zero. The outputs CSYN/VSN, HSN, SLT, HSY and HCL are automatically set to high-impedance state. The I^2C-bus interface is set to a slave receiver.
The D(7-0) pins of the MPU interface are inputs during RESN = LOW. As the circuit requires an external clock signal on pin CLKIN in slave mode, the clock select signal CLKSEL (pin 50) must be LOW during RESN = LOW (pin 54). The LOW time of RESN is preliminary at least 50 pixel clock periods long.

Disable chip

All analog outputs are set to zero by DD-bit = 1 (index "08"); while the outputs CSYN/VSN, HSN, HCL, HSY and SLT are set to high-impedance state. The internal clock is divided by 4 at DD-bit = 1.
The circuit can be disabled for any reason. It must be disabled when CLKIN exceeds 32 MHz. After setting DD-bit = 1, the CLKIN input signal can be set to a frequency of < 60 MHz (modification of control registers and RAM tables is not ensured).
To enable the circuit again, CLKIN must be set to a frequency < 32 MHz, a reset (hardware) then is required to set DD-bit to zero.

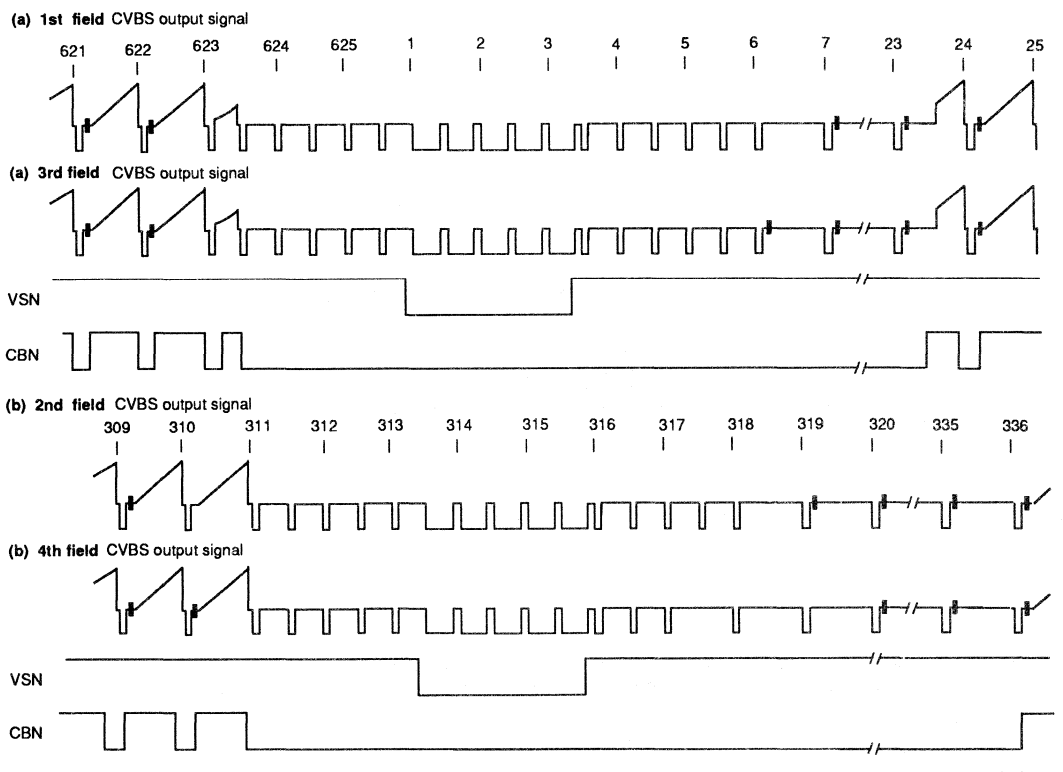


Fig.11 Vertical field and burst blanking sequence for PAL 50 Hz mode.

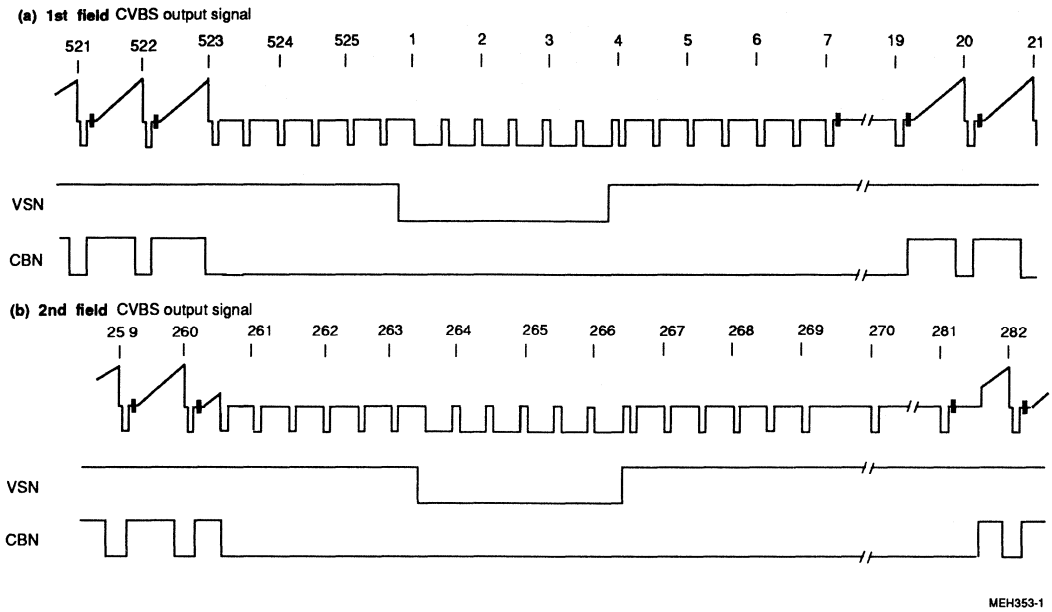


Fig.12 Vertical field and burst blanking sequence for NTSC 60 Hz mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage (pin 2)	−0.3	7	V
V_{DDD2}	supply voltage (pin 21)	−0.3	7	V
V_{DDD3}	supply voltage (pin 41)	−0.3	7	V
V_{DDA1}	supply voltage (pin 66)	−0.3	7	V
V_{DDA2}	supply voltage (pin 70)	−0.3	7	V
V_{DDA3}	supply voltage (pin 72)	−0.3	7	V
V_{DDA4}	supply voltage (pin 64)	−0.3	7	V
$V_{diff\ GND}$	difference voltage between digital and analog ground pins ($V_{DDDn} - V_{DDAn}$)	-	±100	mV
V_n	voltage on all pins, grounds excluded	0	V_P	V
P_{tot}	total power dissipation	-	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through an 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pins 2, 21 and 42)		4.5	5	5.5	V
V_{DDA}	analog supply voltage range (pins 66, 70 and 72)		4.75	5	5.25	V
I_{DDD}	digital supply current I_{DDD1} to I_{DDD3}	40 pF output load	-	-	140	mA
I_{DDA}	analog supply current I_{DDA1} to I_{DDA3}	40 pF output load	-	-	60	mA
Data and control inputs (pins 3 to 20, 23 to 40, 43 to 46, 49, 50, 54 to 56, 59, 73 and 76 to 84)						
V_{IL}	input voltage LOW	note 1	0	-	0.8	V
V_{IH}	input voltage HIGH	note 1	2.0	-	V_{DDD}+ 0.5	V
I_{LI}	input leakage current		-	-	±1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_I	input capacitance	data inputs	-	-	8	pF
		CLKIN, LLC, LDV	-	-	10	pF
		3-state I/O	-	-	10	pF
LFCO output (pin 61)						
V_o	output signal (peak-to-peak value)		1.4	-	2.6	V
V_{61}	output voltage range		0	-	V_{DDD}	V
Data and other control outputs (pins 3, 51, 52, 57, 58, 60, 74 and 75)						
$V_{O\,L}$	output voltage LOW	note 2	0	-	0.6	V
$V_{O\,H}$	output voltage HIGH	note 2	2.4	-	V_{DDD}	V
C, Y and CVBS analog outputs (pins 65, 67 and 69)						
V_o	output signal (peak-to-peak value)	without load	-	2	-	V
$V_{65,67,69}$	output voltage range	without load; V_{DDA} = 5 V	0.2	-	2.2	V
$R_{65,67,69}$	internal serial output resistance	not tested	18	25	35	Ω
$R_{L\,65,67,69}$	output load resistance	recommendation	90	-	-	Ω
B	output signal bandwidth	-3 dB	10	-	-	MHz
ILE	LF integral linearity error	9-bit data	-	-	±1.0	LSB
DLE	LF differential linearity error	9-bit data	-	-	±0.5	LSB
I_{CUR}	input current (pin 71)	Fig.1; $R_{70\text{-}71}$ = 20 kΩ	-	300	-	µA
I²C-bus SDA and SCL (pins 47 and 48)						
$V_{I\,L}$	input voltage LOW		–0.5	-	1.5	V
$V_{I\,H}$	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	µA
V_{OL}	SDA output voltage (pin 47)	I_{47} = 3 mA	-	-	0.4	V
I_{47}	output current	during acknowledge	3	-	-	mA
Crystal oscillator		Fig.14				
f_n	nominal frequency	3rd harmonic; Table 1	-	24.576	-	MHz
		3rd harmonic; Table 1	-	26.8	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	50	-	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	40	80	Ω
	motional capacitance C_1		-	1.5±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LLC and LDV timing (pins 55 and 20)		Fig.16				
t_{LLC}	cycle time	note 3	31.5	-	44.5	ns
t_{CH}	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
t_{LDV}	cycle time		63	-	89	ns
t_{SUL}	LDV set-up time		8	-	-	ns
t_{HDL}	LDV hold time		15	-	-	ns
PIXCLK and CLKO timing (pins 51 and 52)		Fig.16				
t_{DCK}	PIXCLK and CLKO delay time		tbf	-	25	ns
PD1(7-0), PD2(7-0), PD3(7-0), CBN, MPK, KEY and RTCI input timing (pins 4 to 19, 23 to 32, 57 and 73)						
t_{SUD}	input data set-up time	Fig.16	4	-	-	ns
t_{HDD}	input data hold time		4	-	-	ns
CVBS (7-0), VSN/CSYN and HSN timing (pins 76 to 83, 3 and 84)						
t_{SU}	input data set-up time	Fig.17	10	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
CREF timing (pin 56)		Fig.17				
t_{SUC}	input set-up time		10	-	-	ns
t_{HDC}	input hold time		2	-	-	ns
MPU timing A1, A0, R/WN, CSN, D(7-0) (pins 33 to 36, 37 to 40 and 43 to 46); Fig.18						
t_{SA}	A1 and A0 address set-up time (pins 33, 34)		4	-	-	ns
t_{HA}	A1 and A0 address hold time		25	-	-	ns
t_{SR}	R/WN set-up time (pin 35)		4	-	-	ns
t_{HR}	R/WN hold time		25	-	-	ns
t_{CL}, t_{CH}	CSN pulse width LOW and HIGH	note 4	95	-	-	ns
t_{SW}	data set-up time (D7 to D0)	write	80	-	-	ns
t_{HW}	data hold time (D7 to D0)	write	5	-	-	ns
t_{HDR}	data output hold time (D7 to D0)	read; note 5	5	-	-	ns
t_{ZR}	delay to driven ports (D7 to D0)	read	5	-	-	ns
t_{DR}	delay to ports valid (D7 to D0)	read; note 1	-	-	275	ns
t_{RZ}	port outputs disable time (D7 to D0)	read	-	-	25	ns
Output timing (pins 3, 74, 75 and 84)		Fig.17				
t_{OD}	output delay time	minimum clock period	-	-	40	ns

Notes to the characteristics

1. XTAL, XTALI and TP are not characterized with respect to levels; CLKO is characterized up to 32 MHz and PIXCLK up to 16 MHz
2. Levels are measured with load circuit. LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 40 pF at 3V (TTL load).
3. t_{LLC} has to be in the range 63 to 89 ns at CREF = HIGH (pin 56); t_{LLC} = 16.5 ns is allowed only if the multiplexer clock is active.
4. $t_{PIXCLK(min)}$ + 5 ns.
5. 3 x ($t_{PIXCLK(min)}$ + 5 ns).

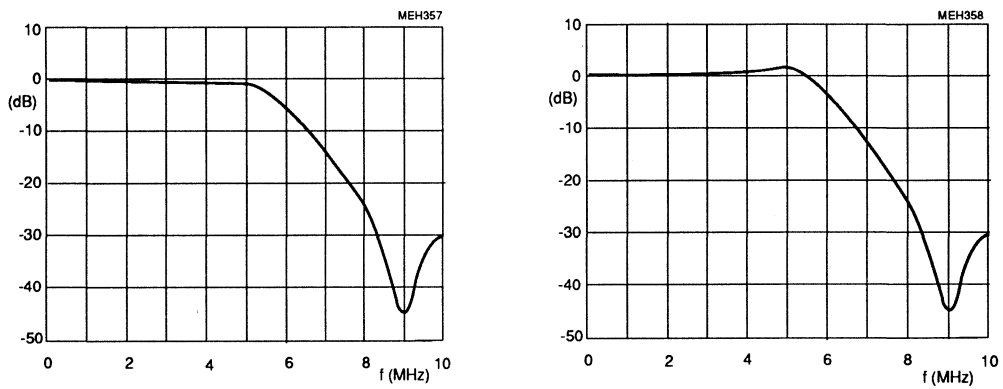


Fig.13 Characteristics of low-pass post-filters. Left: without compensation of DC hold characteristic. Right: with compensatior. of DC hold characteristic.

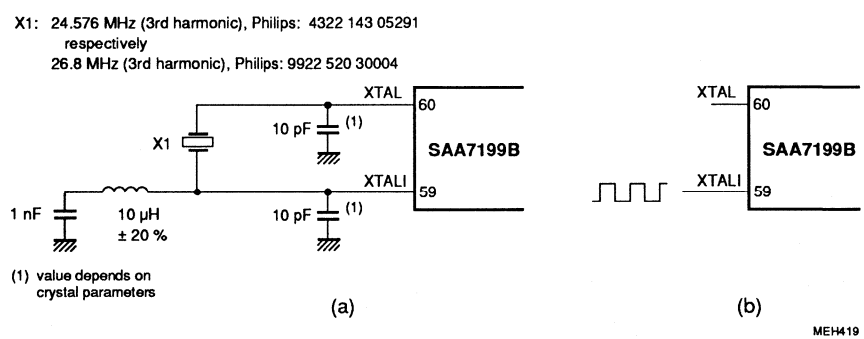
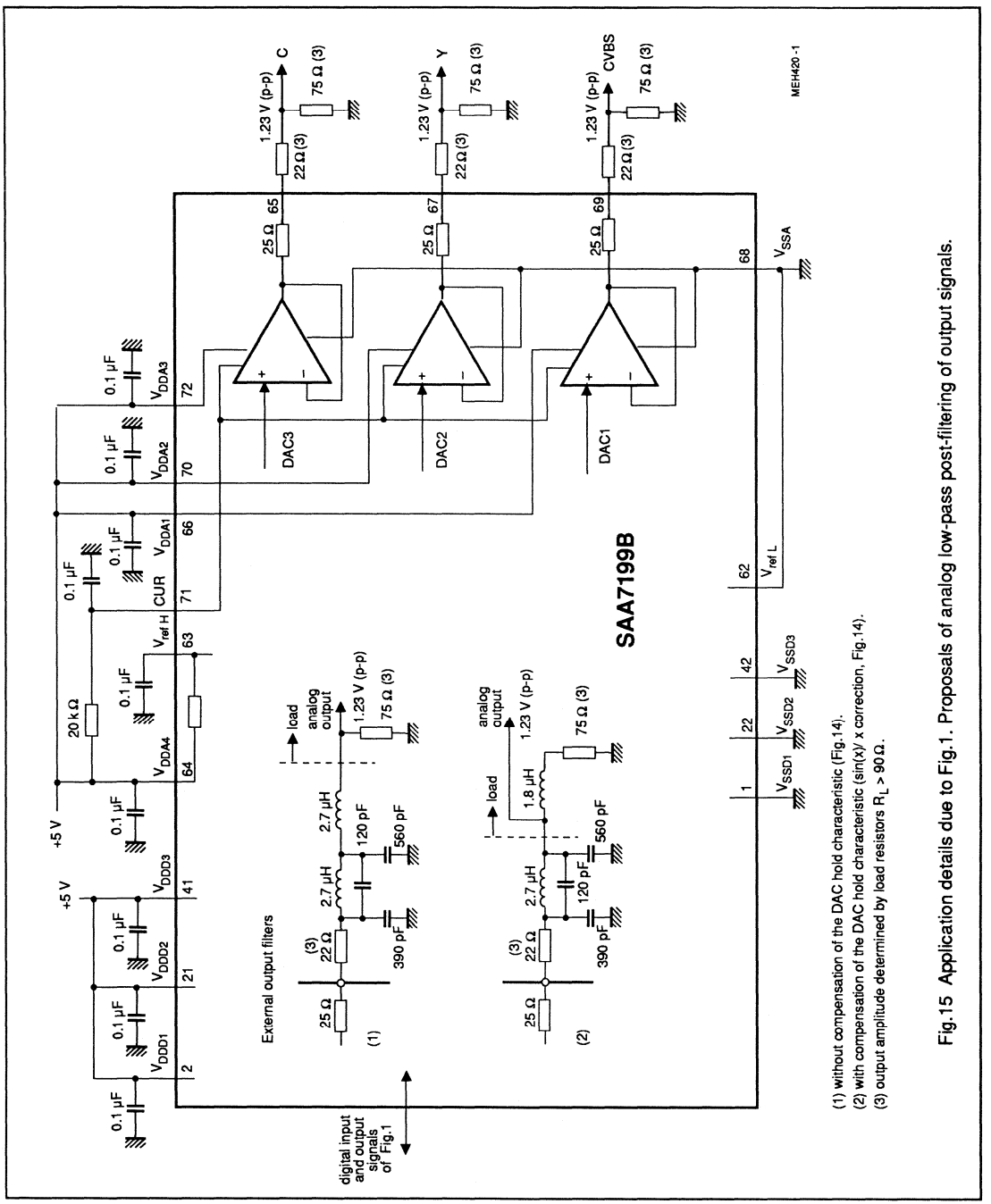


Fig.14 Oscillator application (a) and optional external clock sync (b).



(1) without compensation of the DAC hold characteristic (Fig.14).
(2) with compensation of the DAC hold characteristic (sin(x)/ x correction, Fig.14).
(3) output amplitude determined by load resistors $R_L > 90\,\Omega$.

Fig.15 Application details due to Fig.1. Proposals of analog low-pass post-filtering of output signals.

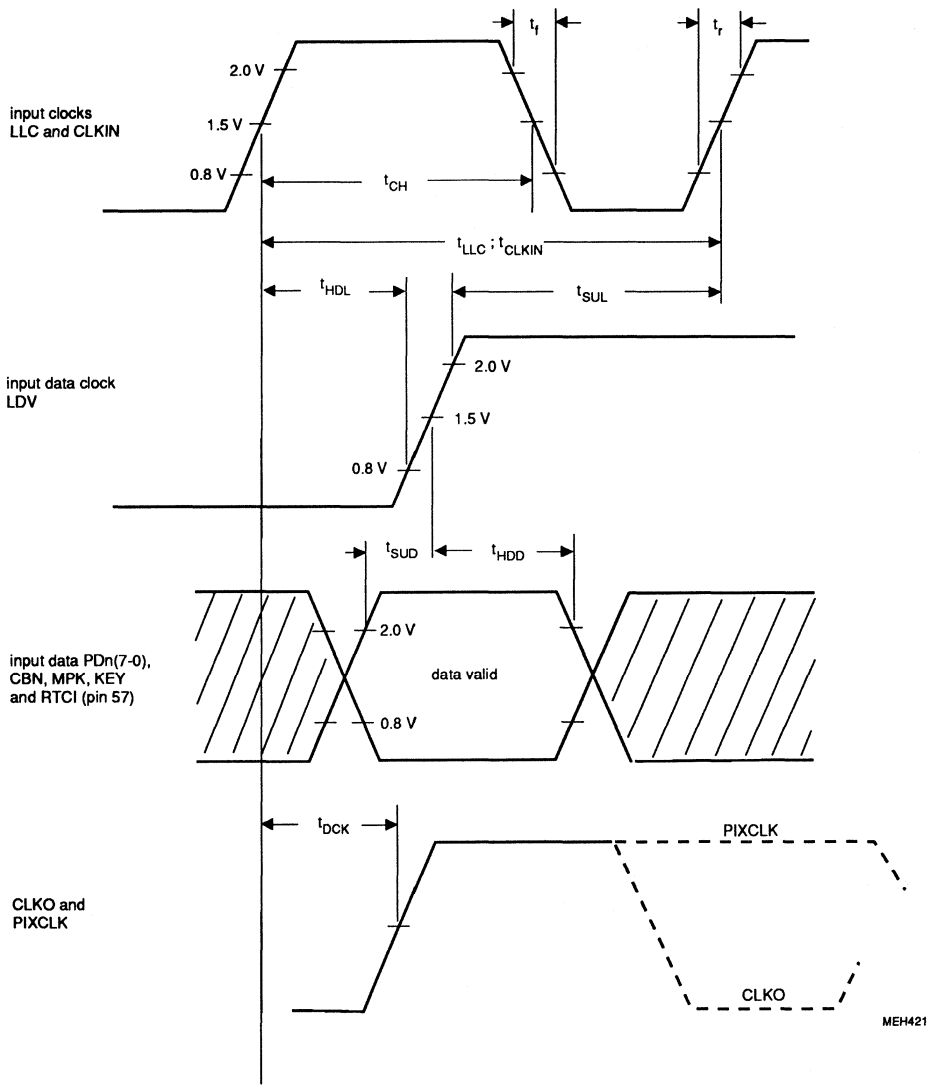


Fig.16 LDV input data timing.

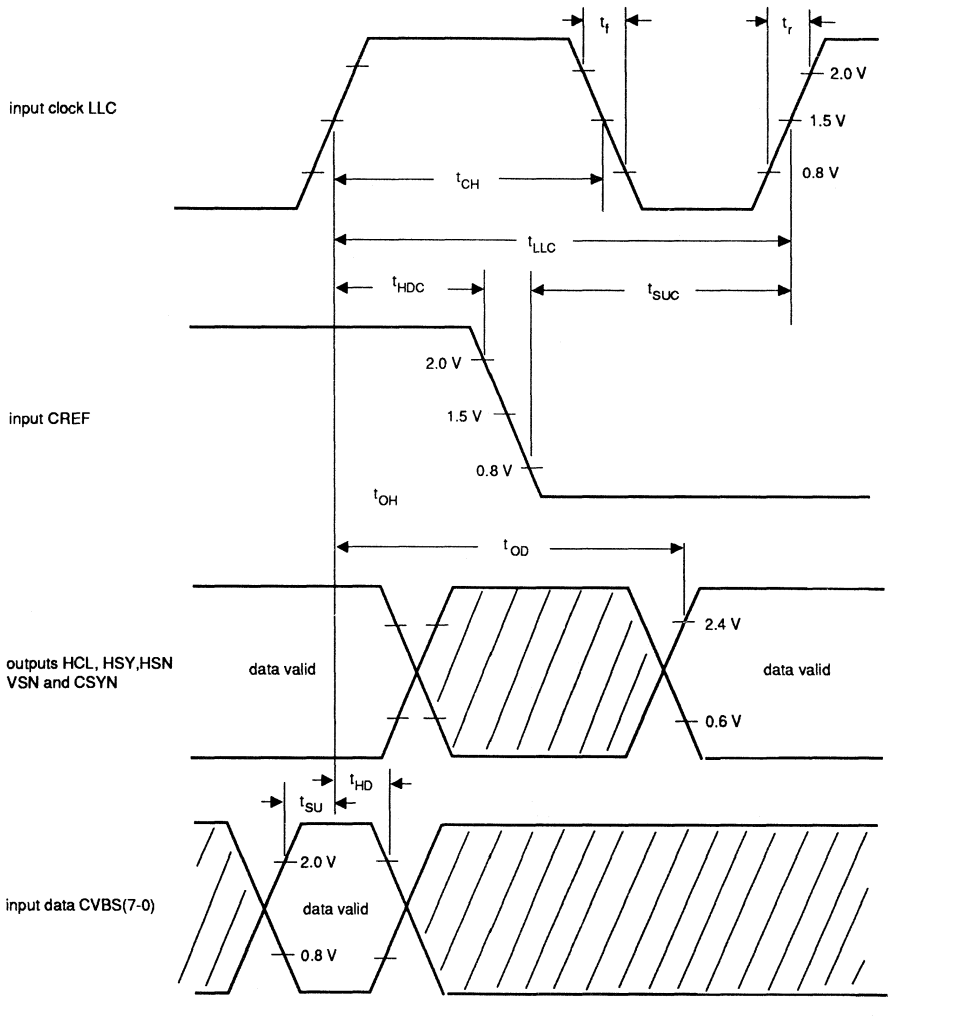


Fig.17 Clock and data timing.

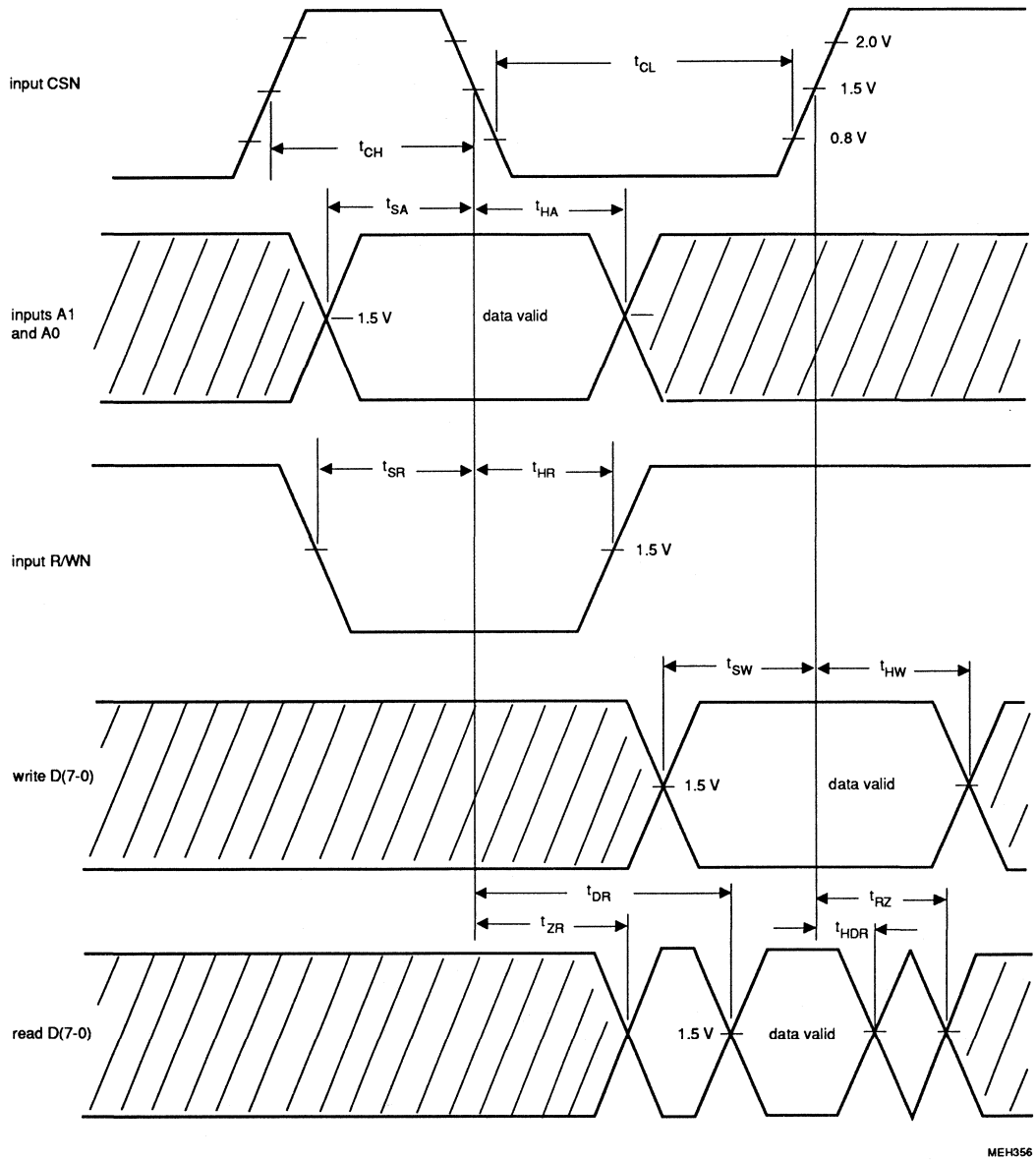


Fig.18 MPU-bus timing.

Terrestrial Digital Sound Decoder (TDSD2) SAA7282

FEATURES

- Full EBU NICAM 728 specification decoder
- Microcomputer controlled via I²C-bus
- Automatic decoding and output configuration depending upon transmission:
  - digital stereo
  - digital mono and data
  - 2 independent mono signals
- On board RAM for de-interleaving and 10 to 14-bit word expansion
- Automatic mute function which silences the digital data and switches to FM sound (if valid) when error rate exceeds user definable limit
- User mute function ($\overline{\text{MUTE}}$ pin) to enable user to perform muting to their own software algorithm if required, or to simply silence the output
- 4 times over-sampling digital filter
- Selectable digital de-emphasis
- 256 times over-sampling Noise Shapers
- Fully integrated 1-bit DACs
- Integrated switching networks allowing selection between NICAM Sound, FM Sound or external "Daisy-Chain" input
- Digital Audio Interface conforming with EBU/IEC 958
- I²C-bus transceiver enabling a master device to read:
  - status information
  - error count byte
  - additional data bits

  and write:
  - switch control codes
  - decoder control
  - upper and lower error rate limits

APPLICATIONS

- Television receivers
- Video cassette recorders

GENERAL DESCRIPTION

Performing all digital decoding functions for a NICAM 728 digital stereo sound system, the SAA7282 is a highly integrated CMOS circuit which only requires a DQPSK (Differential Quadrature Phase Shift Keying) demodulator (TDA8732) and minimal external components to achieve a full NICAM solution.

The device may also be interfaced to other DQPSK demodulators.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	50	–	mA
f_{XTAL}	crystal frequency	–	8.192	–	MHz
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7282ZP	32	DIL32SHR	plastic	SOT232A
SAA7282GP	44	QFP	plastic	SOT205AG

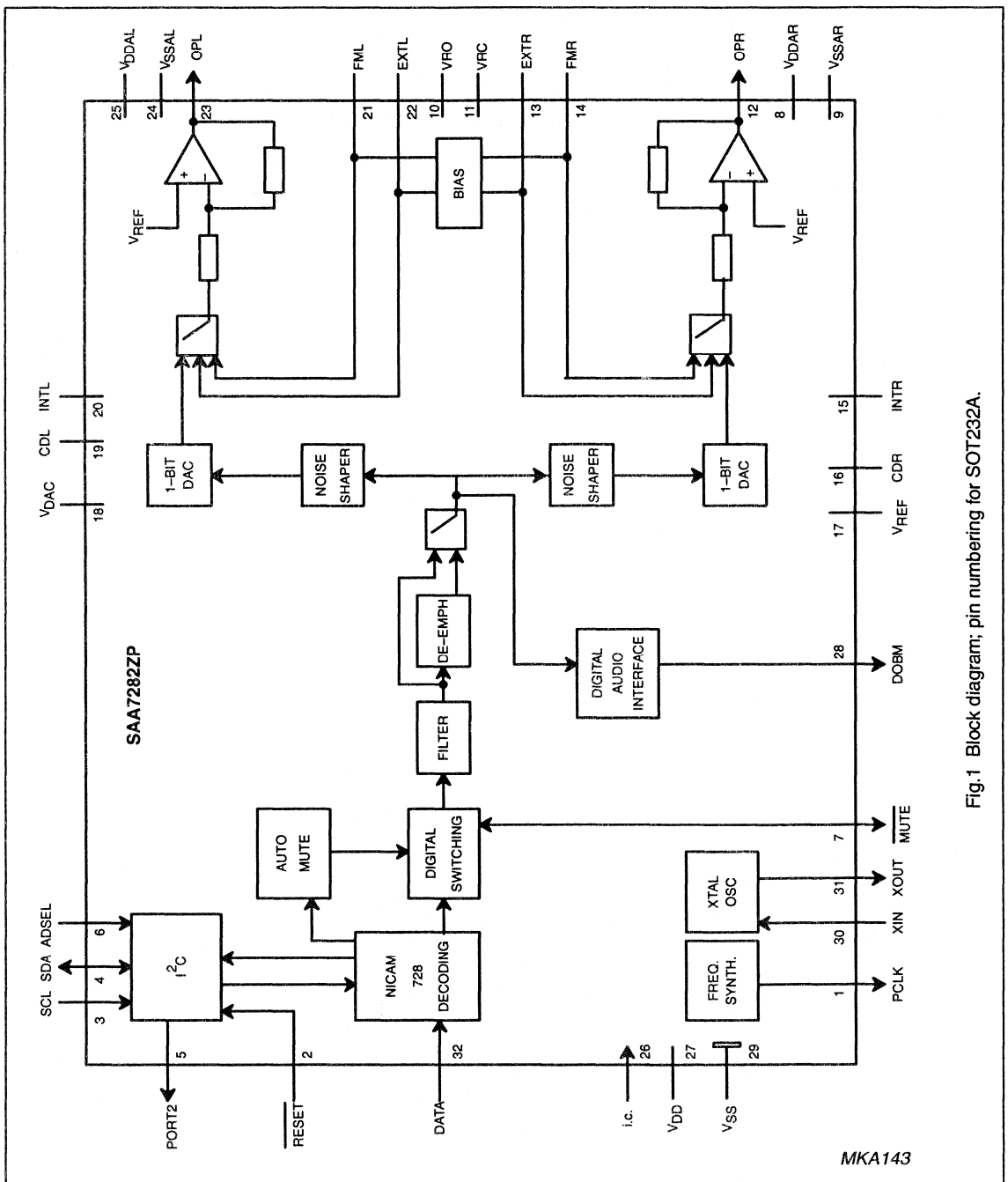


Fig.1 Block diagram; pin numbering for SOT232A.

PINNING

SYMBOL	SOT205AG	SOT232A	DESCRIPTION
DOBM	1	28	digital audio interface output
V_{SS}	2	29	ground connection for the digital section
n.c.	3	–	not connected
XIN	4	30	crystal input at 256fs (8.192 MHz)
XOUT	5	31	crystal output at 256fs (8.192 MHz)
DATA	6	32	serial data input at 728 kbits/s from DQPSK
PCLK	7	1	output clock at 728 kHz to DQPSK demodulator
$\overline{\text{RESET}}$	8	2	active LOW reset. Used to set the device in a valid initial condition
SCL	9	3	clock input for I²C control bus
SDA	10	4	data port for I²C control bus, input/open drain output
PORT2	11	5	output mirroring the I²C control register bit PORT2
n.c.	12	–	not connected
ADSEL	13	6	I²C-bus slave address selection input. Allows selection of one of two separate slave addresses. Defaults to logic 1
$\overline{\text{MUTE}}$	14	7	active LOW mute input. This pin, when set LOW, sets the digital data to zero and either silences the output or switches it to analog FM, depending on the status of MUTEDEF (control bit in the I²C register) and RSSF. Overriden by automute (if automute is used, then $\overline{\text{MUTE}}$ is automatically pulled LOW
n.c.	15 to 17	–	not connected
V_{DDAR}	18	8	analog supply voltage for the right audio channel
V_{SSAR}	19	9	analog ground connection for the right audio channel
VRO	20	10	internal reference voltage buffer output
VRC	21	11	internal reference voltage buffer HIGH impedance node
n.c.	22	–	not connected
OPR	23	12	analog output from the right audio channel
EXTR	24	13	external analog input to the right audio channel
FMR	25	14	FM sound input to the right audio channel
INTR	26	15	integrator output from the right audio channel
CDR	27	16	integrator connection to an external damping capacitor
n.c.	28	–	not connected
V_{REF}	29	17	reference voltage input; 2.5 V (typ.)
V_{DAC}	30	18	quiet V_{SS} to DACs
CDL	31	19	integrator connection to an external damping capacitor
INTL	32	20	integrator output from the left audio channel
FML	33	21	FM sound input to the left audio channel

PINNING

SYMBOL	SOT205AG	SOT232A	DESCRIPTION
EXTL	34	22	external analog input to the left audio channel
OPL	35	23	analog output from the left audio channel
n.c.	36	–	not connected
V_{SSAL}	37	24	analog ground connection for the left audio channel
V_{DDAL}	38	25	analog supply voltage for the left audio channel
n.c.	39 to 41	–	not connected
i.c.	42	26	internally connected. Must be left open-circuit in application
n.c.	43	–	not connected
V_{DD}	44	27	digital supply voltage

PIN CONFIGURATION

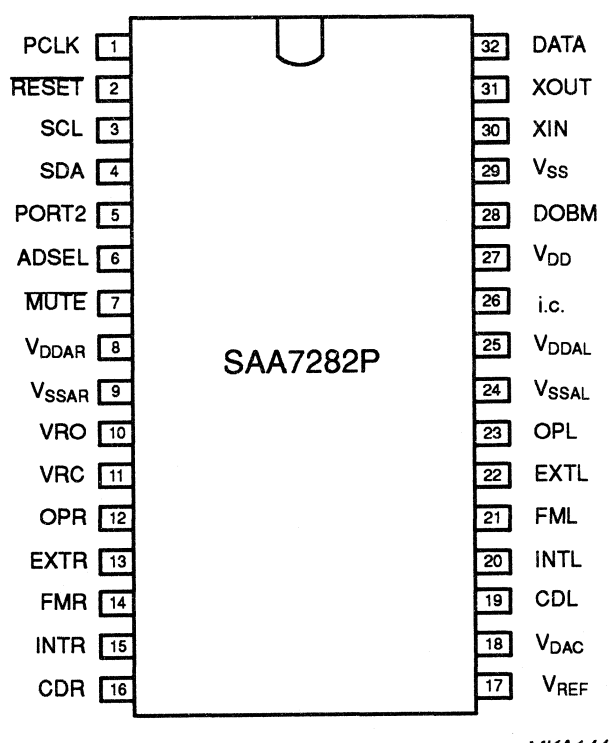


Fig.2 Pin configuration (SOT232A).

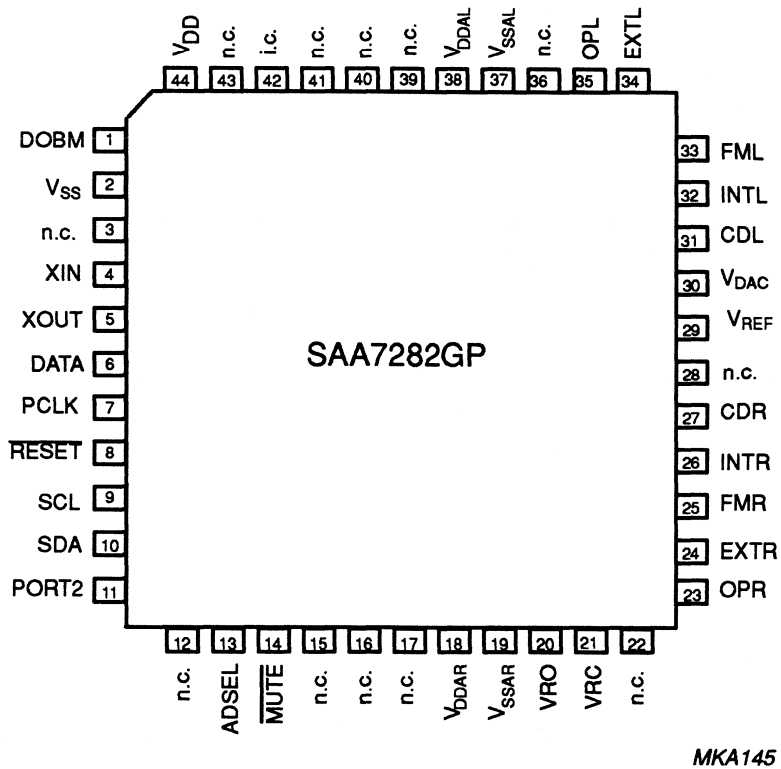


Fig.3 Pin configuration (SOT205AG).

I²C-BUS FORMATS

The SAA7282 contains an I²C-bus slave transceiver permitting a master device to:

- Read decoder status information derived from the transmitted digital audio signal
- Read an error count byte to determine the bit error rate for user mute purposes and to indicate quality of NICAM signal
- Read additional transmitted data bits. Their purpose has yet to be defined but accessibility is provided to allow future services to be implemented in receiver software
- Write control codes to select the available analog switching configurations
- Write upper and lower error count limits for automatic muting function

The device slave address is A(7:1)(R/$\overline{W}$) = 101101X(R/$\overline{W}$). An ADSEL pin is provided to allow selection of one of two different slave addresses via programmable address bit A0.

The SAA7282 does not acknowledge the I²C-bus general call address.

The slave receiver format is:

S SLAVE_ADDR.0 ACK SUB_ADDR ACK DATA BYTE ACK P

<–n bytes–>

Where S = start, A = acknowledge, P = stop.

Auto-increment of the sub-address is provided with wrap-around from 02 (HEX) to 00 (HEX).

The slave receiver data byte format, as a function of sub-address, is as shown in Table 1.

Table 1 Slave receiver data byte

SUB ADDRESS	RESET VALUE HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	90	M1/$\overline{M2}$	DMSEL	SSWIT3	SSWIT2	SSWIT1	PORT2	MUTEDEF	AMDIS
01	50	EMAX7	EMAX6	EMAX5	EMAX4	EMAX3	EMAX2	EMAX1	EMAX0
10	14	EMIN7	EMIN6	EMIN5	EMIN4	EMIN3	EMIN2	EMIN1	EMIN0

M1/M2

This bit selects either M1 (M1/$\overline{M2}$ = 1) or M2 (M1/$\overline{M2}$ = 0) when the input transmission consists of two independent mono signals. Power on resets to 1.

DMSEL

DMSEL is the dual mono selection bit. When asserted it selects M1 and M2 as the output signals if the incoming transmission consists of two independent mono signals (see Table 2). Power on resets to 0.

PORT2

PORT2 controls a bit out, providing direct access to a dedicated output pin (PORT2) via the I²C-bus. See Table 3.

SSWIT3/2/1

These bits control the analog switching, selecting between the FM, external, and NICAM signals. With the NICAM source the signals select whether the de-emphasis is performed and what gain is applied after the filtering and de-emphasis stage. The signal states and their meaning are listed in Table 4. Power on resets to 02 HEX.

AMDIS

This bit enables and disables the automute function (which is activated according to the error limit registers). Power on resets to enabled. AMDIS should be disabled for the user definable mute ($\overline{MUTE}$) to be used.

MUTEDEF

This defines the operation of the user definable $\overline{\text{MUTE}}$ pin when it is pulled LOW externally. If MUTEDEF is HIGH and RSSF = logic 1, the output of the device is switched to FM input. If MUTEDEF is HIGH and RSSF = logic 0, or if MUTEDEF is LOW, the output is muted. Power on resets to LOW.

ERROR LIMIT REGISTERS

UPPER ERROR LIMIT REGISTER

This defines the number of errors in 128 ms period which will cause automute to switch IN. User definable, but power on resets to 50 Hex.

LOWER ERROR LIMIT REGISTER

This defines the number of errors in 128 ms period which will cause automute to switch OUT. User definable, but power on resets to 14 Hex.

Table 2 DMSEL as a function of M1/$\overline{\text{M2}}$

DMSEL	M1/$\overline{\text{M2}}$	FUNCTION
0	0	selects DIGITAL; L = M2, R = M2
0	1	selects DIGITAL; L = M1, R = M1
1	0	selects DIGITAL; L = M2, R = M1
1	1	selects DIGITAL; L = M1, R = M2

Table 3 Port 2 Control

PORT2	OUTPUT STATE
0	LOW
1	HIGH

Table 4 SSWIT signal states and function

SSWIT3	SSWIT2	SSWIT1	FUNCTION
0	0	0	NICAM source de-emphasis switched out, no gain
0	0	1	NICAM source de-emphasis switched in, no gain
0	1	0	NICAM source de-emphasis switched in, +6 dB gain. Power-on reset state
0	1	1	NICAM source de-emphasis switched in, +12 dB gain
1	x	0	external inputs switched in, no change to previous de-emphasis/scaling setting
1	x	1	FM inputs switched in, no change to previous de-emphasis/scaling setting

Note to Table 4

Where x = don't care.

Slave Transmitter

The slave transmitter formats are illustrated thus:

- S SLAVE_ADDR.1 A STATUS_BYTE NA P

  In this format the bus master reads the STATUS_BYTE once.
- S SLAVE_ADDR.1 A STATUS_BYTE A ERROR_BYTE NA P

  In this format the bus master reads two bytes of STATUS_BYTE and ERROR_BYTE.
- S SLAVE_ADDR.1 A STATUS_BYTE A ERROR_BYTE A AD_BYTE_0 A AD_BYTE_1 NA P

  In this format the bus master reads four bytes of STATUS_BYTE, ERROR BYTE and two additional bytes, AD_BYTE_0 and AD_BYTE_1. The additional data bytes contain the eleven additional data bits AD0 to AD10 together with information regarding their status.

Table 5 Data byte formats

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
STATUS_BYTE	PONRES	S/$\overline{M}$	D/$\overline{S}$	VDSP	RSSF	$\overline{OS}$	AM	$\overline{CFC}$
ERROR_BYTE	E7	E6	E5	E4	E3	E2	E1	E0
AD_BYTE_0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
AD_BYTE_1	OVW	SAD		CI2	CI1	AD10	AD9	AD8

The bits may be defined as follows:-

PONRES

This bit is a power-on reset detection bit. It is set HIGH after a power-on reset or supply reduction and is cleared LOW when the STATUS_BYTE is read.

S/$\overline{M}$ (stereo/mono indication)

S/$\overline{M}$ = 1 indicating an incoming stereo transmission
S/$\overline{M}$ = 0 indicating that the incoming transmission is not stereo.

D/$\overline{S}$ (dual/single mono indication)

D/$\overline{S}$ = 1 indicating an incoming dual mono transmission
D/$\overline{S}$ = 0 indicating that the incoming transmission is not dual mono.

VDSP

This bit indicates that the decoded signal is valid digital sound. When VDSP = logic 0 the incoming transmission carries either a 704 kbit/s transparent data channel or a currently undefined format and the device automatically switches to FM regardless of RSSF.

RSSF

RSSF is the reserve sound switching flag indication equal to the C4 bit in the NICAM transmission. RSSF = logic 1 when the FM sound signal is carrying the same programme material as the digitally modulated carrier (specifically the M1 signal in the event of a dual mono transmission). RSSF = logic 0 when the FM signal is not reproduced within the digital signal.

$\overline{OS}$

This bit provides an active LOW indication that the decoder is out of sync. If $\overline{OS}$ = logic 1 the decoder is frame synchronized and has obtained C0 (16 frame) sync. If $\overline{OS}$ = logic 0, the decoder is out of sync and the indicator bits are as given in Table 6.

Table 6 Indicator bits functional truth table

TRANSMISSION	C1	C2	C3	S/$\overline{M}$	D/$\overline{S}$	VDSP	$\overline{OS}$
STEREO	0	0	0	1	0	1	1
M1 + M2	0	1	0	0	1	1	1
M1 + DATA	1	0	0	0	0	1	1
TRANS. DATA	1	1	0	0	0	0	1
ANY CURRENTLY UNDEFINED COMBINATION OF C1, C2, C3				0	0	0	1
DECODER UNSYNCHRONIZED ($\overline{OS}$ = 0)				0	0	0	0

AM

This bit indicates when the automuting function has switched from the NICAM sound to the conventional FM sound. This enables the software controller to display the relevant information to the customer, for example, on screen display. If AM bit = logic 0 no switching has been carried out by the automuting function. If AM bit = logic 1 then the automuting function has switched to the FM inputs.

M1/$\overline{M2}$

This bit in conjunction with DMSEL bit, determines the output configuration in dual mono mode (see Table 2). Power on resets to 1.

DMSEL

This bit determines whether one or both of the dual mono signals are output (see Table 2). Power on resets to 0.

$\overline{CFC}$

Signals a change of configuration at the 16-frame boundary. It is cleared to logic 1 by the I²C-bus reading the status register.

E7 to E0

This is an error count byte which counts the number of error flags in a 128 ms period. The register is updated every 128 ms.

AD10 to AD0

These are the additional data bits from the transmission and are updated every 1 ms. This provides a data capacity of 11 kbit/s.

SAD

SAD is the 'status additional data' bit. This is set to logic 1 when new bits AD10 to AD0 are latched into the I²C-bus registers. It is automatically reset to logic 0 when AD_BYTE_1 is read by the bus master.

OVW

OVW is the overwrite indicator for the additional data. This bit is set when the transmission overwrites additional data bits which have not been read by the bus master. This bit is automatically reset to logic 0 when AD_BYTE_1 is read by the bus master.

CI1 to CI2

These represent the CIB bits which are extracted by a majority logic process from the parity checks of the last ten samples in a frame (samples 55 to 64). CI1 will be conveyed by the parity grouping of samples 55 to 59 and CI2 will be conducted by the parity grouping of samples 60 to 64. Both parity groups will be even for UK transmissions such that CI2 = logic 0 and CI1 = logic 0. The transmissions of countries following the specification issued by the EBU (Document SPB424; Digital sound transmissions in terrestrial television) will allow odd or even parity groups, thus providing an additional 2 kbit/s data capacity.

DIGITAL AUDIO INTERFACE IEC/EBU 958

Block structure

The output is grouped into a block of 192 consecutive frames providing, for each channel the 192 channel status data bits. The start of a block is designated by a special sub-frame preamble.

Sub-frame structure

Each frame is divided into 32 time-slots numbered 0 to 31.

Time-slots 0 to 3 carry one of three permitted preambles These are used to affect synchronization of sub-frames, frames and blocks.

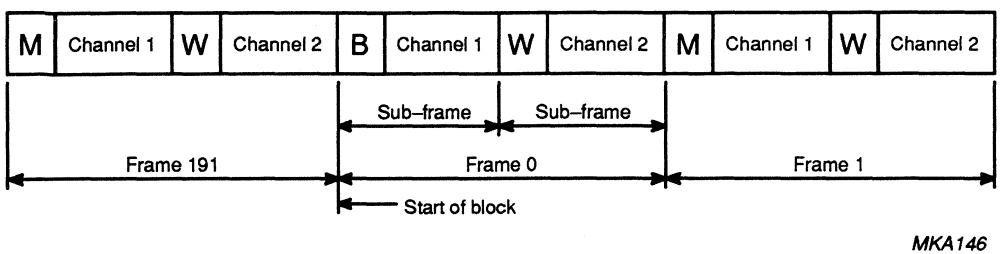


Fig.4 Frame format.

Frame structure

Each frame is uniquely composed of two sub-frames. The rate of transmission of frames corresponds exactly to the source sampling frequency. In the 2-channel operation, samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. Sub-frames related to Channel 1 (left or 'A' channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However the preamble is changed to preamble B once every 192 frames. This defines the block structure used to organize the channel status information. Sub-frames of Channel 2 (right or 'B' channel in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

Time-slots 4 to 27 carry the audio sample word in linear two's complement representation. The most significant bit is carried by time-slot 27.

Time-slot 28 carries the validity flag associated with the audio sample word. This flag is set to logic 0 if the audio sample is reliable. If set to logic 1 then the sample is unreliable.

Time-slot 29 carries one bit of the user data channel. In this application this is not used and so is set to logic 0.

Time-slot 30 carries one bit of the channel status word associated with the audio channel transmitted in the same sub-frame.

Time-slot 31 carries a parity bit such that time-slots 4 to 31 inclusive will carry an even number of ones and an even number of zeros.

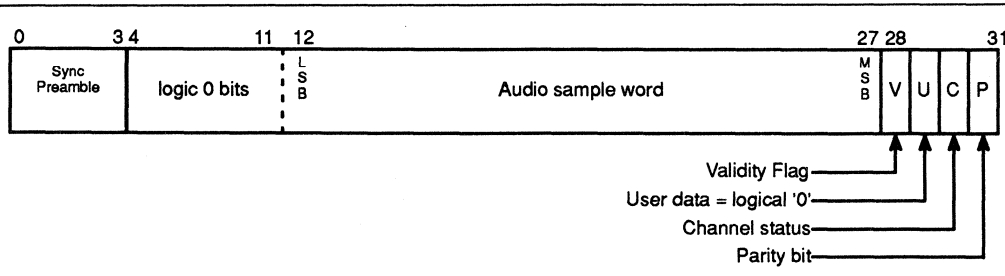


Fig.5 Sub-frame format.

Channel coding

Time-slots are encoded as bi-phase mark data. Each bit transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit being transmitted is logic 0, however it is different if the bit is logic 1.

Table 7 Channel coding

Preceding state	0	1
Transmitted bit	Channel coding	
0	11	00
1	10	01

Preambles

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.
A set of three preambles is used. These preambles are transmitted in the time allocated to four time-slots and are represented by eight succesive states. The first state of the preamble is always different from the second state of the previous symbol. Depending on this state the preambles are as shown in Table 8.

Table 8 Preambles

Preceding state	0	1
Preamble	Channel coding	
B	11101000	00010111
M	11100010	00011101
W	11100100	00011011

The preambles preceding each digital audio sample are used to indicate the beginning of a sample as follows:

- **Preamble B** indicates the start of Channel A data and the beginning of a block
- **Preamble M** indicates the start of Channel A data but not the beginning of a block
- **Preamble W** indicates the start of Channel B data

Channel status

The channel status information is organized in 192-bit words. The first bit of each word is carried in the frame with preamble B. The 192-bit word is organized into sections as shown in Table 9.

Table 9 Channel status codes

BIT	CODE	DESCRIPTION
0	0	consumer
1	0	sound data
2	1	digital copy permitted
3, 4	00	indicates digital de-emphasis switched in
	11	indicates digital de-emphasis switched out
5	0	
6, 7	00	
8 to 15	00110001	category code
16 to 19	0000	source code (don't care)
20 to 23	0000	channel number (don't care)
24 to 27	1100	sampling frequency (32 kHz)
28, 29	00	clock accuracy (level II)
30 to 191	all 0s	

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	note 1	−0.5	+6.5	V
$V_{I(max)}$	maximum input voltage (any input)		−0.5	V_{DD}+0.5	V
$V_{O(max)}$	maximum output voltage		−0.3	V_{DD}+0.5	V
I_{IOK}	DC input or output diode current		–	±20	mA
$I_{O(max)}$	output current (each output)		–	±10	mA
T_{amb}	ambient operating temperature range		0	+70	°C
T_{stg}	storage temperature range		−55	+125	°C
V_{stat}	electrostatic handling	note 2	−2000	+2000	V

Notes to the Limiting values

1 All V_{DD} and V_{SS} connections must be made externally to the same power supply.

2. Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to +70 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage	see Fig.9	4.5	5.0	5.5	V
I_{DD}	total supply current		–	50	–	mA
V_{SS}, V_{SSAL}, V_{SSAR}, V_{DAC}	ground supply voltage		0	–	0	V
V_{DDAL}, V_{DDAR}	analog supply voltage	see Fig.9	4.5	5.0	5.5	V
Digital inputs						
DATA						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
I_{LI}	input leakage current		−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
ADSEL (THIS PIN IS INTERNALLY PULLED HIGH WHEN NOT CONNECTED)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
Z_I	input impedance		–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
$\overline{\text{RESET}}$ (SCHMITT TRIGGER INPUT)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
V_{hys}	hysteresis		$0.05V_{DD}$	–	–	V
SCL						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
V_{hys}	hysteresis		$0.05V_{DD}$	–	–	V
I_{LI}	input leakage current		−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
Digital input/output						
SDA						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
V_{hys}	hysteresis		$0.05V_{DD}$	–	–	V
I_{LI}	input leakage current		−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_L	load capacitance					
	active pull-up		–	–	400	pF
	passive pull-up		–	–	200	pF
MUTE I/O (THIS PIN HAS AN INTERNAL PULL-UP)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 2.8 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage		2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
Z_I	input impedance		–	50	–	kΩ
Digital outputs						
PORT2, PCLK, DOBM						
V_{OL}	LOW level output voltage	I_{OL} = 2.8 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = 800 µA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
Crystal oscillator						
f_c	crystal frequency		–	8.192	–	MHz
gm	mutual conductance	at 100 kHz	1.5	-	–	mA/V
Av	small signal gain	Av = gm.Ro	3.5	–	-	V/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		-	–	5	pF
C_O	output capacitance		-	–	10	pF
Crystal oscillator						
XIN						
V_{IL}	LOW level input voltage		0	–	–	V
V_{IH}	HIGH level input voltage		–	–	V_{DD}	V
I_{LI}	input leakage current		–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
Digital filter specification						
f_s	output sample frequency		–	128	–	kHz
PR	pass band ripple	at 0 Hz to 15 kHz	–	–	±0.01	dB
SBA	stop band attenuation	at f ≥17 kHz	30	–	–	dB
Digital de-emphasis						
DEV	deviation from ideal		–	–	±0.09	dB
ANALOG SECTION (measured at V_{DD} = 5 V and T_{amb} = 25 °C)						
Reference voltage buffer						
VRC OUTPUT						

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{rc}	voltage reference at VRC	see Fig.10	–	$0.5V_{DD}$	–	V
DACs						
V_{REF} INPUT						
V_{ref}	reference input voltage		–	$0.5V_{DD}$	–	V
Switching operational amplifiers						
C_L	output load capacitance		–	–	300	pF
R_L	output load resistance		3	–	–	kΩ
Z_O	output impedance		–	150	–	Ω
G	output gain		–	0	–	dB
CHM	channel matching	0 dB, 1 kΩ	–	0	–	dB
PSSR	powewr supply rejection ratio		–	40	–	dB
EXTERNAL INPUTS SELECTED (FML, FMR, EXTL, EXTR)						
V_{ain}	input voltage level (RMS value)		–	–	1.1	V
S/N	signal-to-noise ratio (relative to 1 V RMS, unity gain)	FM or EXT	90	100	–	dB
THD	total harmonic distortion (unity gain, O/P = 1 V RMS)	FM or EXT	–	–90	–70	dB
NICAM INPUTS SELECTED (INTL, INTR)						
V_{ain}	input voltage level (RMS value)	at 0 dB; V_{REF} = 2.5 V	–	1.0	–	V
THD+N	total harmonic distortion plus noise	NICAM 728; notes 2 and 3	–	–80	–	dB
DIGS	digital silence level	$\overline{\text{MUTE}}$ on	–	–80	–	dB
Timing (all timing values refer to V_{IH} and V_{IL} levels)						
DATA WITH RESPECT TO PCLK (SEE FIG.7)						
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		250	–	–	ns
SDA with repect to SCL (see Fig.8)						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{BUF}	bus free time		1300	–	–	ns
$t_{HD;STA}$	start code hold time		600	–	–	ns
t_{LOW}	SCL clock LOW time		1300	–	–	ns
t_{HIGH}	SCL clock HIGH time		600	–	–	ns
$t_{SU;STA}$	start code set-up time		600	–	–	ns
$t_{HD;DAT}$	data hold time	note 4	0	–	–	ns
$t_{SU;DAT}$	data set-up time	note 5	100	–	–	ns
t_r	SDA and SCL rise time		50	–	300	ns
t_f	SDA and SCL fall time		50	–	300	ns
$t_{SU;STO}$	stop code set-up time		600	–	–	ns
t_{of}	output fall time	note 6	50	–	200	ns

Notes to the characteristics

1. Outputs OPL and OPR are measured with external components as recommened in Fig.11.
2. Total analog performance is limited by dynamic range of the NICAM 728 system. Due to compansion the quantization noise is never lower than approximately –62 dB with respect to the input level.
3. Measured with a –30 dB, 1 kHz NICAM 728 input signal.
4. Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.
5. If a fast I²C-bus device is used in an up to 100 kbit/s I²C-bus system, then the requirement $t_{SU;DAT} \geq 250$ ns is always fulfilled if this device cannot stretch tne LOW level of the SCL signal. If a device stretches the LOW level of the SCL signal, then data to SDA must be asserted ($t_{RD(max)} + t_{SU;DAT}$) = 1000 + 250 = 1250 ns before the SCL signal is released to be compatible with the up to 100 kbit/s I²C-bus specification.
6. The output fall time is measured between 3.0 V and 1.5 V for a bus capacitance of 400 pF and an active pull-up.

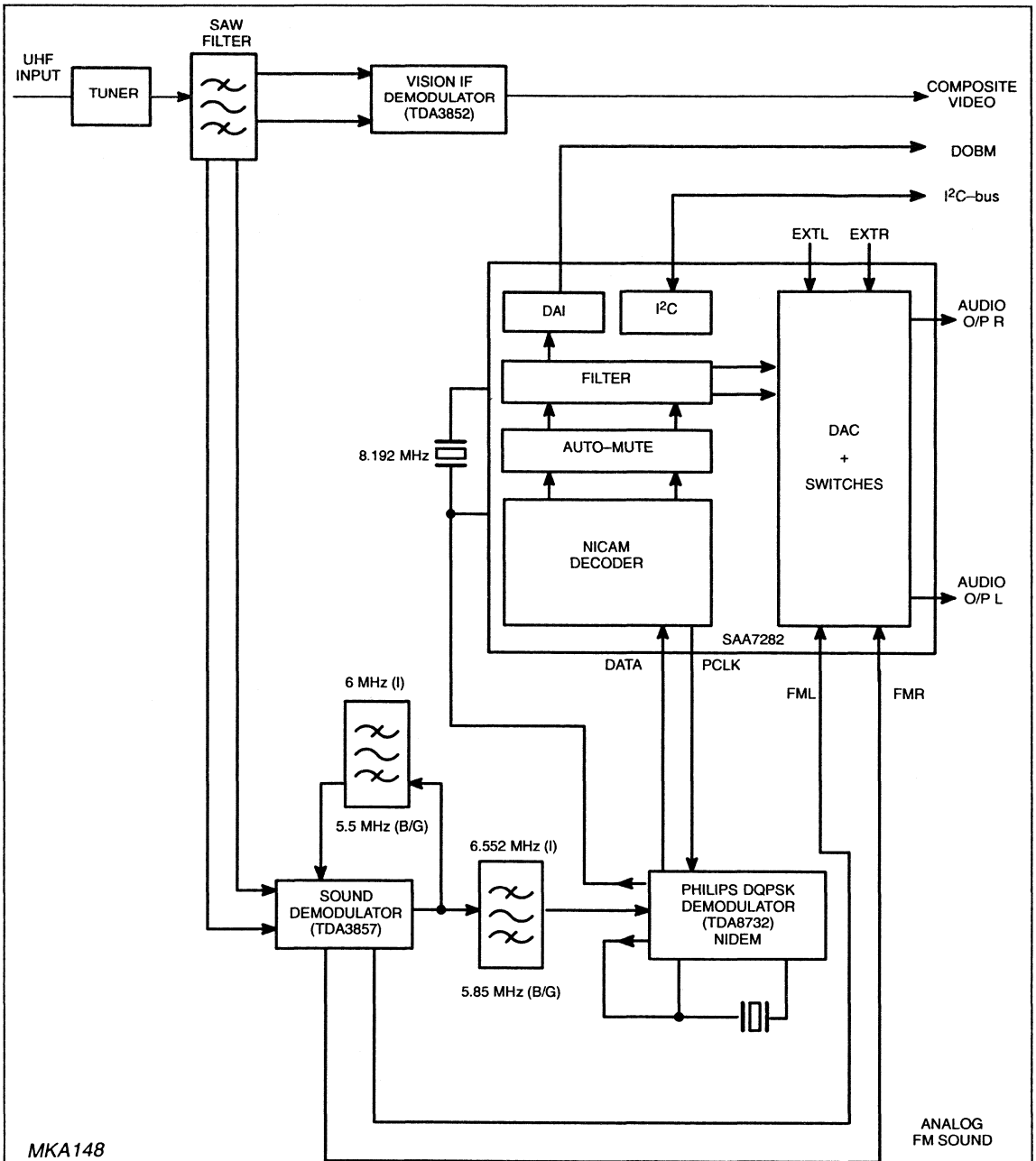


Fig.6 System block diagram showing SAA7282 with TDA8732.

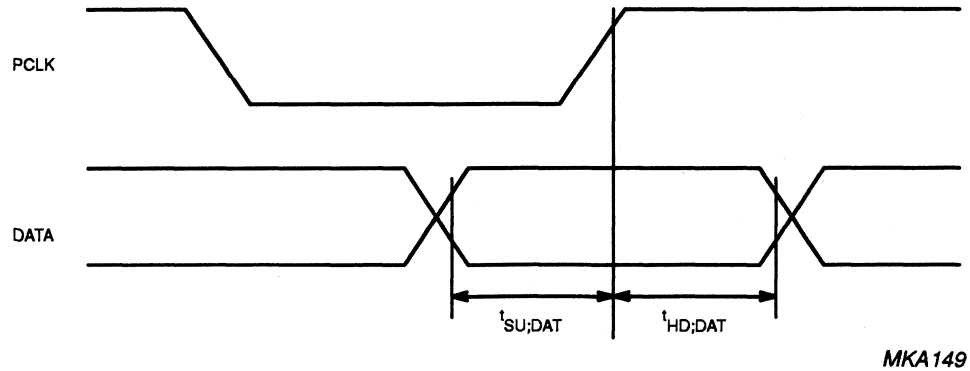


Fig.7 Data output timing.

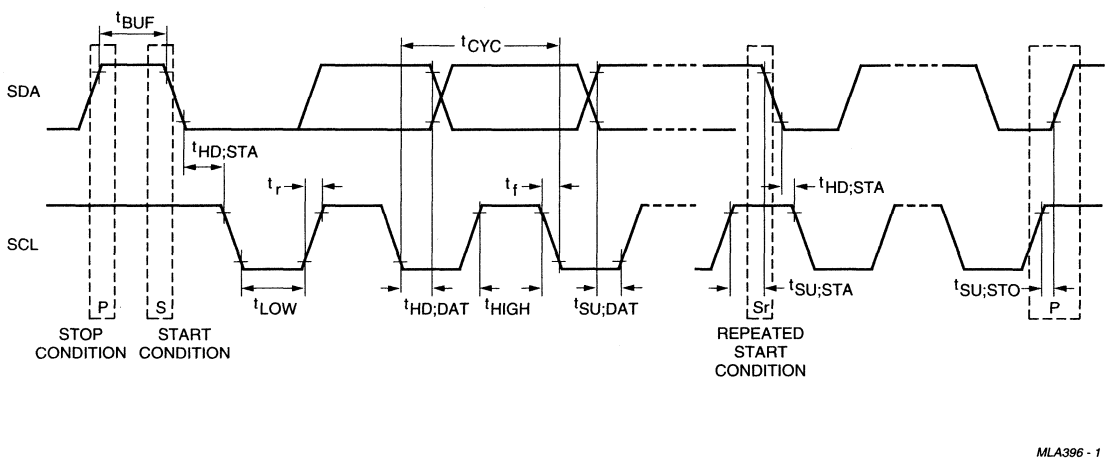


Fig.8 I²C-bus interface timing.

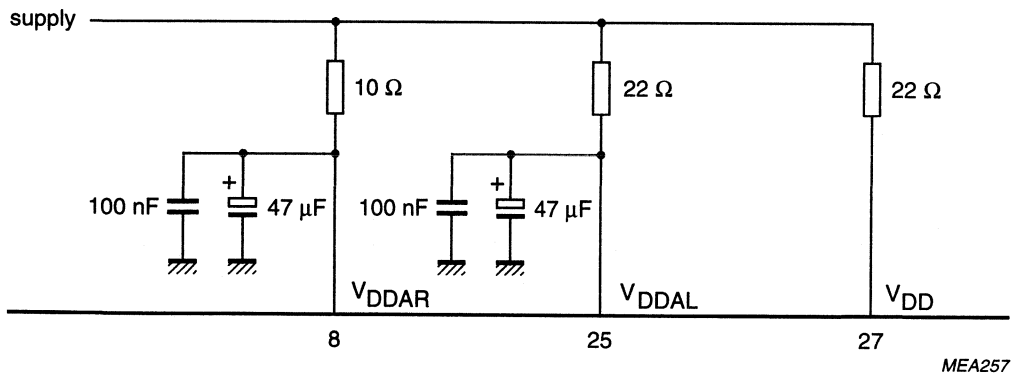


Fig.9 V_{DD} external circuitry (same external circuit values also required for V_{DDAL} and V_{DDAR}).

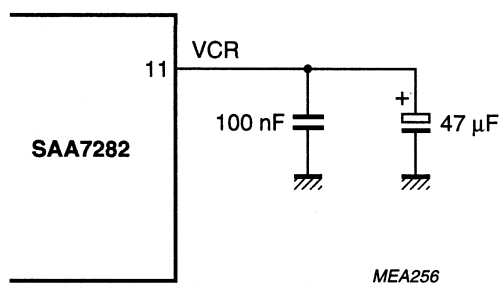


Fig.10 VRC external circuitry (same external circuit values also required for VRO).

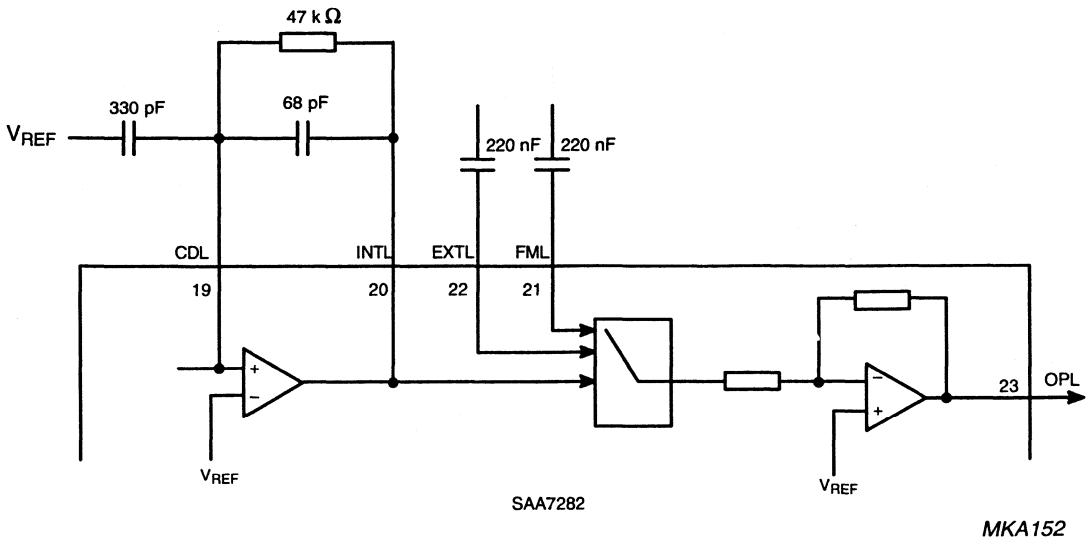


Fig.11 External circuitry for left channel DAC (same external circuit values also required for right channel DAC).

TELETEXT IC FOR ANALOG AND DIGITAL TV

GENERAL DESCRIPTION

The SAA9042 is a CMOS integrated circuit designed for reception, decoding and display of 625 and 525 line World System Teletext (WST).

It is used in conjunction with a teletext video processor (SAA5235/6 or SAA5191) for data regeneration, and a single-chip 64 K x 4-bit or 256 K x 4-bit dynamic RAM page memory.

The SAA9042 acquires teletext packets defined at levels 1, 2 and 3 in the WST specification and produces a level 1 display.

The device is μC controlled via the standard I^{2}C-bus and is compatible with analog, digital and features TV.

Features

General

- Interfaces with the Philips digital TV chip-set
- Interfaces with analog TV
- Directly interfaces up to 1 Mbit dynamic RAM
- Fully independent acquisition and display timing
- 3 display modes
  - normal
  - 32 kHz (progressive scan)
  - 100 Hz/120 Hz (field doubling)
- I^{2}C controlled
- Single 5 V power supply

Acquisition

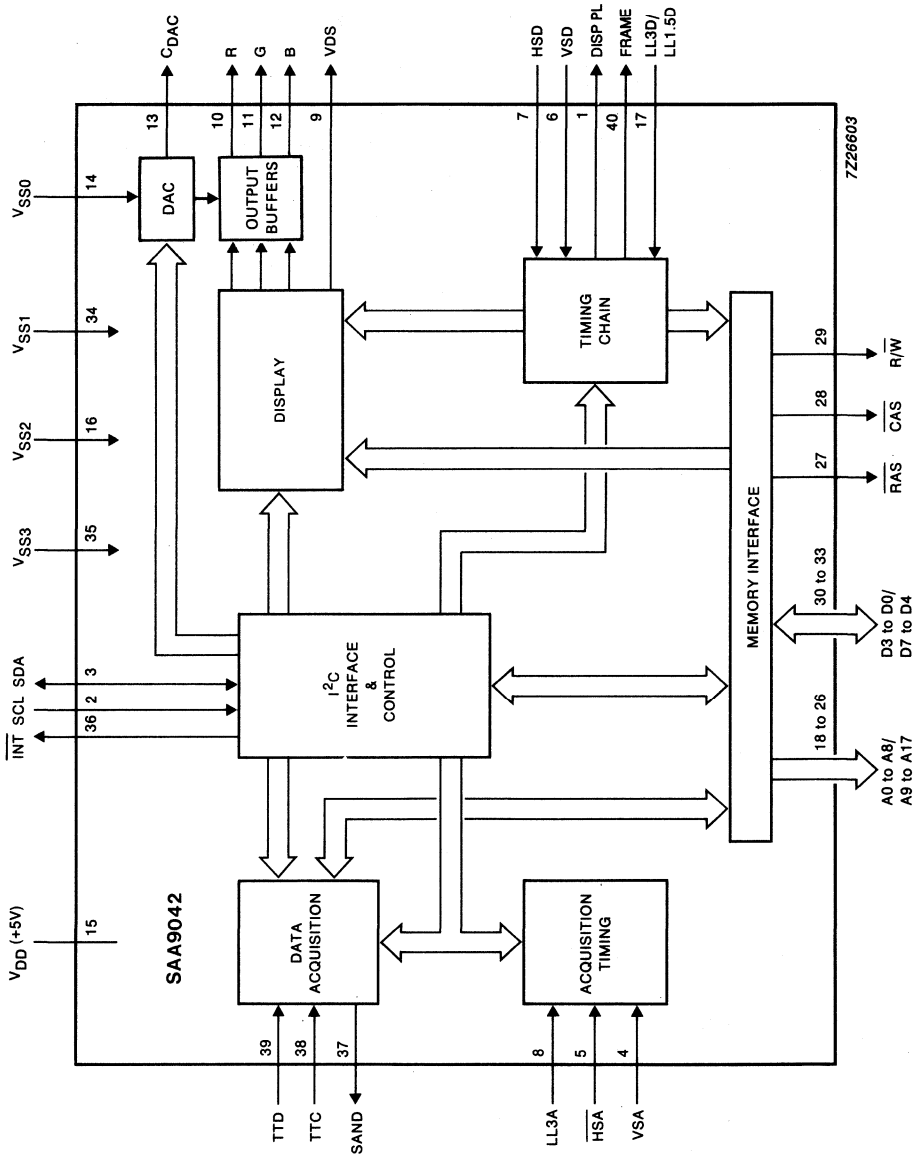
- Simultaneous update of up to 8 pages
- Up to 100 page background memory capability
- Software selectable 625/525 line operation
- Full level One Features (FLOF) operation
- TOP compatible
- VPT compatible
- VBI and full channel operation
- Extension packets 26/27/28/29 and 30 fully decoded

Display

- Stable display by slaving from scan-related timing signals
- Automatic selection of six different languages
- Storage of 192 characters (13 x 10 dot matrix)
- Software controlled RGB level removes the need for hardware adjustment
- Up to 27 display rows; 0 to 24 and up to 2 status rows

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).


SAA9042
DAC
OUTPUT BUFFERS
DISPLAY
TIMING CHAIN
I²C INTERFACE & CONTROL
MEMORY INTERFACE
DATA ACQUISITION
ACQUISITION TIMING
CDAC
R
G
B
VDS
HSD
VSD
DISP PL
FRAME
LL3D/ LL1.5D
VSS0
VSS1
VSS2
VSS3
VDD (+5V)
INT
SCL
SDA
R/W
CAS
RAS
30 to 33
D3 to D0/ D7 to D4
18 to 26
A0 to A8/ A9 to A17
TTD
TTC
SAND
LL3A
HSA
VSA
7Z26603

PINNING

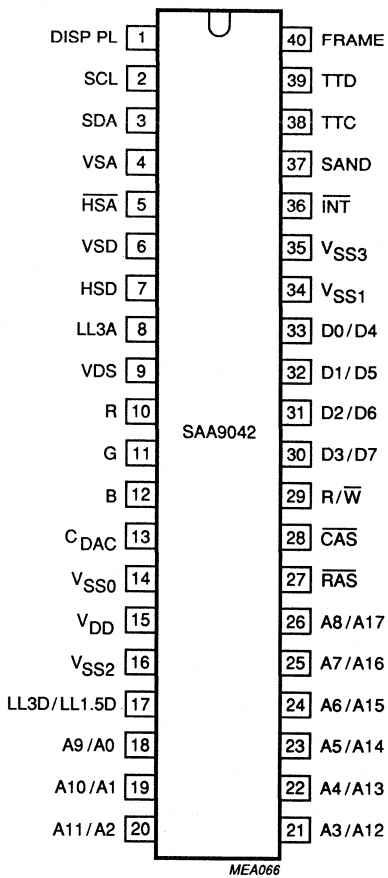


Fig.2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	DISP PL	**Display PL:** a programmable decode from the display-timing chain which can be used as a reference signal in an external PLL in scan-locked applications.
2	SCL	**Serial Clock:** input signal which is the I^2C-bus clock from the microcontroller.
3	SDA	**Serial Data:** is the I^2C-bus data line connected to the microcontroller. It is an input/output function with an open-drain output.
4	VSA	**Vertical Synchronization Acquisition:** vertical synchronization signal from the SAA9051 (VS) or SAA5191 (VCS), derived from the incoming video. This input enables field timing to be established in the acquisition section.
5	$\overline{\text{HSA}}$	**Horizontal Synchronization Acquisition:** horizontal synchronization signal derived from the incoming video e.g. burst gate pulse. This active LOW input enables line timing to be established in the acquisition section.
6	VSD	**Vertical Synchronization Display:** synchronization signal indicating the vertical position of the TV picture. This input allows field synchronization of the display section.
7	HSD	**Horizontal Synchronization Display:** synchronization signal indicating the horizontal position of the TV picture. This input allows line synchronization of the TV picture.
8	LL3A	**Line-Locked system clock:** 13.5 MHz system clock input for the acquisition section.
9	VDS	**Video/Data Switch:** push-pull active HIGH 3-state output which controls the switching between text (HIGH) and normal TV (LOW) picture for both normal text and superimposed displays.
10 11 12	R G B	**Red, Green, Blue:** analog 3-state outputs which contain video character and background information for text display. The output level is adjustable over 16 steps and is controlled by V_{SS0}, V_{DD} and an internal register.
13	C_{DAC}	**DAC output:** DAC output level, requires an external decoupling capacitor not less than 1 μF.
14	V_{SS0}	**Ground:** ground connection for video outputs.
15	V_{DD}	**Power Supply:** + 5 V (typ.).
16	V_{SS2}	**Ground:** ground connection.
17	LL3D/ LL1.5D	**Line-Locked system clock:** 13.5 MHz or 27 MHz system clock input for the display, memory interface and control sections.
18 to 26	A0 to A8/ A9 to A17	**Address:** multiplexed address outputs for the external nibble-wide dynamic RAM (DRAM). With a 64-Kbit (16 K x 4) DRAM the address A8 pin is not used.
27	$\overline{\text{RAS}}$	**Row Address Strobe:** active LOW output for the external DRAM.
28	$\overline{\text{CAS}}$	**Column Address Strobe:** active LOW output for the external DRAM.
29	R/$\overline{\text{W}}$	**Read/Write:** active LOW write enable signal for the external DRAM.

pin no.	mnemonic	description
30 to 33	D3 to D0/ D4 to D7	**Data:** data inputs/outputs to and from the external nibble-wide DRAM.
34	V_{SS1}	**Ground:** ground connection.
35	V_{SS3}	**Ground:** ground connection.
36	$\overline{INT}$	**Interrupt:** open-drain active LOW output which provides an interrupt signal for a microprocessor indicating the arrival of a page or packet in any one of the acquisition channels, change in newsflash/subtitle status or power-on reset.
37	SAND	**Sandcastle:** 3-level output for the SAA5191 or SAA5236 representing the PL/$\overline{CBB}$ signal, derived from the acquisition timing chain.
38	TTC	**Teletext Clock:** input from the SAA5191 or SAA5236 supplied via an external coupling capacitor.
39	TTD	**Teletext Data:** input from the SAA5191 or SAA5236 supplied via an external coupling capacitor, internally clamped to V_{SS} for 4 to 8 μs of each line to maintain the correct DC level.
40	FRAME	**Frame:** output for de-interlacing ciruits. The signal is LOW for even fields and HIGH for odd fields when text but no picture is displayed. It is forced LOW when a TV picture is present.

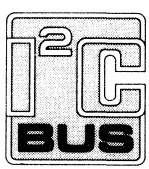
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.5	+ 6.5	V
DC input voltage	V_I	−0.5	V_{DD} + 0.5	V
DC input current	I_I	−20	+ 20	mA
DC output voltage	V_O	−0.5	V_{DD} + 0.5	V
DC output current	I_O	−20	+ 20	mA
DC V_{DD} current	I_{DD}	*	*	mA
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Electrostatic handling**	V_{es}	−1000	+ 1000	V

Notes to the ratings

1. All voltages are with respect to V_{SS}.
2. V_{SSO} is considered as an output.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Value to be fixed.

** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	note 1	V_{DD}	4.5	5.0	5.5	V
Supply current		I_{DD}	–	100	–	mA
Inputs	note 2					
TTD	note 3					
Input voltage						
(peak-to-peak value)		$V_{I(p-p)}$	2.0	–	5.0	V
External coupling capacitor		C_{ext}	–	22	50	nF
Input rise and fall times	notes 4 and 26	t_r, t_f	10	–	80	ns
Input data set-up time	note 5	$t_{SU;DAT}$	40	–	–	ns
Input data hold time	note 5	$t_{HD;DAT}$	40	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	7	–	pF
Clamp start time	note 6	t_{CLon}	3.5	4.0	4.5	μs
Clamp finish time	note 6	t_{CLoff}	7.5	8.0	8.5	μs
Clamp output current	note 7	I_{clamp}	1.0	–	–	mA
TTC	note 8					
Input voltage						
(peak-to-peak value)		$V_{I(p-p)}$	2.0	–	5.0	V
External coupling capacitor		C_{ext}	–	10	10	nF
Peak input current		I_{IM}	−10	–	+ 10	mA
Input peaks relative to 50% duty factor		$\pm V_{IM}$	0.2	–	3.5	V
Input rise and fall times	notes 4 and 26	t_r, t_f	10	–	80	ns
Input capacitance	note 26	C_I	–	7	–	pF
Input clamp voltage		V_{clamp}	1.2	1.4	1.6	V
Clock frequency						
625 line		f_{TTC}	–	6.9375	–	MHz
525 line		f_{TTC}	–	5.7272	–	MHz

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (continued)	note 2					
$\overline{HSA}$	note 9					
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
VSA						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH	note 27	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
LL3A (TTL mode)						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
LL3A cycle time	note 10	t_{CA}	69	74	80	ns
LL3A HIGH time		t_{CAH}	28	–	–	ns
LL3A LOW time		t_{CAL}	28	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−100	–	+ 100	μA
Input capacitance	note 26	C_I	–	–	10	pF
LL3A (AC mode)	13.5 MHz					
Mean voltage level	notes 25 and 26	V_{ACM}	−12	–	+ 12	V
AC voltage (peak-to-peak value)		$V_{AC(p-p)}$	1.0	–	3.0	V
Voltage HIGH w.r.t. mean		V_{ACH}	0.3	–	2.0	V
Voltage LOW w.r.t. mean		V_{ACL}	−2.0	–	−0.3	V
Input mark/space ratio w.r.t. mean t_{ACH}: t_{ACL} or t_{ACL} : t_{ACH}	note 28		30 : 70	–	70 : 30	
Series capacitor		C_S	47	100	220	pF
Input impedance	notes 24 and 26	Z_{ACI}	10	–	–	kΩ
SCL						
Input voltage LOW		V_{IL}	0	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD}	V
Input rise time	notes 4 and 26	t_r	–	–	1	μs
Input fall time	notes 11 and 26	t_f	–	–	300	ns
Input leakage current	note 12; V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance	note 26	C_I	–	–	7	pF
HSD						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	50	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
VSD						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
LL3D (TTL mode)						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	10	ns
LL3D cycle time						
13.5 MHz		t_{CA}	69	74	80	ns
27.0 MHz		t_{CA}	35	37	40	ns
LL3D HIGH time						
13.5 MHz		t_{CAH}	28	–	–	ns
27.0 MHz		t_{CAH}	14	–	–	ns
LL3D LOW time						
13.5 MHz		t_{CAL}	28	–	–	ns
27.0 MHz		t_{CAL}	14	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−100	–	+ 100	μA
Input capacitance	note 26	C_I	–	–	10	pF
LL3D (AC mode)						
Mean voltage level	notes 25 and 26	V_{ACM}	−12	–	+ 12	V
AC voltage (peak-to-peak value)		$V_{AC(p-p)}$	1.0	–	3.0	V
Voltage HIGH w.r.t. mean		V_{ACH}	0.3	–	2.0	V
Voltage LOW w.r.t. mean		V_{ACL}	−2.0	–	−0.3	V
Input mark/space ratio w.r.t. mean t_{ACH}: t_{ACL} or t_{ACL} : t_{ACH}	note 28		30 : 70	–	70 : 30	
Series capacitor		C_S	47	100	220	pF
Input impedance	notes 24 and 26	Z_{ACI}	10	–	–	kΩ
Inputs/Outputs (I/O)	note 13					
SDA (open drain I/O)						
Input voltage LOW		V_{IL}	0	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD}	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
SDA (open drain I/O) (continued)						
Input rise time	notes 4 and 26	t_r	–	–	1	μs
Input fall time	notes 11 and 26	t_f	–	–	300	ns
Input leakage current	note 12; V_I = 0 to V_{DD}; (with output off)	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	0	–	0.4	V
Output fall time	notes 11 and 26	t_f	–	–	300	ns
Load capacitance		C_L	–	–	400	pF
D3 to D0						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input leakage current	note 12; V_I = 0 to V_{DD}; (with output off)	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V	note 26	t_r, t_f	–	–	10	ns
Load capacitance	note 21	C_L	–	–	100	pF
Outputs	note 13					
SAND	note 22					
Output voltage LOW	I_{OL} = 0.2 mA	V_{OL}	0	–	0.3	V
Output voltage INTERMEDIATE	$\pm I_{OI}$ = 30 μA	V_{OI}	1.3	–	2.7	V
Output voltage HIGH	I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 1.1 V	note 26	t_r, t_f	–	–	400	ns
Output rise time V_{OL} to V_{OH} between 2.9 V and 4.0 V	note 26	t_r, t_f	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 4.0 V and 0.4 V	note 26	t_r, t_f	–	–	50	ns
Load capacitance		C_L	–	–	30	pF

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{INT}$ (open-drain output)						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output leakage current	output off; V_{PU} = 0 to V_{DD}	I_{LO}	−10	–	+ 10	μA
Output fall time	notes 15 and 26	t_f	–	–	50	ns
Load capacitance		C_L	–	–	100	pF
A0 to A8						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V	note 26	t_r, t_f	–	–	10	ns
Load capacitance	note 23	C_L	–	–	100	pF
$\overline{RAS}$, $\overline{CAS}$, R/$\overline{W}$						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V	note 26	t_r, t_f	–	–	10	ns
Load capacitance	note 23	C_L	–	–	100	pF
DISP PL, FRAME						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times	notes 16 and 26	t_r, t_f	–	–	200	ns
Load capacitance		C_L	–	–	200	pF
R, G, B (3-state)	note 29					
Output voltage LOW	note 17; I_{OL} = 2.0 mA	V_{OL}	V_{SS0}	–	V_{SS0}+0.2	V
Output voltage HIGH	note 18; I_{OH} = −2 mA	V_{OH}	–	*	–	V
Output rise and fall times between 0.6 V and 1.8 V	notes 4, 17 and 26	t_r, t_f	–	–	10	ns
Load capacitance		C_L	–	–	30	pF
Output capacitance	OFF state; note 26	C_{off}	–	–	10	pF
Output leakage current	OFF state; V_I = 0 to V_{DD}	I_{off}	−10	–	+ 10	μA
VDS (3-state)	note 29					
Output voltage LOW	I_{OL} = 1.0 mA	V_{OL}	0	–	0.2	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	1.1	–	2.8	V
Output rise and fall times	note 26	t_r, t_f	–	–	10	ns
Load capacitance		C_L	–	–	30	pF
Output leakage current	OFF state; V_I = 0 to V_{DD}	I_{off}	−10	–	+ 10	μA

* Adjustable over 0.5 to 1.5 V, via the I^2C-bus.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
TIMING						
I²C-bus	note 20					
SCL clock frequency		f_{SCL}	0	–	100	kHz
Input clock period						
HIGH time		t_{HIGH}	4	–	–	μs
LOW time		t_{LOW}	4	–	–	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop set-up time from clock HIGH		$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop		t_{BUF}	4	–	–	μs
Start hold time		$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock LOW-to-HIGH transition		$t_{SU;STA}$	4	–	–	μs
Memory interface	note 14					
Cycle time		t_{CY}	–	481	–	ns
Transition time		t_T	–	–	10	ns
$\overline{RAS}$ pulse width		$t_{W;RAS}$	120	–	–	ns
$\overline{RAS}$ pre-charge time		$t_{PC;RAS}$	90	–	–	ns
$\overline{CAS}$ hold time		$t_{HD;CAS}$	120	–	–	ns
Page mode cycle time		$t_{CY;PM}$	120	–	–	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time		t_d	25	–	–	ns
$\overline{CAS}$ pulse width		$t_{W;CAS}$	60	–	–	ns
$\overline{CAS}$ pre-charge time		$t_{PC;CAS}$	50	–	–	ns
Row address set-up time		$t_{SU;ROW}$	0	–	–	ns
Row address hold time		$t_{HD;ROW}$	15	–	–	ns
Column address set-up time		$t_{SU;COL}$	0	–	–	ns
Column address hold time		$t_{HD;COL}$	20	–	–	ns
Read command set-up time		$t_{SU;RD}$	0	–	–	ns
Read command hold time referenced to $\overline{CAS}$		$t_{HD;RDC}$	0	–	–	ns
Read command hold time referenced to $\overline{RAS}$		$t_{HD;RDR}$	10	–	–	ns
Access time from $\overline{CAS}$		$t_{ACC;CAS}$	–	–	60	ns

parameter	conditions	symbol	min.	typ.	max.	unit
Write command pulse width		$t_{W;WR}$	50	–	–	ns
Write command hold time		$t_{HD;WR}$	40	–	–	ns
Data-in set-up time		$t_{SU;DATI}$	0	–	–	ns
Data-in hold time		$t_{HD;DATI}$	40	–	–	ns
Access time from $\overline{RAS}$		$t_{ACC;RAS}$	–	–	120	ns
$\overline{RAS}$ hold time after $\overline{CAS}$		$t_{HD;RC}$	60	–	–	ns
$\overline{CAS}$ to $\overline{RAS}$ pre-charge time		$t_{PC;CR}$	20	–	–	ns
Column address hold time referenced to $\overline{RAS}$		$t_{HD;COLR}$	80	–	–	ns
Data-in hold time referenced to $\overline{RAS}$		$t_{HD;DATIR}$	100	–	–	ns

Notes to the characteristics

1. The rise time of V_{DD} from 0 to 4.5 V must be >150 ns to ensure that the internal power-on reset triggers. For this circuit to reset the chip, V_{DD} must be initially <1.0 V or fall to <1.0 V for at least 100 ns. Spikes on V_{DD} are tolerable provided that V_{DD} is not reduced to <2.5 V.
2. All inputs are protected against static charge under normal handling.
3. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor.
4. Rise and fall times are measured between 10% and 90% levels.
5. Teletext input data set-up and hold times are measured with respect to 50% duty factor level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2.0 V, data stable 0 $\leqslant$ 0.8 V.
6. Clamp times measured from the line sync reference point, assuming acquisition timing is set correctly.
7. Clamp transistor on, $V_{TTD} - V_{SSI} \leqslant 0.1$ V.
8. The TTC input has an internal clamping diode.
9. HSA is falling edge triggered.
10. Minimum and maximum cycles times are $\pm$ 7.1% of the typical value.
11. Fall time is measured between 3.0 V and 1.5 V.
12. Applies even when $V_{DD} = 0$ V.
13. All input/outputs and outputs are protected against static charge under normal handling.
14. For details of memory interface timings to and from external DRAM see Fig. 5 and Fig. 6.

Notes to the characteristics (continued)

15. Output fall time measured between 4.0 V and 1.0 V levels with a 3.3 kΩ load to 5.0 V.
16. Output rise and fall times measured between 0.8 V and 2.0 V levels.
17. Measured with $V_{SS0} = V_{SS}$ and output voltage (C_{DAC}) = 1.5 V.
18. Measured with $V_{SS0} = V_{SS}$ and output voltage (C_{DAC}) = 0.5 V to 1.5 V.
19. Skew delay time measured at 0.7 V levels.
20. For details of I²C-bus timings see Fig. 3; timings are referred to V_{IH} = 3.0 V and V_{IL} = 1.5 V.
21. Load capacitance measured with two DRAM data inputs; 50 pF maximum.
22. A current of 1 μA flows out of the SAA5191 or SAA5236 while its SAND input is in the range of 1 V to 3.5 V.
23. Load capacitance measured with eight DRAM data inputs; 80 pF maximum.
24. Through a 200 pF capacitor with a 13.5 MHz sinewave.
25. To be applied via the series capacitor only.
26. This specification point is included because of its importance to the application environment; it is not however guaranteed.
27. When connected to the SAA5191, it is acceptable for the clock frequency to initially attain ⩽ 15 MHz in order to achieve synchronism.
28. When connected to the SAA5191, it is acceptable for the input voltage to attain V_{DD} + 0.9 V. The input current must be restricted as specified in the RATINGS.
29. These outputs can be made 3-state via the I²C-bus.

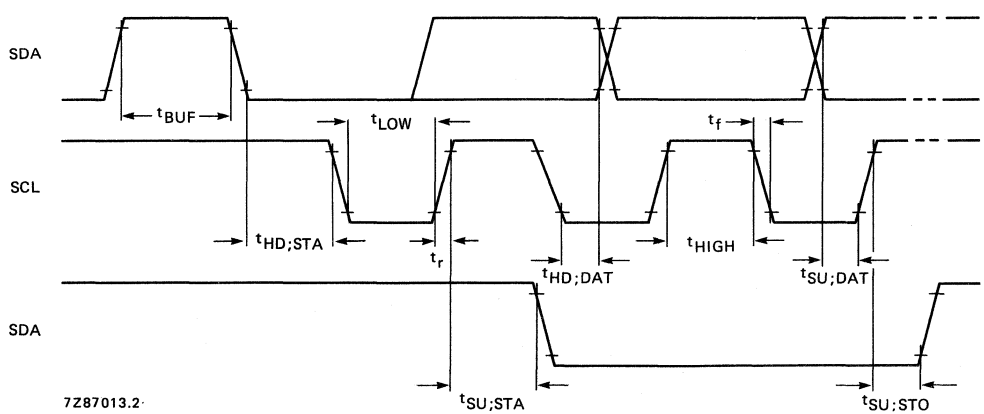


Fig.3 I²C-bus timing.

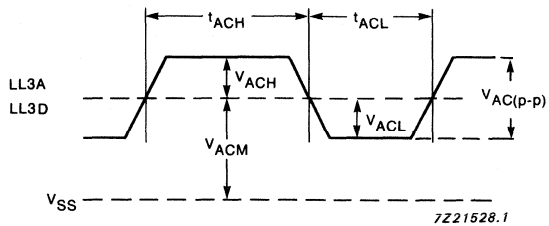


Fig.4 Line-Locked system clock LL3A and LL3D timing diagram.

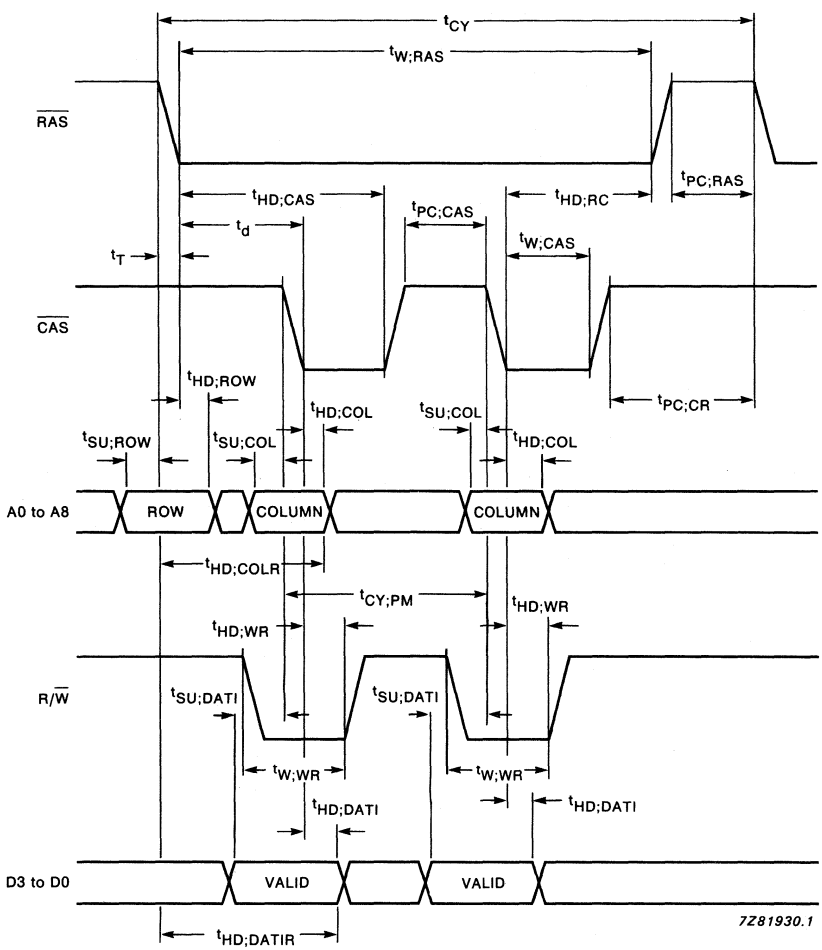


Fig.5 Memory interface timing for write cycle to external DRAM.

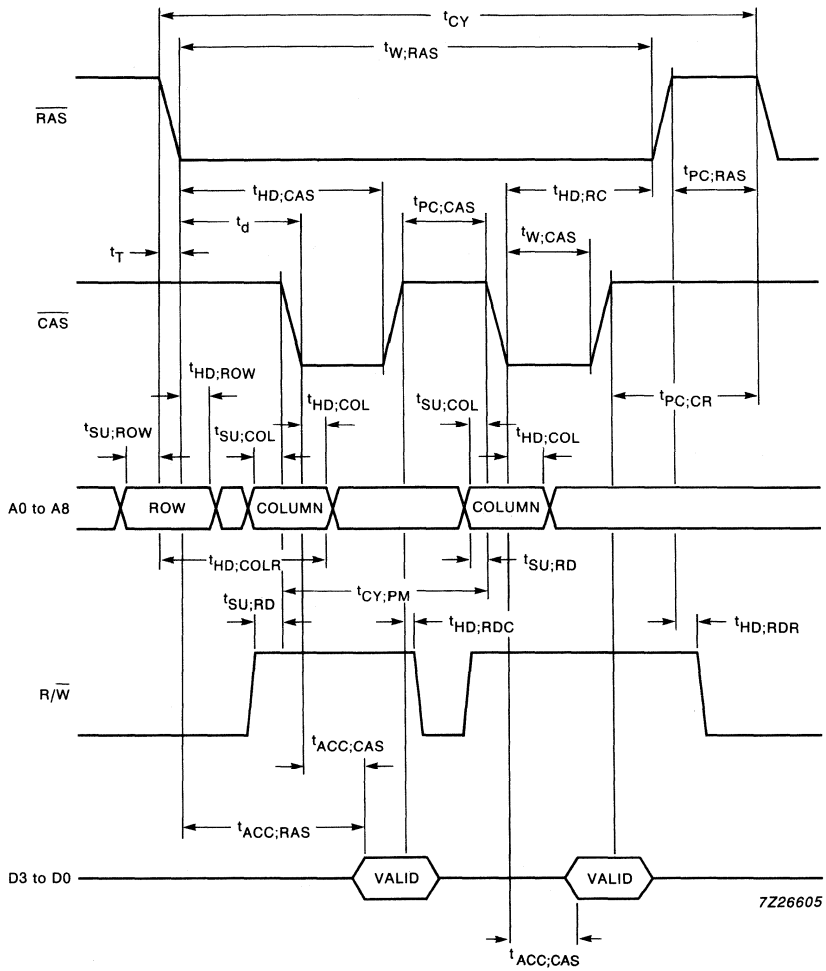
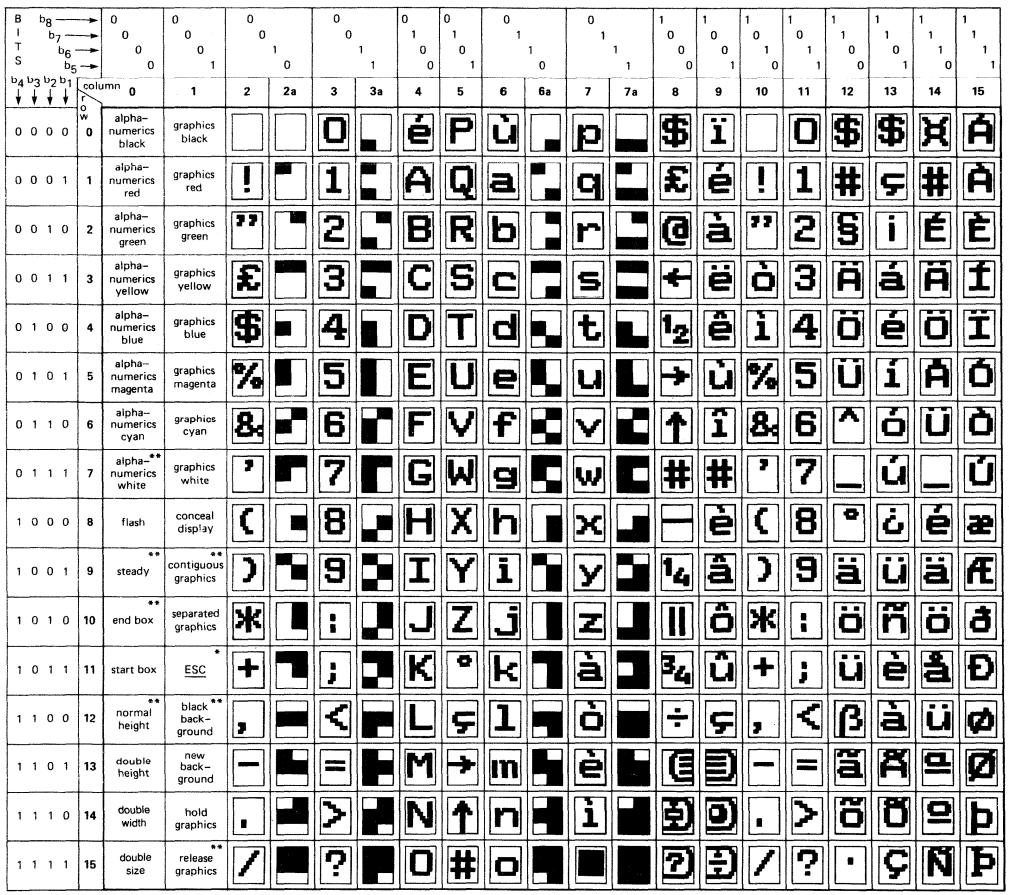


Fig.6 Memory interface timing for read cycle from external DRAM.

DEVELOPMENT DATA



*These control characters are reserved for compatability with other data codes.

**These control characters are presumed before each row begins.

Fig.7 SAA9042A West European character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

7Z22659.2

(1) Where PHCB are the page Header Control Bits.
Other combinations of PHCB default to English.

Fig.8 SAA9042A West European national option sets.

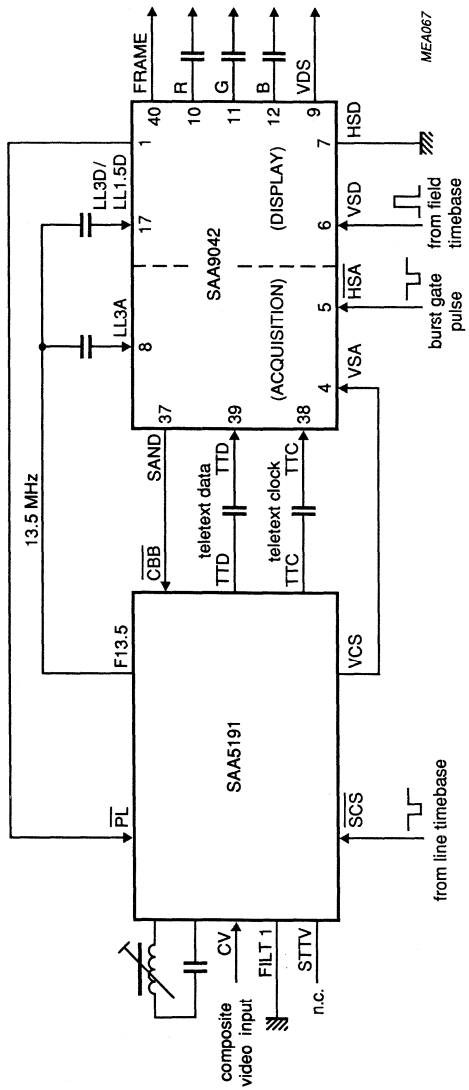


Fig.9 Synchronization of SAA9042 in analog TV (slave sync mode).

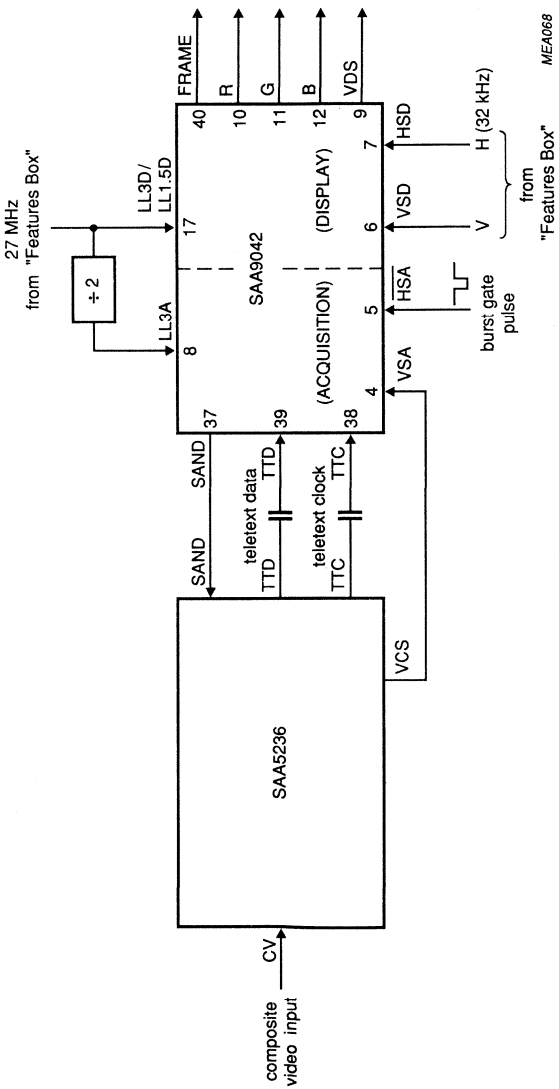


Fig.10 Synchronization of SAA9042 in analog TV with 2 x H features.

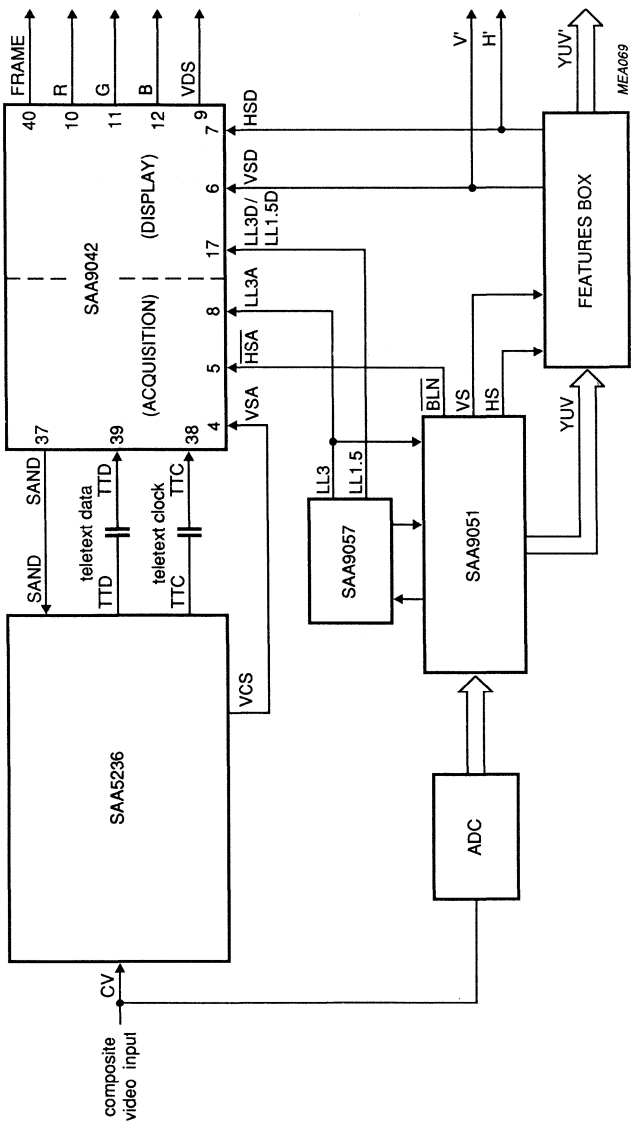


Fig.11 Synchronization of SAA9042 in digital TV with 2 x H features.

Philips Semiconductors

Data sheet	
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SAA9051

Digital multistandard TV decoder with separate chrominance and luminance inputs

FEATURES

- All operations based on a sampling frequency of 13.5 MHz, providing:
  - full adaptability to all transmission standards
  - capability for memory-based features
- Separate chrominance and luminance input (Y/C)
- CVBS input for standard applications
- CVBS throughput capability for SECAM application
- Luminance signal processing for all TV standards (PAL, NTSC, SECAM, B/W)
- Horizontal and vertical synchronization detection for all standards
- Chrominance signal processing for all quadrature amplitude modulated colour-carrier signals
- Requires only one crystal
- Controlled via the I²C-bus
- User-programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filter (NTSC)
- Wide range hue control

GENERAL DESCRIPTION

The SAA9051 digital multistandard decoder (S-DMSD) performs demodulation and decoding of all quadrature modulated colour TV standards, as well as performing luminance and processing for all TV standards with CVBS or Y/C input signals.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9051	68	PLCC	plastic	SOT188

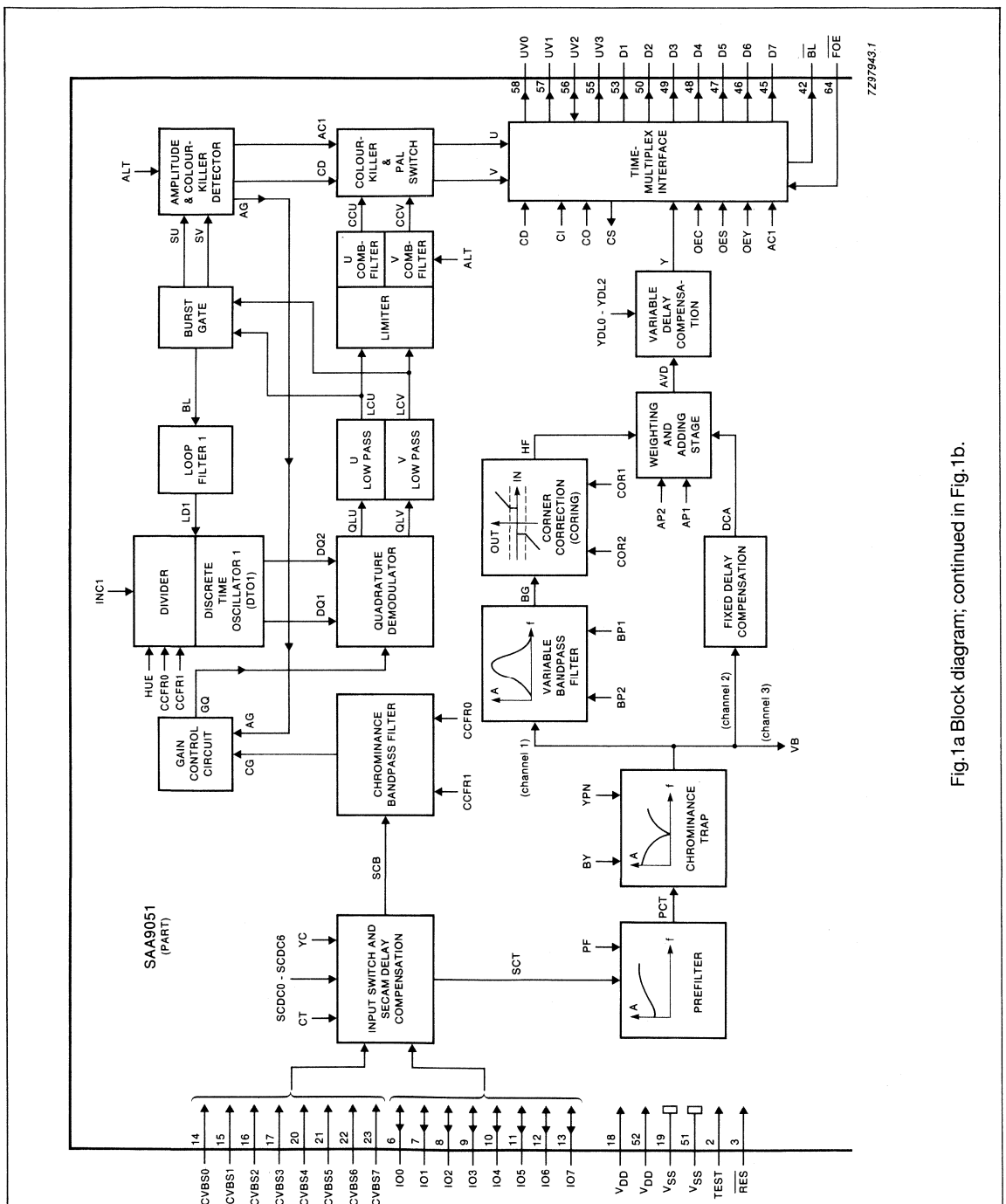


Fig.1a Block diagram; continued in Fig.1b.

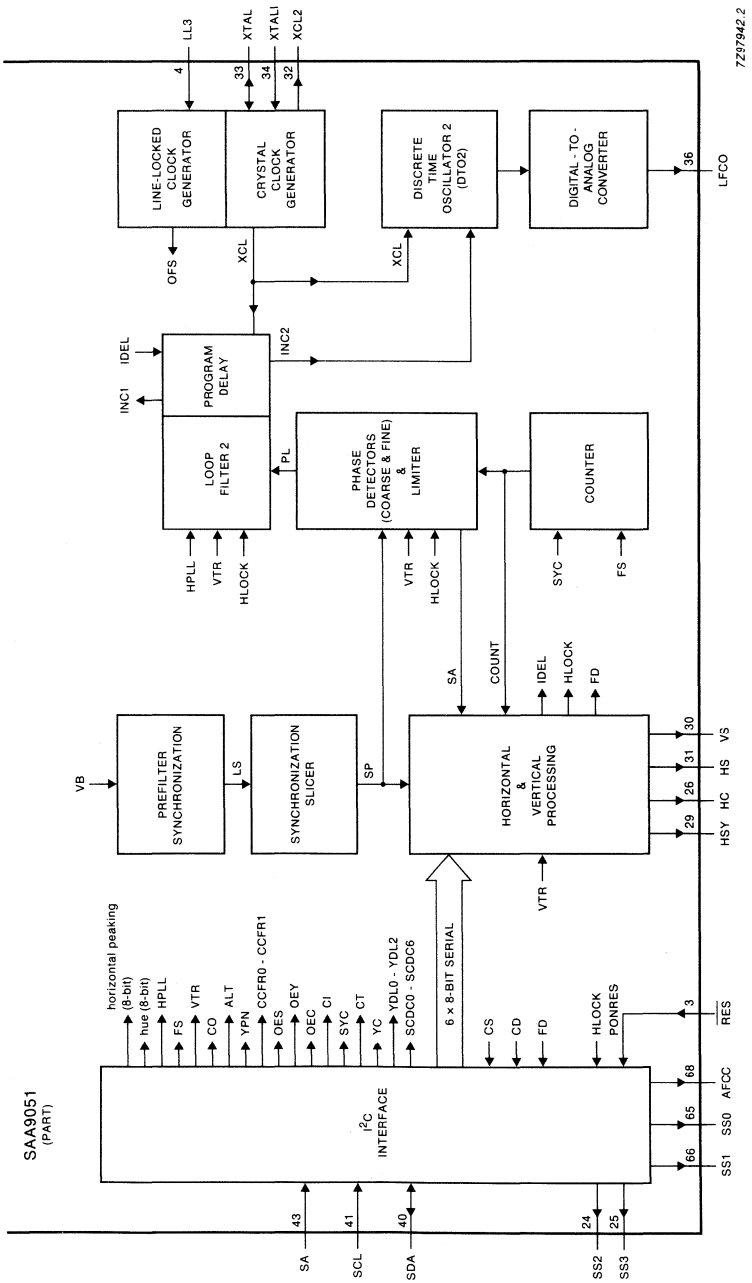


Fig.1b Block diagram; from Fig.1a.

PIN CONFIGURATION

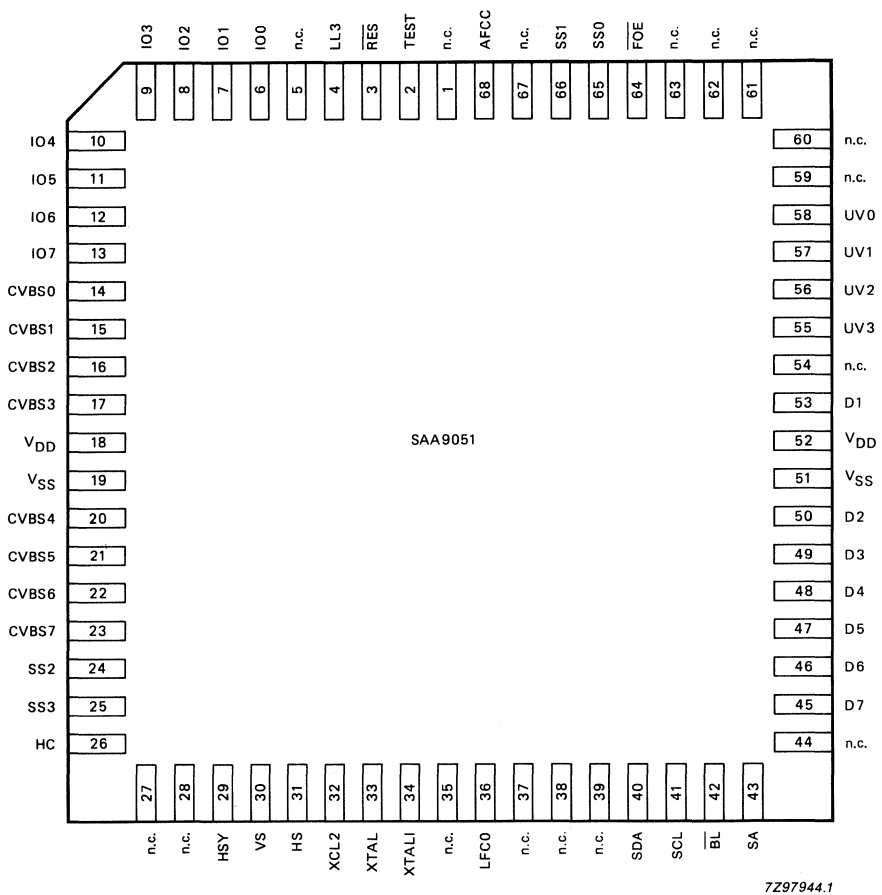


Fig.2 Pinning configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
TEST	2	test input (active HIGH); when HIGH enables scan-test mode
$\overline{RES}$	3	reset input (active LOW); results in the I²C-bus control registers 1 to 3 and internal stages being reset during the reset phase. The minimum LOW period of $\overline{RES}$ is 120 LL3 clock cycles
LL3	4	13.5 MHz line-locked system clock
n.c.	5	not connected
IO0 (LSB) – IO7 (MSB)	6 – 13	bidirectional data path; chrominance input for separate luminance and chrominance input (Y/C) or CVBS output for SECAM decoder SAA9056. Two's complement format (IO0 is only used internally for CVBS throughput)
CVBS0 (LSB) – CVBS7 (MSB)	14 – 17, 20 – 23	digitalized composite video blanking and synchronization signals; containing luminance, chrominance and all synchronization information or luminance, blanking and synchronization signals in the event of separate luminance and chrominance (Y/C) input. Two's complement format (CVBS0 is only used internally for CVBS throughput)
V_{DD}	18	positive supply voltage (+5 V)
V_{SS}	19	ground (0 V)
SS2 – SS3	24 – 25	source select output signals; I²C-bus controlled, TTL compatible switches
HC	26	programmable horizontal output pulse; when used in conjunction with the TDA9045 or TDA8708 it indicates the black-level position before analog-to-digital conversion. The start and stop times are programmable, between –9.4 µs and +9.5 µs in steps of 74 ns, via the I²C-bus
n.c.	27 – 28	not connected
HSY	29	programmable horizontal output pulse; when used in conjunction with the TDA9045 OR TDA8708 it indicates the synchronization pulse position before analog-to-digital conversion. The start and stop times are programmable, between –14.2 µs and +4.7 µs in steps of 74 ns, via the I²C-bus
VS	30	vertical synchronization output; indicates the vertical position of the picture for 50/60 Hz field frequency

PINNING (continued)

SYMBOL	PIN	DESCRIPTION
HS	31	horizontal synchronization pulse output (duration = 64 LL3 clock cycles). HS is programmable, between −32 µs and +32 µs in steps of 300 ns, via the I²C-bus
XCL2	32	clock output; half of the crystal clock frequency (12.288 MHz). In phase with XTAL (pin 33)
XTAL	33	crystal oscillator input/inverting amplifier output; input to the internal clock generator from an external oscillator or output of the inverting amplifier to an external crystal (24.576 MHz)
XTALI	34	input to the inverting amplifier from an external crystal (24.576 MHz); connect to ground if an external oscillator is used
n.c.	35	not connected
LFCO	36	line frequency control; analog output representing a multiple of the line frequency (6.75 MHz) with 4-bit resolution, the phase of which is compared to the system clock by the CGC (SAA9057)
n.c.	37 – 39	not connected
SDA	40	I²C-bus serial data input/output
SCL	41	I²C-bus serial clock input
$\overline{BL}$	42	blanking signal output (active LOW); indicates the active video and line blanking periods. $\overline{BL}$ also synchronizes the data multiplexers/demultiplexers
SA	43	I²C-bus select address; input for selection of the appropriate I²C-bus slave address
D7 (MSB) – D1 (LSB)	45 – 50, 53	luminance data output
V_{SS}	51	ground (0 V)
V_{DD}	52	positive supply voltage (+5 V)
n.c.	54	not connected
UV3 – UV0	55 – 58	multiplexed PAL or NTSC colour difference signal output or SECAM CS input signal from the SECAM decoder. Output data format is two's complement. The multiplexer is synchronized to the rising-edge of $\overline{BL}$
n.c.	59 – 63	not connected
$\overline{FOE}$	64	fast output enable signal (active LOW); sets D1 – D7 and UV0 – UV3 outputs to the HIGH-impedance Z-state

SYMBOL	PIN	DESCRIPTION
SS0 – SS1	65 – 66	source select output signals, set via the I²C-bus; used to control the input switch (e.g. TDA9045)
n.c.	67	not connected
AFCC	68	additional output for circuit control; activated via the I²C-bus

FUNCTIONAL DESCRIPTION

(see Fig.1)

The S-DMSD performs demodulation and decoding for all quadrature modulated colour TV standards (PAL-B, G, H, I, M, N, NTSC 4.43 MHz, NTSC-M), as well as performing luminance and parts of the synchronization processing for TV standards (PAL, NTSC and SECAM). All of the controllable functions, user as well as factory adjustments, are accessed via I²C-bus. Thereby enhancing the adaptability of the digital TV concept.

Operation is based on a line-locked sampling frequency of 13.5 MHz, making the system fully adaptable to all line frequencies and requiring only one crystal for all TV standards.

The S-DMSD is designed to operate in conjunction with the SAA9057A (CGC). If the CGC is not utilized the designer must ensure:

- a reset pulse is applied to the S-DMSD after a power failure
- that a continuous clock signal (minimum 1 MHz) is connected to the S-DMSD.

Y/C processing

In the Y/C mode, the following occurs:

- The chrominance signal is input at the IO port (IO0 – IO7) and transmitted via the input switch/ SECAM delay compensation circuit (multiplexer) to the chrominance bandpass filter (see section chrominance path)
- The other components, Y signal and synchronization pulse, are input via inputs CVBS0 – CVBS7 and transmitted via the input switch/SECAM delay compensation circuit to the luminance prefilter.

CVBS processing

In the CVBS mode:

- The CVBS signal is separated into its luminance (VBS) and chrominance (CG) parts by the chrominance trap and bandpass circuits. These circuits can be switched by the standard identification signals (CCFR0, CCFR1/YPN) according to the detected colour-carrier frequency, 3.58 MHz or 4.43 MHz.
- On reception of a SECAM signal the signal is transmitted to the SECAM decoder (SAA9056) via the IO port (IO0 – IO7). Bit CT enables the 3-state buffer between both parts.

Luminance path

The luminance path is separated into three channels after the chrominance trap stage (see Fig.1). The following occurs:

CHANNEL 1 SIGNAL

The channel 1 signal is transmitted to the programmable bandpass filter where the high luminance frequencies are removed (centre frequency is programmable via bits BP1 and BP2). The signal BC is transmitted to the coring (corner correction) stage where low amplitude noise is removed (amount of low amplitude noise removal is programmable via bits COR1 and COR2). The signal HF is transmitted to the weighting and adding stage, see section 'Combining channel 1 and channel 2 signals'.

CHANNEL 2 SIGNAL

The channel 2 signal is transmitted to the fixed delay compensation stage where delay compensation and black level adjustment occurs. The signal DCA is transmitted to the weighting and adding stage, see section 'Combining channel 1 and channel 2 signals'.

FUNCTIONAL DESCRIPTION (continued)

Luminance path (continued)

CHANNEL 3 SIGNAL

The channel 3 signal VB is transmitted to the prefilter synchronization stage, see section 'Synchronization path'.

COMBINING CHANNEL 1 AND CHANNEL 2 SIGNALS

The channel 1 signal HF is weighted and added to the Channel 2 signal DCA. The combined signals are matched to the specified amplitude and the word size is reduced to 7 bits. The signal AVD is transmitted to the variable delay compensation stage where compensation for IF group delays occurs, the amount of delay is programmable (from −4 to +3 LL3 clock cycles, see note) via bits YDL0 – YDL2. The signal Y is transmitted to the time multiplexed interface where the signal is output via D1 – D7.

Note

Differences in the delay compensation required for PAL and NTSC are catered for by identification signal YPN which switches the chrominance trap to the appropriate colour-carrier frequency 3.58 MHz or 4.43 MHz.

Chrominance path

In the chrominance path the following occurs (see Fig.1):

The chrominance signal CG is transmitted from the chrominance bandpass stage to the gain control circuit (see note 1). The gain control stage ensures that the chrominance signal has constant burst amplitude. The signal GQ is transmitted to the quadrature demodulator, where demodulation of the quadrature modulated chrominance signal GQ to colour difference signals occurs. The signals QLU and QLV are transmitted to a low-pass filter for filtering. The signals LCU and LCV are transmitted to the limiter and comb-filter stage. The comb-filter stage (see note 2) separates remaining vertically correlated luminance components for NTSC (for PAL, the signals are phase corrected). The signals CCU and CCV are transmitted to the colour-killer and PAL switch stage (see note 3). At this stage signals which do not comply with the selected standard are removed. In PAL mode this stage restores the correct phase of signal V. The signals are then transmitted to the time multiplexed interface and output via UV0 – UV3.

Notes

1. The gain control stage is controlled by signal AG which is derived form the amplitude and colour-killer detector stage (ACKD). A non-standard burst to amplitude ratio results in an automatic colour-leveling stage functioning as an amplitude detector to ensure correct amplitude and avoid overflow/limiter defects.
2. The comb-filter can be altered from alternate to non-alternate mode by the ALT signal.
3. The colour-killer and PAL switch stage are controlled by the amplitude and colour-killer detection circuit using signals AC1 and CD.

COLOUR-CARRIER FREQUENCY REGENERATION

The regeneration of the colour-carrier frequency is performed by the phase-locked-loop (PLL) which comprises of a quadrature demodulator, low-pass filter, burst gate, loop filter 1 and divider/discrete time oscillator (DTO1). The DTO1 is controlled by the standard identification signals CCFR0 – CCFR1 and the Hue signal which influences the demodulation phase of the chrominance signal.

Synchronization path

In the synchronization circuit, prefilter synchronization is implemented to normalize the synchronization pulse slopes. A synchronization-slicer provides the detected synchronization pulses (SP) to the horizontal and vertical processing and phase detector stages.

HORIZONTAL AND VERTICAL PROCESSING

The horizontal and vertical processing comprises part of a PLL circuit for regeneration of the horizontal synchronization (HS) and an adaptive filter for detection of the vertical synchronization (VS). The horizontal and vertical processing also generates:

- coincidence signal HLOCK which controls the mute function
- standard identification signal FD which identifies nominal 525 or 625 lines per picture.

PHASE DETECTORS

The phase detectors that receive the SP signal, also part of the PLL, control the generation of the line-locked clock (PL). Loop filter 2, which has a variable bandwidth dependent on the time constant signal VTR, generates two increment signals (INC1 and INC2) with different delays. INC2 is programmable via the increment delay signal IDEL. INC1 corrects the regenerated subcarrier frequency at DTO1 and INC2 performs phase incrementing of DTO2. The crystal clock generator provides a stable 24.576 MHz clock input to DTO2 which in turn supplies the 4-bit DAC with a digital control signal of 432 or 429 times the line frequency. The analog output LFCO from the DAC is transmitted to the SAA9057 (CGC).

Output interface

The signals OES, OEY, OEC, CO, CI and CD control the output interface (see Fig.5). All but one of these signals are received via the I^2C-bus, the exception being signal CD which is detected in the S-DMSD. A power-ON reset results in these signals being set to zero.

Table 1 OES signal

OES	OUTPUTS	OUTPUT STATUS
0	HS and VS	inactive (HIGH-impedance Z-state)
1	HS and VS	active

Table 2 CO, CI and CD signals

CO	CI	CD	OUTPUTS	OUTPUT STATUS
0	X	X	UV0 – UV3	colour OFF (zero)
1	0	0	UV0 – UV3	colour OFF (controlled by CD)
1	0	1	UV0 – UV3	colour ON (controlled by CD)
1	1	X	UV0 – UV3	colour forced ON

Where:

X = don't care.

$\overline{\text{FOE}}$ signal

In PIPCO (picture-in-picture controller, SAA9068) applications, the PIPCO requires access to the digital YUV-bus on a pixel time-base. This requirement is catered for by PIPCO generated signal $\overline{\text{FOE}}$, which forces all data output of the S-DMSD and DSD (SAA9056) into the HIGH-impedance Z-state. The $\overline{\text{FOE}}$ signal does not affect the synchronization data lines (HS and VS) or the blanking data line ($\overline{\text{BL}}$), see Fig.6.

FUNCTIONAL DISCRIPTION (continued)

Output interface (continued)

Table 3 OEC, OEY, $\overline{FOE}$, $\overline{BL}$, D1 – D7 and UV0 – UV3 signals

OEC	OEY	$\overline{FOE}$	$\overline{BL}$	D1 – D7	UV0 – UV3	REMARKS
0	0	X	HIZS	HIZS	HIZS	status after power-ON reset
1	1	1	active	HIZS	HIZS	
1	1	0	active	active	active	
0	1	1	active	HIZS	HIZS	
0	1	0	active	active	active	

Where:

X = don't care
HIZS = HIGH-impedance Z-state.

Note to Table 3

1. Combinations other than those shown in Table 3 are not allowed.

CS signal

The CS signal is transmitted from the digital SECAM decoder (DSD) during the H-blanking period and is received via the UV2 input (see Fig.5). The CS bit is read by the S-DMSD once per line at LL3 clock cycle number 748, see Fig.7.

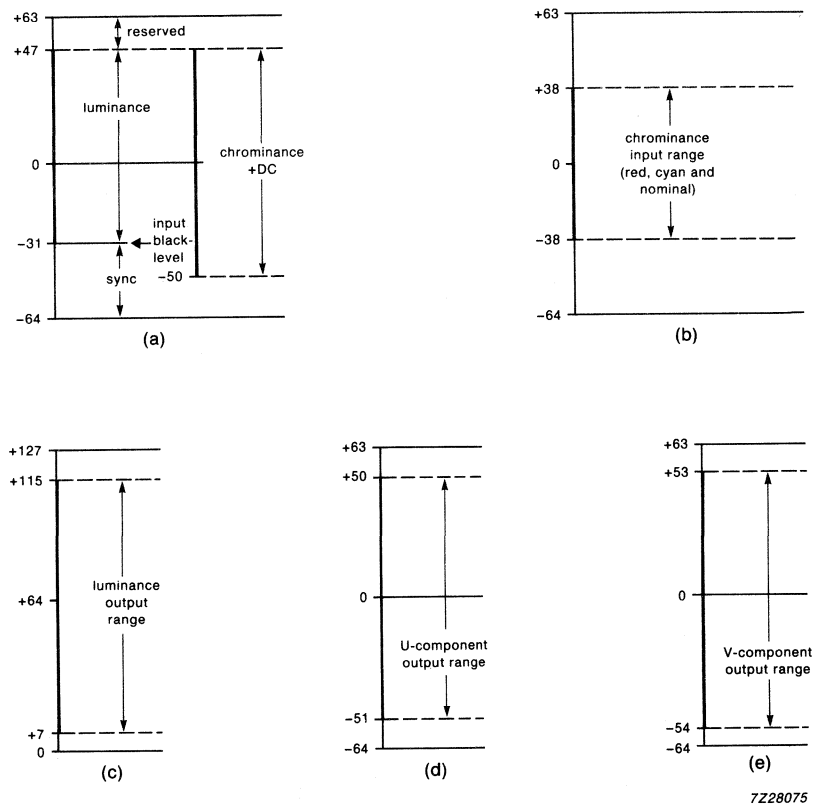
I²C bus interface (see Tables 1 to 3)

The following control signals are received via the I²C bus interface:

- standard identification signals (CCFR0, CCFR1, ALT, FS, YPN)
- video recorder/TV time constant (VTR)
- hue control (HUE)
- delay programming of the horizontal signals (HS, HC, HSY)
- increment-delay (IDEL)
- luminance aperture-correction control (BY, PF, BP2, COR2, COR1, AP2, AP1)
- luminance delay compensation (YDL0, YDL1, YDL2)
- fixed clock generation command (HPLL)
- internal colour ON/OFF (CO)
- internal colour forced ON, test purposes only (CI)
- synchronization output enable (OES)
- luminance output enable (OEY)
- chrominance output enable (OEC)
- switch signals (source select signals SS0, SS1, SS2, SS3)
- additional output for circuit control (AFCC)
- chrominance source select CVBS/ chrominance input/output (CT/ YC).
- SECAM chrominance delay compensation (SCDC0, SCDC21, SCDC2, SCDC3, SCDC4, SCDC5, SCDC6).

Signals transmitted from the S-DMSD via the I²C bus are:

- standard identification signals (FD, CS)
- colour-killer status signal (CD)
- coincidence information (HLOCK)
- power-on-reset of S-DMSD (PONRES).



(a) CVBS1 to CVBS7 input range

(b) IO1 to IO7 input range

(c) Y output range

(d) U output range –(B – Y)

(e) V output range –(R – Y)

Fig.3 Diagram showing input/output range of the S-DMSD; all levels in EBU colour bar, values in binary, 100% luminance and 75% chrominance amplitude.

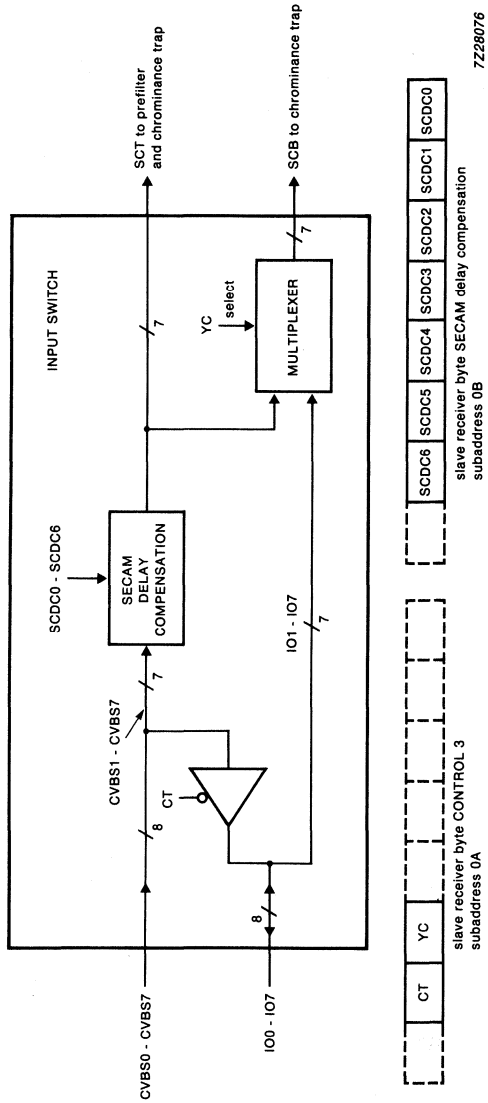


Fig.4 Schematic diagram of the input switch.

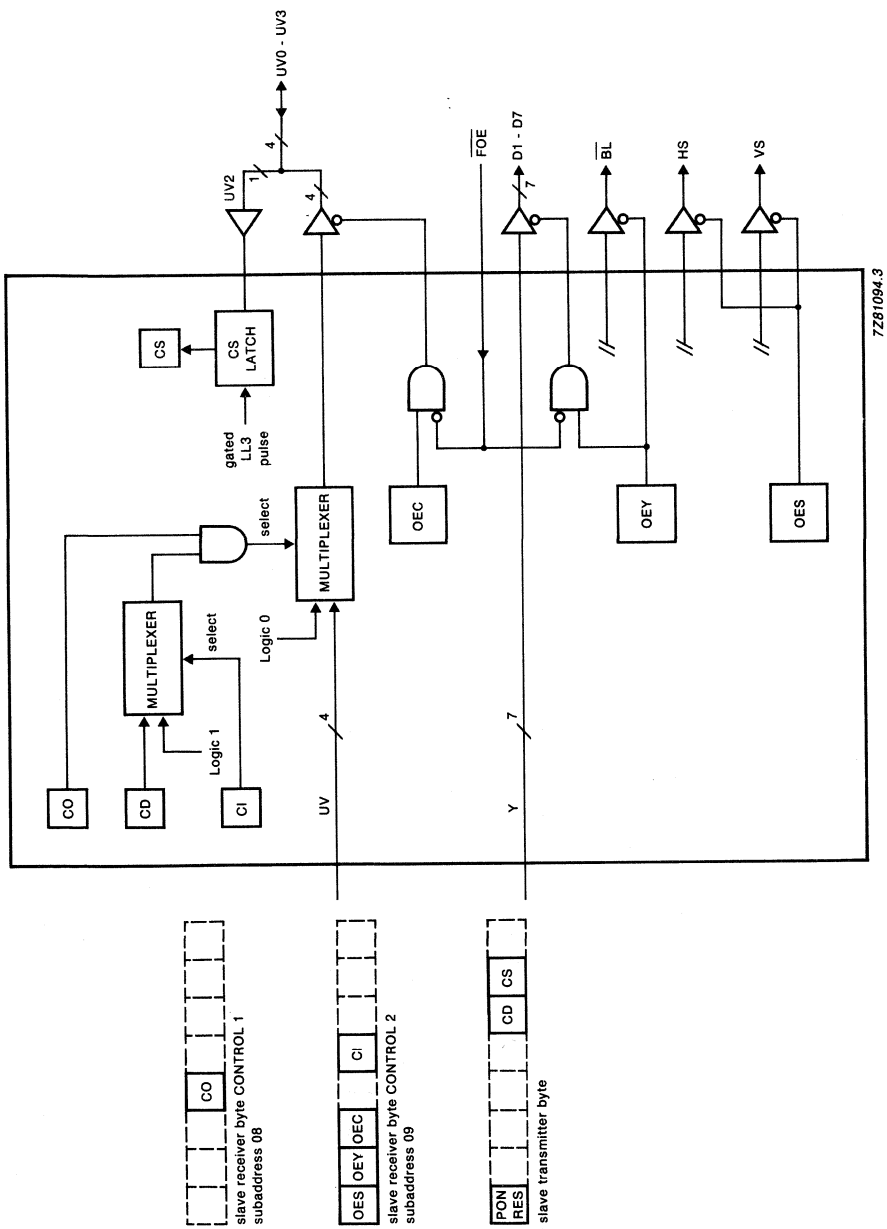


Fig.5 Schematic diagram of control signals at the output interface.

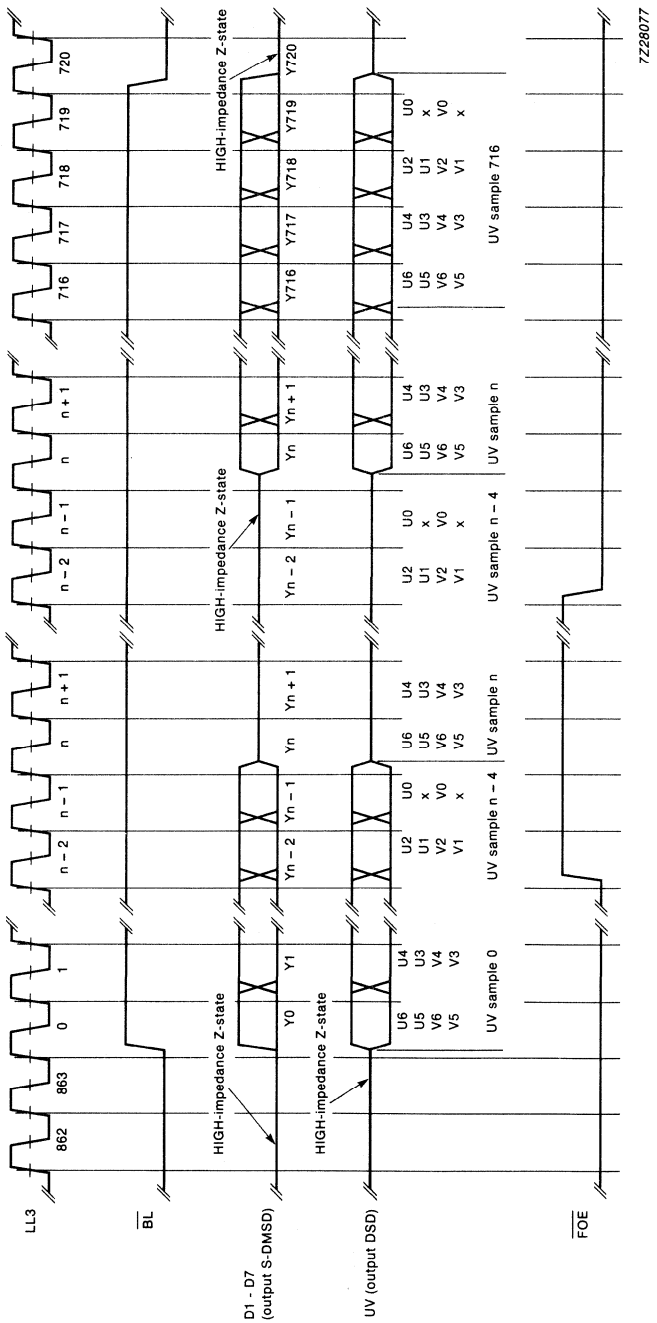
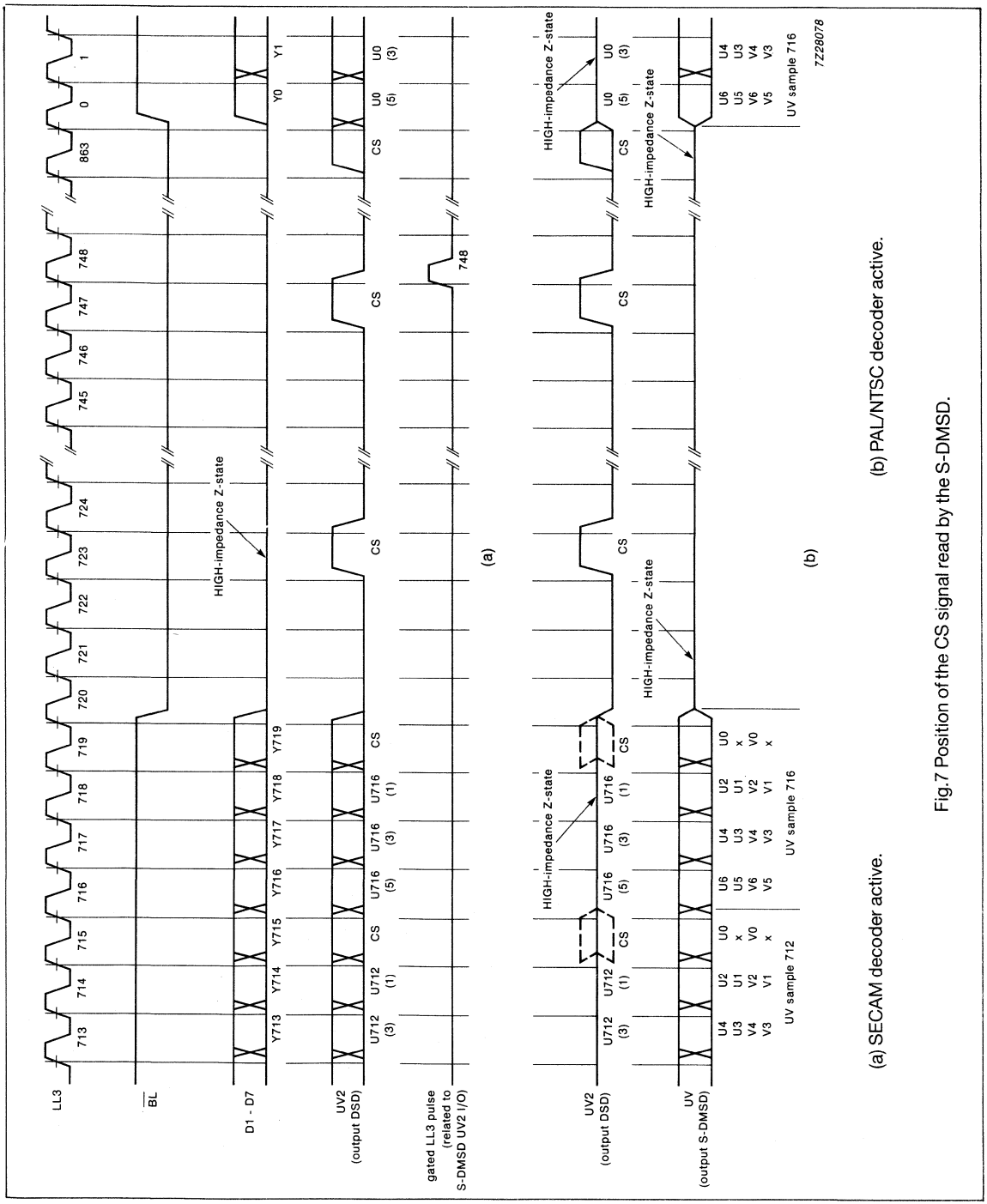


Fig.6 Timing waveform of the output data and $\overline{FOE}$ signals.



(a) SECAM decoder active.

(b) PAL/NTSC decoder active.

Fig.7 Position of the CS signal read by the S-DMSD.

SLAVE RECEIVER ORGANIZATION

Slave address and receiver format

There are two slave addresses, programmable via input SA, which determine the operating mode of the S-DMSD, see Table 4.

Table 4 Slave addresses

SLAVE RECEIVER ADDRESS									REMARKS
SA	A6	A5	A4	A3	A2	A1	A0	*	
0	1	0	0	0	1	0	1	0	binary value (8A hex)
1	1	0	0	0	1	1	1	0	binary value (8E hex)

Where:

* = logic 0, receiver mode
* = logic 1, transmitter mode.

Table 5 Subaddress byte and data byte formats

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Increment delay IDEL	00	A07	A06	A05	A04	A03	A02	A01	A00
HSY start time	01	A17	A16	A15	A14	A13	A12	A11	A10
HSY stop time	02	A27	A26	A25	A24	A23	A22	A21	A20
HC start time	03	A37	A36	A35	A34	A33	A32	A31	A30
HC stop time	04	A47	A46	A45	A44	A43	A42	A41	A40
HS start time (after PHI1)	05	A57	A56	A55	A54	A53	A52	A51	A50
Horizontal peaking	06	BY	PF	BP2	BP1	COR2	COR1	AP2	AP1
Hue control	07	A77	A76	A75	A74	A73	A72	A71	A70
Control 1	08	HPLL	FS	VTR	CO	ALT	YPN	CCFR1	CCFR0
Control 2	09	OES	OEY	OEC	X	CI	AFCC	SS1	SS0
Control 3	0A	SYC	CT	YC	SS3	SS2	YDL2	YDL1	YDL0
SECAM delay compensation	0B	X	SCDC6	SCDC5	SCDC4	SCDC3	SCDC2	SCDC1	SCDC0
Reserved	0C – 0F	X	X	X	X	X	X	X	X

Where:

X = don't care.

Notes to Table 5

The subaddress is automatically incremented. This enables quick initialization, within one transmission, by the I²C-bus controller.

The subaddresses shown are acknowledged by the device. Subaddresses 10 to 1F (reserved for the SECAM decoder SAA9056) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.

After power-on-reset the control registers 1 to 3 (subaddresses 08, 09 and 0A) are, with the exception of bits YDL0 – YDL2 of counter 3, set to logic 0. All other registers are undefined.

The least significant bit of an analog control or alignment register is defined as AX0.

SUBADDRESS 00

Table 6 Increment delay control IDEL (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS*							
		A07	A06	A05	A04	A03	A02	A01	A00
–1 to –110	–148 ns (min. value)	1	1	1	1	1	1	1	1
–1 to –110	–16.3 µs (outside available range)	1	0	0	1	0	0	1	0
–111 to –214	–16.44 µs	1	0	0	1	0	0	0	1
–111 to –214	–31.7 µs (max. value if FS = logic 1)	0	0	1	0	1	0	1	0
–215	–31.85 µs (outside central counter range if FS = logic 1)**		0		0		1		0
–216	–32 µs (max. value if FS = logic 0)**	0	0	1	0	1	0	0	0
–217 to –256	–32.148 µs (outside central counter if FS = logic 0)**		0		0		1		0
–217 to –256	–37.9 µs (outside central counter)**	0	0	0	0	0	0	0	0

Where:

* A sign bit, designated A08 and internally set to HIGH, indicate values are always negative.

** The horizontal PLL does not operate in this condition. The system clock frequency is set to a value fixed by the last update and is within ±7.1% of the nominal frequency.

SUBADDRESS 01

Table 7 Horizontal synchronization HSY start time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A17	A16	A15	A14	A13	A12	A11	A10
+ 191 to + 1	–14.2 µs (max. negative value)	1	0	1	1	1	1	1	1
+ 191 to + 1	–0.074 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
–1 to –64	+0.074 µs	1	1	1	1	1	1	1	1
–1 to –64	+4.7 µs (max. positive value)	1	1	0	0	0	0	0	0

SUBADDRESS 02

Table 8 Horizontal synchronization HSY stop time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS							
		A27	A26	A25	A24	A23	A22	A21	A20
+ 191 to + 1	−14.2 μs (max. negative value)	1	0	1	1	1	1	1	1
+ 191 to + 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −64	+0.074 μs	1	1	1	1	1	1	1	1
−1 to −64	+4.7 μs (max. positive value)	1	1	0	0	0	0	0	0

SUBADDRESS 03

Table 9 Horizontal clamp HC start time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS							
		A37	A36	A35	A34	A33	A32	A31	A30
+ 127 to + 1	−9.4 μs (max. negative value)	0	1	1	1	1	1	1	1
+ 127 to + 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −128	+0.074 μs	1	1	1	1	1	1	1	1
−1 to −128	+9.5 μs (max. positive value)	1	0	0	0	0	0	0	0

SUBADDRESS 04

Table 10 Horizontal clamp HC stop time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS							
		A47	A46	A45	A44	A43	A42	A41	A40
+ 127 to + 1	−9.4 μs (max. negative value)	0	1	1	1	1	1	1	1
+ 127 to + 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −128	+0.074 μs	1	1	1	1	1	1	1	1
−1 to −128	+9.5 μs (max. positive value)	1	0	0	0	0	0	0	0

SUBADDRESS 05

Table 11 Horizontal synchronization HS start time after PHI1 (application dependent); 50 Hz; 625 lines (FS = 0)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/13.5 MHz = 296 ns)	CONTROL BITS							
		A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 109	Forbidden; outside available central counter range		0		1		1		1
+ 127 to + 109	Forbidden; outside available central counter range		0		1		1		0
+ 108 to + 1	−32 µs (max. negative value)	0	1	1	0	1	1	0	0
+ 108 to + 1	−0.296 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1 to −107	+0.296 µs	1	1	1	1	1	1	1	1
−1 to −107	+31.7 µs (max. pos. value)	1	0	0	1	0	1	0	1
−108 to −128	Forbidden; outside available central counter range		1		0		0		1
−108 to −128	Forbidden; outside available central counter range		1		0		0		0

Table 12 Horizontal synchronization start time after PHI1 (application dependent); 60 Hz; 525 lines (FS = 1)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/13.5 MHz = 296 ns)	CONTROL BITS							
		A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 107	Forbidden; outside available central counter range		0		1		1		1
+ 127 to + 107	Forbidden; outside available central counter range		0		1		1		0
+ 106 to + 1	−31.8 µs (max. negative value)	0	1	1	0	1	0	1	0
+ 106 to + 1	−0.294 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1 to −107	+0.294 µs	1	1	1	1	1	1	1	1
−1 to −107	+31.5 µs (max. pos. value)	1	0	0	1	0	1	0	1
−108 to −128	Forbidden; outside available central counter range		1		0		0		1
−108 to −128	Forbidden; outside available central counter range		1		0		0		0

Programming IDEL, HSY, HC and HS

The variables IDEL, HSY, HC and HS are programmed using data words via the I²C-bus. In the following examples a decrease in value corresponds to an increase in time.

IDEL (Fig.8)

The IDEL data word compensates for the time delays in data processing between loop filter 2, quadrature demodulator and internal/external (system) signal paths. The internal delay (t_{REF}) is the period required for INC1 to pass from the loop filter 2, through the divider and through DTO1. This delay corrects the relationship between the subcarrier frequency and the line frequency. The external path is a result of the following time delays (time delay is given in term of LL3 clock cycles):

- t_{IDEL}; programmable delay time
- t_a; processing time of DTO2 and the DAC
- t_b; chrominance bandpass and gain control stage delay times
- t_{CGC}; clock generator circuit delay time
- t_{ADC}; analog-to-digital converter delay time
- t_{INP}; input switch delay time.

As delay t_a and t_b are known constants, t_{IDEL} is programmed, range of −115 to −214/216 LL3 clock cycles, as follows:

- $t_{IDEL} = -115 - 0.5$ (* - $t_{CGC} - t_{ADC} - t_{INP}$).

HSY

Referring to Fig.9 point (1) and periods a and b:

- HSY start time = $t_{(1)}$ − a (LL3 clock cycles)
- HSY stop time = $t_{(1)}$ − b (LL3 clock cycles)

Programming range of HSY start/stop time: +191 to −64 (LL3 clock cycles).

HC

Referring to Fig.9 point (1) and periods c and d:

- HC start time = $t_{(1)}$ − c (LL3 clock cycles)
- HC stop time = $t_{(1)}$ − d (LL3 clock cycles)

Programming range of HSY start/stop time: +127 to −128 (LL3 clock cycles).

HS

The HS reference positions in PAL and NTSC modes are shown in Fig.9 at points (3) and (4) respectively. To move the HS pulse to the centre of blanking pulse BL the following equation is used:

- HS (NTSC);

  position of HS relative to the zero point (LL3 clock cycles)
  4 LL3 clock cycles

- HS (PAL);

  position of HS relative to the zero point (LL3 clock cycles)
  4 LL3 clock cycles

The length of HS is 64 LL3 clock cycles.

* Value to be fixed.

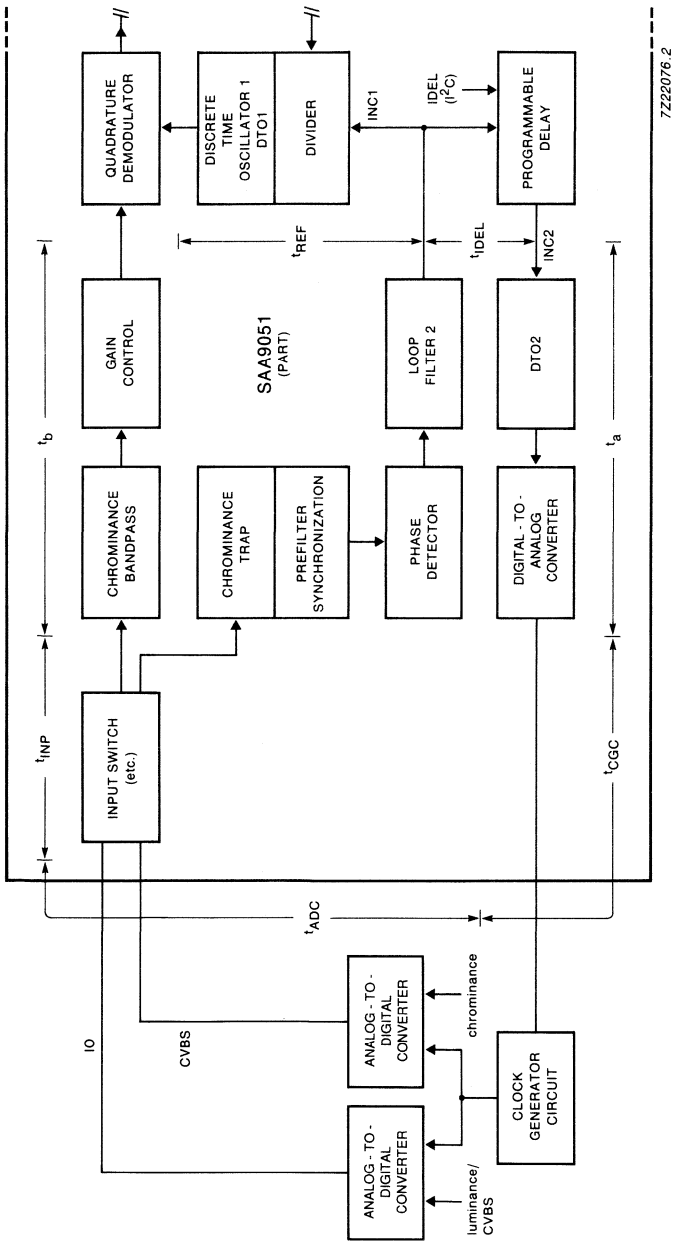


Fig.8 Compensation of delay times by incrementing delay control IDEL.

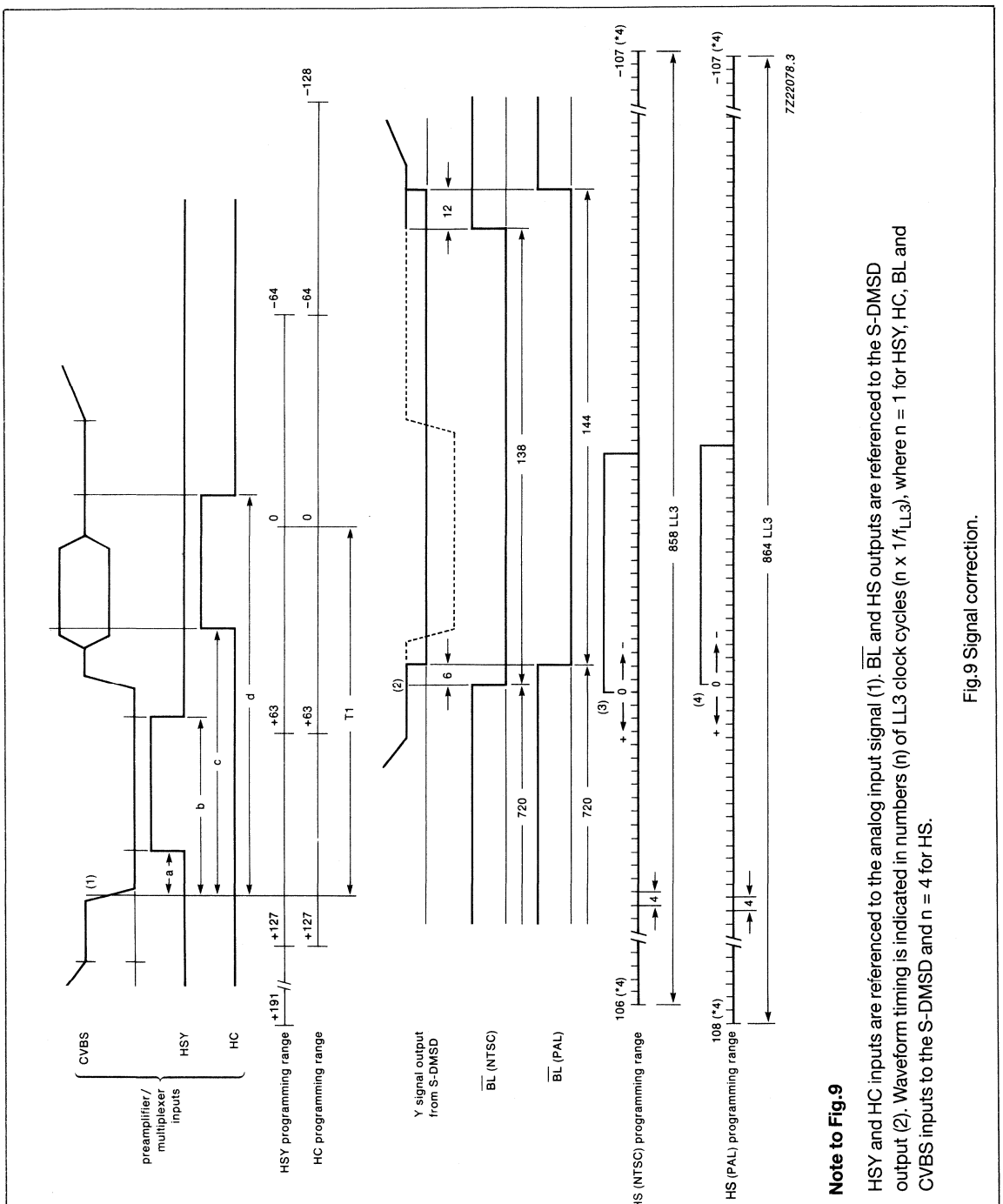


Fig.9 Signal correction.

Note to Fig.9

HSY and HC inputs are referenced to the analog input signal (1). $\overline{BL}$ and HS outputs are referenced to the S-DMSD output (2). Waveform timing is indicated in numbers (n) of LL3 clock cycles (n x $1/f_{LL3}$), where n = 1 for HSY, HC, BL and CVBS inputs to the S-DMSD and n = 4 for HS.

Programming of the luminance path of the S-DMSD

The VBS (without chrominance) or CVBS input signal enters the prefilter (a high-pass transfer function with maximum amplification of 9.5 dB). The control bit PF switches the filter into the bypass mode. The next stage is the chrominance trap which can be programmed (zero point) to 4.43 MHz (PAL) or 3.58 MHz (NTSC) by the control bit YPN. Bit BY activates the bypass function for the YUV mode of the S-DMSD. The chrominance trap output signal is then divided into three channels:

- Channel 1 signal; The channel 1 signal is transmitted to the programmable bandpass filter where the high luminance frequencies are removed, the centre frequency is programmable via bits BP1 and BP2. The signal BC is transmitted to the coring (corner correction) stage where low amplitude noise is removed, the amount of low amplitude noise removal is programmable via bits COR1 and COR2. The signal HF is transmitted to the weighting stage and adding stage, see 'Combining channel 1 and channel 2 signals'.
- Channel 2 signal; The channel 2 signal is transmitted to the fixed delay compensation stage where delay compensation and black level adjustment occurs. The signal DCA is transmitted to the weighting and adding stage, see section 'Combining channel 1 and channel 2 signals'.
- Combining Channel 1 and Channel 2 signals; The channel 1 signal HF is weighted, programmable via bits AP2 and AP1 and added to the Channel 2 signal DCA. The combined signals are matched to the specified amplitude and the word size is reduced to 7-bits. The signal AVD is transmitted to the variable delay compensation stage where compensation for IF group delays occurs, the amount of delay is programmable (from –4 to +3 LL3 clock cycles, see note) via bits YDL0 – YDL2. The signal Y is transmitted to the time multiplexed interface where the signal is output via D1 – D7.

Note

Differences in the delay compensation required for PAL and NTSC are catered for by identification signal YPN which switches the chrominance trap to the appropriate colour-carrier frequency 3.58 MHz or 4.43 MHz.

- Channel 3 signal; The channel 3 signal VB is transmitted to the pre-filter synchronization stage, see section 'Synchronization path'.

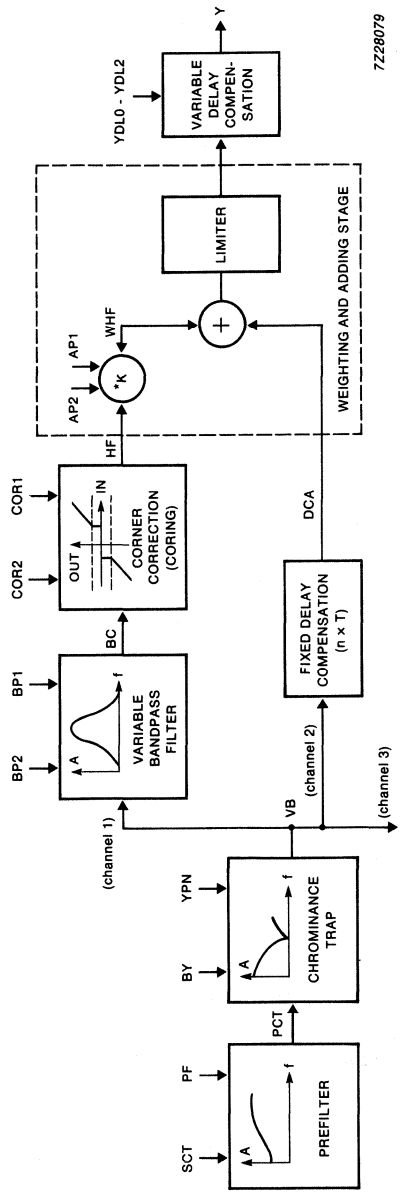


Fig.10 Luminance path of the S-DMSD.

SUBADDRESS 06

Table 13 Chrominance trap select (BY switches the chrominance trap to the bypass mode; YPN selects the notch-frequency)

PREFILTER	CONTROL BITS	
	BY	YPN
PAL (4.43 MHz)	0	0
NTSC (3.58 MHz)	0	1
bypass	1	X

Table 14 Disconnecting the luminance prefilter (user dependent)

PREFILTER	CONTROL BIT PF
ON	0
OFF	1

Table 15 Bandpass control (BP1 and BP2 control the centre frequency of the bandpass filter, see Figs 12 to 15)

BANDPASS TYPE (CENTRE FREQUENCY)	CONTROL BITS	
	BP2	BP1
type 1 (4.1 MHz)	0	0
type 2 (3.8 MHz)	0	1
type 3 (2.6 MHz)	1	0
type 4 (2.9 MHz)	1	1

Table 16 Coring threshold level (COR1 and COR2 control the suppression of low amplitude and high frequency signal components, see Fig.11)

THRESHOLD	CONTROL BITS	
	COR2	COR1
coring off	0	0
coring on (–8 to 7 LSB)	0	1
coring on (–16 to 15 LSB)	1	0
coring on (–32 to 31 LSB)	1	1

Note to Table 16

The thresholds are related the word width of the bandpass filter (12 bits).

Table 17 Aperture correction factor (AP1 and AP2 select the weighting factor K of the high frequency (HF) luminance components, see Fig.10)

WEIGHTING FACTOR K	CONTROL BITS	
	AP2	AP1
0.	0	0
0.25	0	1
0.5	1	0
1.	1	1

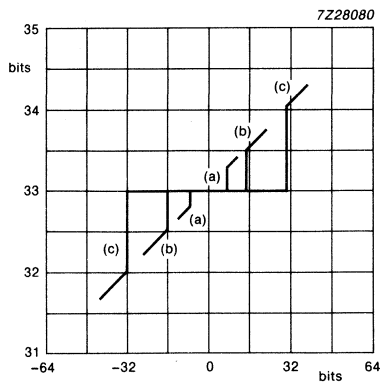


Fig.11 Coring stage response; (a) for COR2 = 0 and COR1 = 1; (b) for COR2 = 1 and COR1 = 0; (c) for COR2 = 1 and COR1 = 1.

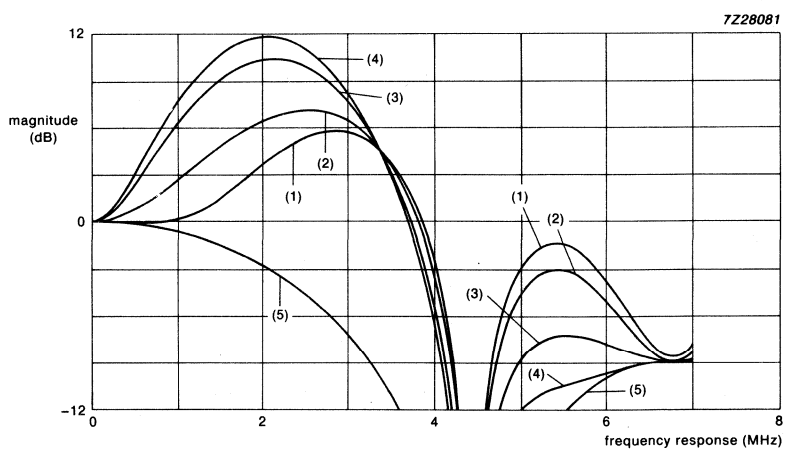


Fig.12 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); PAL mode; prefilter OFF; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

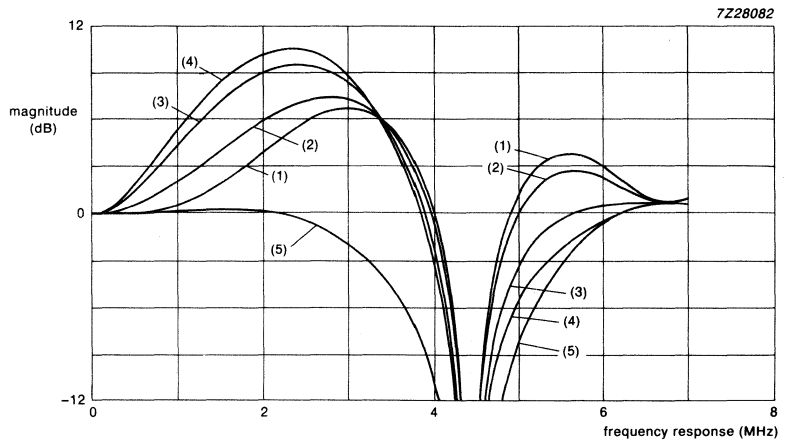


Fig.13 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); PAL mode; prefilter ON; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

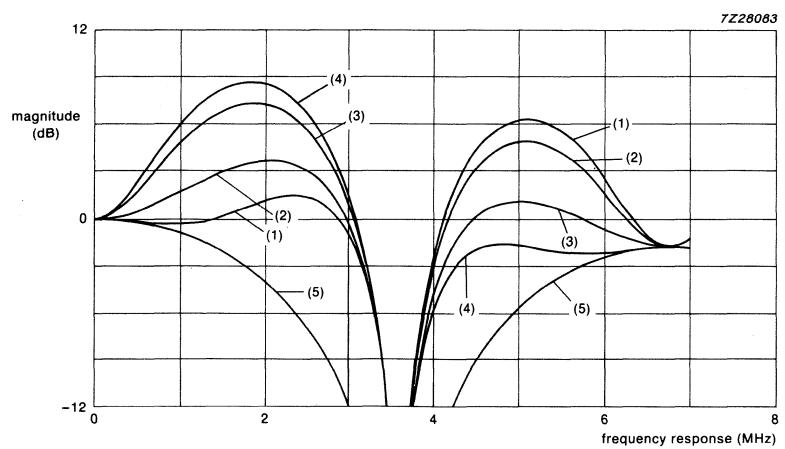


Fig.14 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); NTSC mode; prefilter OFF; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

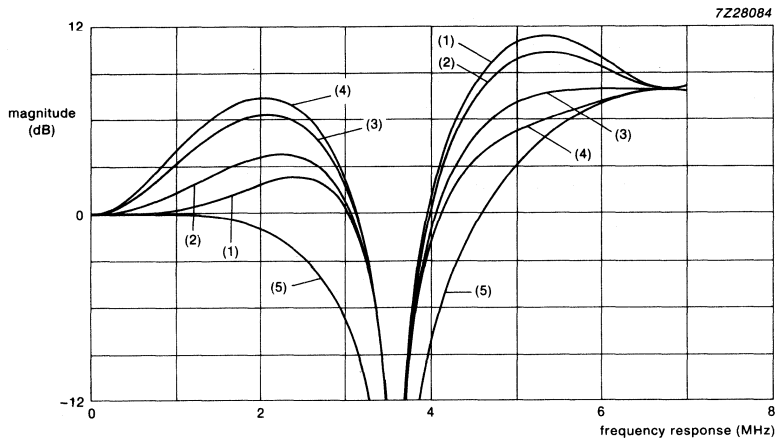


Fig.15 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); NTSC mode; prefilter ON; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

SUBADDRESS 07

Table 18 Hue phase (user dependent, see notes 1 to 3)

HUE PHASE (deg)	CONTROL BITS							
	A77	A76	A75	A74	A73	A72	A71	A70
+ 178.6 to 0	1	1	1	1	1	1	1	1
0.	1	0	0	0	0	0	0	0
0. to −180	0	0	0	0	0	0	0	0

Notes to Table 18

1. Step size per least significant bit (A70) = 1.4 degree.
2. Reference point for positive colour difference signals = 0 degree.
3. The hue phase may be shifted ±180 degrees from the reference point using bit A77, the colour difference signals are then switched from normally positive to negative polarity.

SUBADDRESS 08

Table 19 Horizontal clock PLL (application dependent)

FUNCTION	HPLL CONTROL BIT
horizontal clock PLL open, horizontal frequency fixed	1
horizontal clock PLL closed	0

Table 20 Field frequency select (system mode dependent)

FUNCTION	CONTROL BIT FS
60 Hz; 525-line mode	1
50 Hz; 625-line mode	0

Table 21 VTR/TV mode select (system mode dependent)

FUNCTION	CONTROL BIT VTR
VTR mode	1
TV mode	0

Table 22 Colour on control (system mode dependent)

FUNCTION	CONTROL BIT CO
colour ON	1
colour OFF (all colour output samples zero)	0

Table 23 Alternate/non–alternate mode (system mode dependent)

FUNCTION	CONTROL BIT ALT
alternate mode (PAL)	1
non-alternate mode (NTSC)	0

Table 24 Chrominance trap select and amplitude matching (system mode dependent)

CHROMINANCE TRAP	CONTROL BIT YPN
3.58 MHz	1
4.43 MHz	0

Table 25 Colour carrier frequency control (system mode dependent)

COLOUR CARRIER FREQUENCY	CONTROL BITS	
	CCFR1	CCFR0
4 433 618.75 Hz (PAL-B, G, H, 1; NTSC 4.43)	0	0
3 575 611.49 Hz (PAL-M)	0	1
3 582 056.25 Hz (PAL-N)	1	0
3 579 545 Hz (NTSC-M)	1	1

SUBADDRESS 09

Table 26 Synchronization output enable (system mode dependent)

FUNCTION	CONTROL BIT OES
outputs HS and VS active	1
outputs HS and VS HIGH-impedance Z-state	0

Table 27 Y-output enable (system mode dependent)

FUNCTION	CONTROL BIT OEY
outputs D0 – D6 and $\overline{BL}$ active	1
outputs D0 – D6 and $\overline{BL}$ HIGH-impedance Z-state	0

Table 28 Chrominance output enable (system mode dependent)

FUNCTION	CONTROL BIT OEC
outputs UV0 – UV3 active; if CD = logic 1, chrominance signal output; if CD = logic 1, zero signal	1
outputs UV0 – UV3 HIGH-impedance Z-state	0

Table 29 Internal colour forced ON/OFF (test purposes only)

FUNCTION	CONTROL BIT CI
colour forced ON, if CO = logic 1 (CD = X) or colour OFF, if CO = logic 0 (CD = X)	1
colour OFF, if CO = logic 0 (CD = X) or colour controlled by CD, if CO = logic 1	0

Where:

X = don't care.

Table 30 Additional output for circuit control

FUNCTION	CONTROL BIT AFCC
output AFCC = HIGH	1
output AFCC = LOW	0

Table 31 Source-select (system mode dependent)

FUNCTION	CONTROL BIT SS0 – SS3
output SS0 – SS3 = HIGH	1
output SS0 – SS3 = LOW	0

Note to Table 31

SS2 and SS3 are part of subaddress 0A.

SUBADDRESS 0A

Table 32 Disabling of HSY and HC pulses (system mode dependent)

FUNCTION	CONTROL BIT SYC
HYS and HC output pulses disabled	1
HSY and HC output pulses enabled	0

Table 33 Chrominance input/output 3-state control

FUNCTION	CONTROL BIT CT
CVBS output active	1
output HIGH-impedance Z-state	0

Table 34 Chrominance source select

FUNCTION	CONTROL BIT YC
Y/C separate inputs	1
CVBS input	0

Table 35 Variable delay compensation of the luminance path (YDL0 – YDL2 control the luminance delay in order to compensate different chrominance delays throughout the system)

DELAY (N =)	CONTROL BITS		
	YDL2	YDL1	YDL0
0	0	0	0
+ 1	0	0	1
+ 2	0	1	0
+ 3	0	1	1
– 4	1	0	0
– 3	1	0	1
– 2	1	1	0
– 1	1	1	1

Note to Table 35

The delay is given in terms of clock cycles:

- 13.5 MHz = N x 74 ns.

SUBADDRESS 0B

Table 36 SECAM chrominance delay compensation (system mode dependent)

PROGRAMMABLE DELAY*	CONTROL BITS						
	SCDC6	SCDC5	SCDC4	SCDC3	SCDC2	SCDC1	SCDC0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.
4	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.
8	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.
16	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.
32	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.
63	0	1	1	1	1	1	1
64	1	1	1	0	0	0	0
65	1	1	1	0	0	0	1
.	.	.	.	.	.	.	.
79	1	1	1	1	1	1	1
Maximum delay selected by single control bit							
	16	32	16	8	4	2	1

* Delay in number of LL3 clock cycles.

SLAVE TRANSMITTER ORGANIZATION

Slave transmitter format

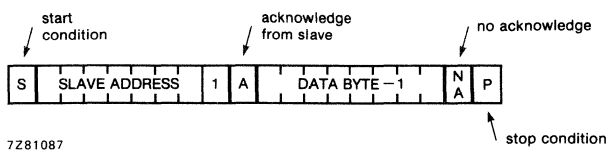


Fig.16 Slave transmitter format (a general call address is not acknowledged).

Note to Fig.16

Data bits D0, D3 and D5 are inverted in slave transmitter byte.

The format of data byte 1 is:

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	HLOCK	1	FD	0	CD	CS	0

Table 37 Description of data byte 1

BIT	DESCRIPTION
PONRES	Status bit for power-on-reset ($\overline{RES}$) and after a power failure. logic 1 after the first power-on-reset and after a power failure. Also set to logic 1 after a severe voltage dip that may have disturbed slave receiver data in the PAL/NTSC decoder (SAA9050). PONRES sets all data bits of control registers 1 and 2 to zero. logic 0 after a successful read of the PAL/NTSC decoder status byte
HLOCK	Status bit for horizontal frequency lock (transmitter identification, stop or mute bit): logic 1 if horizontal frequency is not locked (no transmitter available); logic 0 if horizontal frequency is locked (transmitter received)
FD	Detected field frequency status bit: logic 1 when received signal has 60 Hz synchronization pulses; logic 0 when received signal has 50 Hz synchronization pulses
CD	PAL/NTSC colour-detected status bit: logic 1 when PAL/NTSC colour signal is detected; logic 0 when no PAL/NTSC colour signal is detected
CS	SECAM colour-detected status bit: logic 1 when SECAM colour signal is detected; logic 0 when no SECAM colour signal is detected.

Default coefficients set for the S-DMSD and SAA9056

The default coefficients are set for operation with the TDA8703 or TDA8708, these devices are analog-to-digital converters with built-in sample rate converter. The 3-state outputs of the chrominance ADC are controlled by the SS3 switch in this example (all numbers are hex values).

The slave addresses are as follows:

- S-DMSD; 8A or 8E
- SAA9056; 8A or 8E

Table 38 Slave address (SAA9051 part)

SUBADDRESS	FUNCTION	SHORT DELAY	LONG DELAY
00	inc. delay	5E	7E
01	HSY start	37	73
02	HSY stop	07	43
03	HC start	F6	32
04	HC stop	C7	03
05	HS start	FF	FF
06	H-peaking	02	02
07	HUE control	00	00
08	control 1	38 (77 NTSC)	38 (77 NTSC)
09	control 2	E3	E3 (D3 SECAM)
0A	control 3	58 (28 YUV mode)	58 (28 YUV mode)
0B	SECAM delay	00	3C

Notes to Table 38

1. Subaddress 05; application dependent.
2. Subaddress 08; HPLL is in the VTR mode. Hex value for TV mode is 18 (58 for NTSC).

Table 39 Slave address (SAA9056 part)

SUBADDRESS	FUNCTION	VALUE
10	luminance delay	C0 – FF
11	$\overline{BL}$ delay	00
12	burst gate start	42
13	burst gate stop	56
14	sensitivity	20
15	filter	24
16	control	00 (02 active)

Note to Table 39

Subaddress 16; set to 04 when used in conjunction with SAA9056 and the CS bit is to be transmitted in the horizontal blanking.

Table 40 Operating modes of the S-DMSD

INPUT	CT	YC	SS3	CE	SCDC	IDEL	YPN	BY	FS	ALT	CCFR1	CCFR0	REMARKS
PAL B, G, H, I													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	1	0	0	
YUV	0	1	0	0	A	A	0 (1)	1	0	1	0	0	
PAL M													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	1	0	1	1	0	1	
YUV	0	1	0	0	A	A	1 (0)	1	1	1	0	1	
PAL N													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	1	1	0	
YUV	0	1	0	0	A	A	0 (1)	1	0	1	1	0	
SECAM													
CVBS	1	0 (1)	1	1	B	B	0	0	0	0 (1)	0 (1)	0 (1)	
YUV	0	1 (0)	0	1	B	B	0 (1)	1	0	0 (1)	0 (1)	0 (1)	
NTSC 4.43 MHz													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	0	0	0	use FS = 1 for 60 Hz vertical frequency
YUV	0	1	0	0	A	A	0 (1)	1	1	0	0	0	use FS = 1 for 60 Hz vertical frequency
NTSC M													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	1	0	1	0	1	1	
YUV	0	1	0	0	A	A	1 (0)	1	1	0	1	1	

Where:

A = short time delay.
B = long time delay.

Notes to Table 40

1. SS3 is assumed to control the 3-state output of the chrominance ADC (active LOW).
2. To avoid data collision care must be taken with the programming of CT and SS3 (in this equal they are always equal).

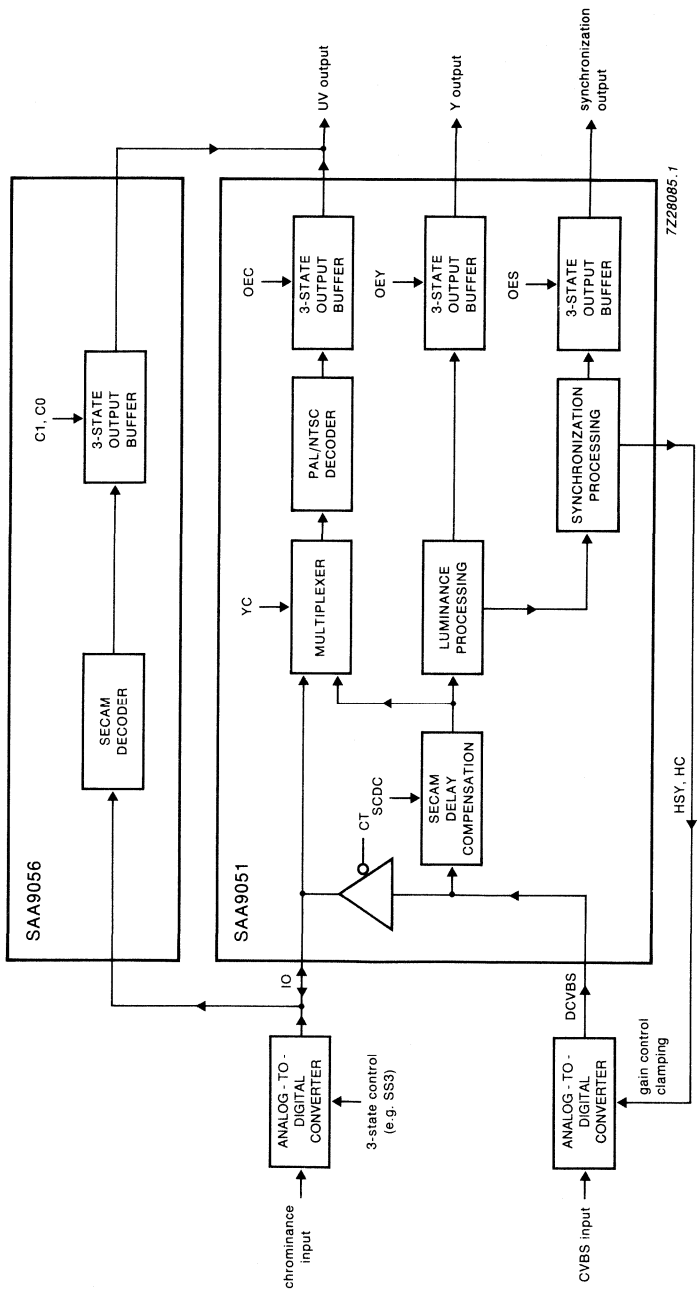
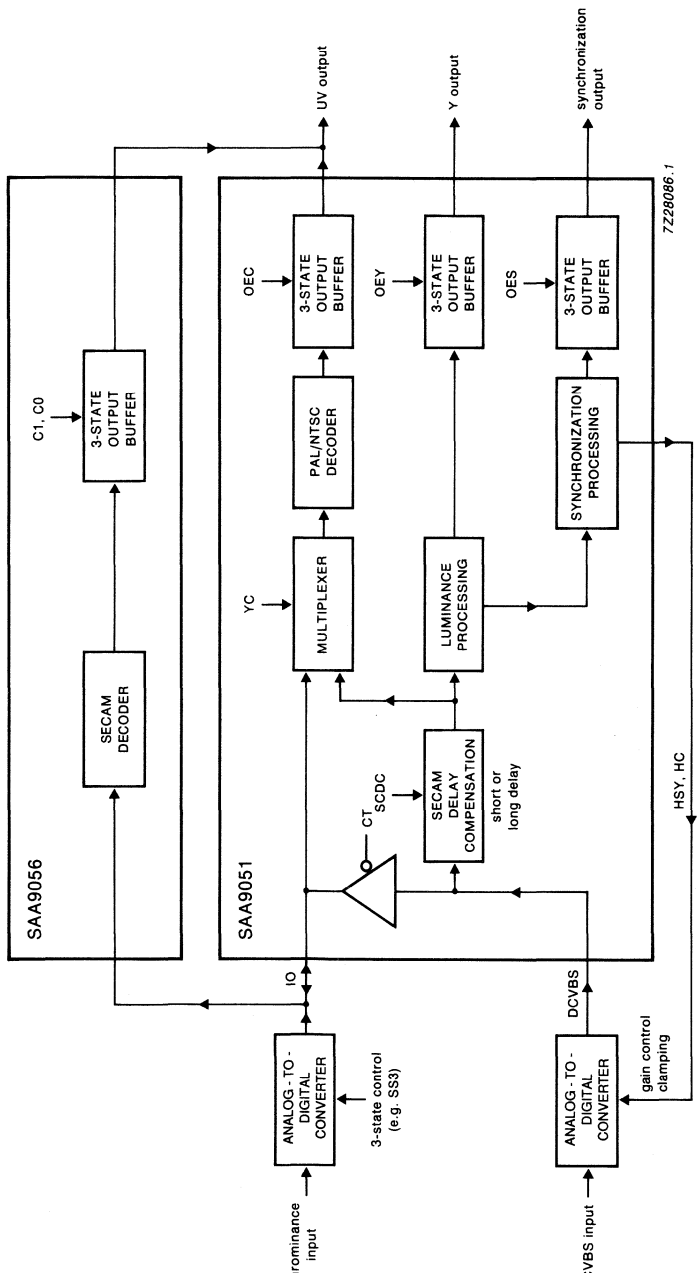
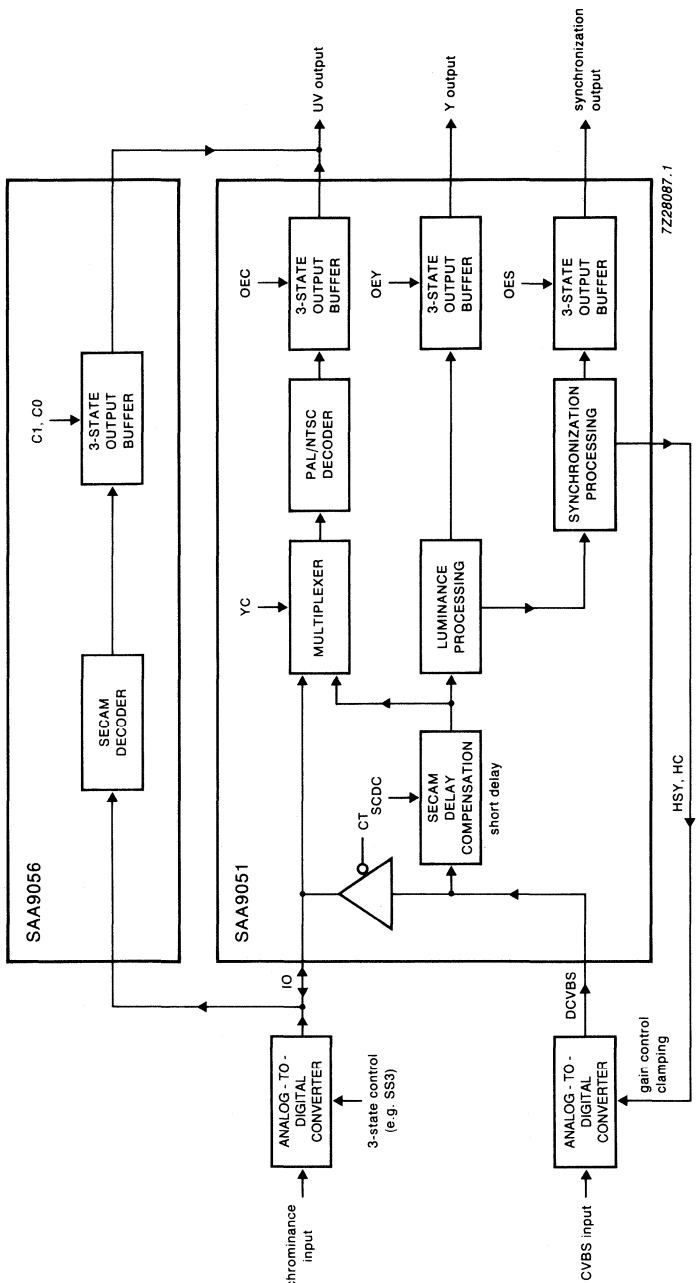


Fig.17 SAA9051 signal flow when used in conjunction with SAA9056.



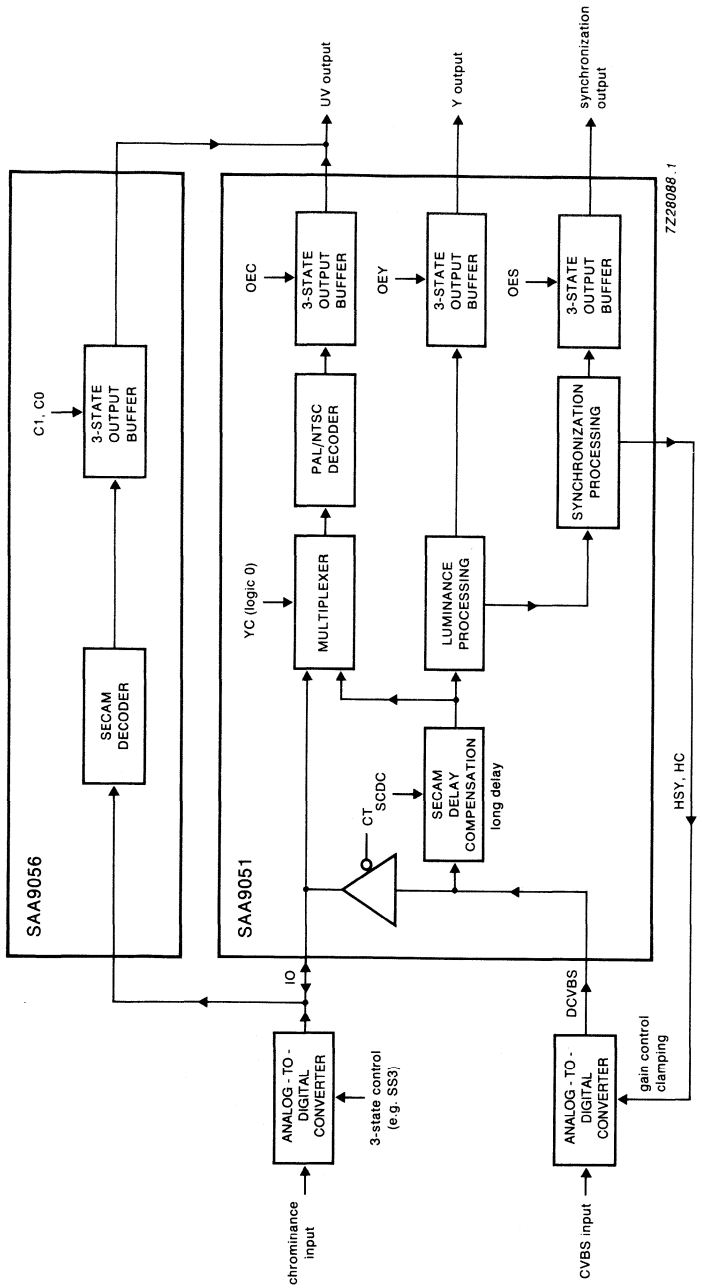
(a) PAL or NTSC with CVBS input signal.

Fig.18 Signal flow in different operating modes.



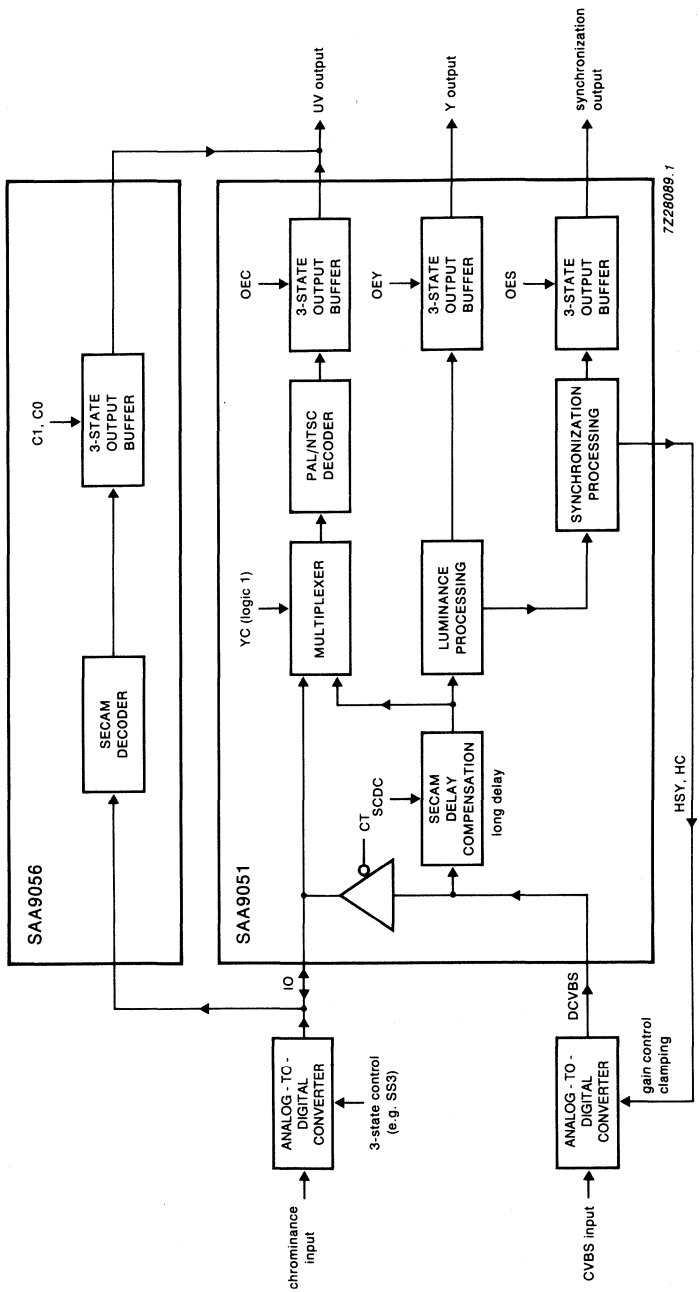
(b) PAL or NTSC with Y/C input signal.

Fig. 18 Signal flow in different operating modes.



(c) SECAM with CVBS input signal.

Fig.18 Signal flow in different operating modes.



(d) SECAM with Y/C input signal.

Fig.18 Signal flow in different operating modes.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage range		−0.5	+ 7.0	V
V_I	Input voltage range		−0.5	+ 7.0	V
V_O	Output voltage range	I_{Omax} = 20 mA	−0.5	+ 7.0	V
P_{tot}	Maximum power dissipation per package		-	3000	mW
T_{amb}	Operating ambient temperature range		0	+ 70	°C
T_{stg}	Storage temperature range		−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 4.5 V to 5.5 V; T_{amb} = 0 to +70 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	Supply voltage		4.5	5.0	5.5	V
I_{DD}	Supply current	note 1	-	380	550	mA
Inputs **Input voltage LOW**						
V_{IL}	pins 2 – 4, 6 – 17, 20 – 23, 43, 56 and 64		–0.5	-	+ 0.8	V
V_{IL}	pins 40 and 41		–0.5	-	+ 1.5	V
Input voltage HIGH						
V_{IH}	pins 2 – 3, 6 – 17, 20 – 23, 43, 56 and 64		2.0	-	V_{DD}	V
V_{IH}	pin 4		2.0	-	V_{DD}	V
V_{IH}	pins 34, 40 and 41		3.0	-	V_{DD}	V
Input leakage current						
I_I	pins 2 – 4, 6 – 17, 20 – 23, 40 – 41, 43 and 64		-	-	10	μA
Input capacitance						
C_I	pin 4		2	-	10	pF
C_I	pins 2 – 3, 14 – 17, 20 – 23, 43 and 64		2	-	7.5	pF
C_I	pins 6 – 13	HIGH-impedance Z-state	2	-	7.5	pF
Outputs **Output voltage LOW**						
V_{OL}	pins 6 – 13, 24 – 26, 29 – 32, 42, 45 -50, 53, 55 – 58, 65 – 66 and 68	I_{OL} = 2.0 mA	0	-	0.6	V
V_{OL}	pin 40 and 41	I_{OL} = 5.0 mA	0	-	0.45	V
Output voltage HIGH						
V_{OH}	pins 6 – 13, 24 – 26, 29 – 33, 42 and 45 – 50, 53, 55 – 58, 65 – 66 and 68	I_{OH} = –0.5 mA	2.2	-	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output capacitance						
C_O	pins 45 – 50, 53 and 55 – 58		-	-	7.5	pF
LFCO output (peak-to-peak value)						
$V_{o(p-p)}$	$R_L \geq 10$ kΩ; $C_L < 15$ pF		1	-	-	V
$V_{o(p-p)}$	$R_L \geq 1$ kΩ; $C_L < 15$ pF		0.5	-	-	V
Timing (see Fig.19)						
t_{C3}	LL3 cycle time		69	-	80	ns
t_{C3H}/t_{C3}	LL3 duty factor		43	-	57	%
t_r, t_f	LL3 rise and fall times	note 3	-	-	6	ns
$t_{SU;\ DAT}$	Input data set-up time		12	-	-	ns
$t_{HD;\ DAT}$	Input data hold time		5	-	-	ns
t_{HD}	Output data hold time		5	-	-	ns
t_D	Output data delay time	except HCY and HS; C_L = 25 pF; I_{OL} = 2.0 mA; V_{OH} = 2.2 V	-	-	50	ns
t_D	HCY and HS output delay time	C_L = 25 pF; I_{OL} = 2.0 mA; V_{OH} = 2.6 V	-	-	80	ns
C_L	Output data load capacitance		7.5	-	25	pF
Crystal oscillator (see Fig.20)						
f_n	Nominal frequency	third harmonic	-	24.576	-	MHz
$\Delta f/f_n$	Permissible deviation f_n		-	$\pm 50 \times 10^{-6}$	-	
$\Delta f/f_n$	Temperature deviation from f_n		-	$\pm 20 \times 10^{-6}$	-	
T_{XTAL}	Temperature range		0	-	+ 70	°C
C_{LXTAL}	Load capacitance		8	-	-	pF
R_r	Maximum resonance resistance		-	40	-	Ω
C_1	Motional capacitance		-	1.5 ±20%	-	fF
C_0	Parallel capacitance		-	3.5 ±20%	-	pF

Notes to the characteristics

1. Inputs LOW and outputs not connected, V_{DD} = 5 V.
2. 4-bit triangular waveform clocked at 24.576 MHz, AC coupled at pin 36.
3. Rising and falling edges of the clock signal are assumed to be smooth e.g. due to roll-off low-pass filtering.

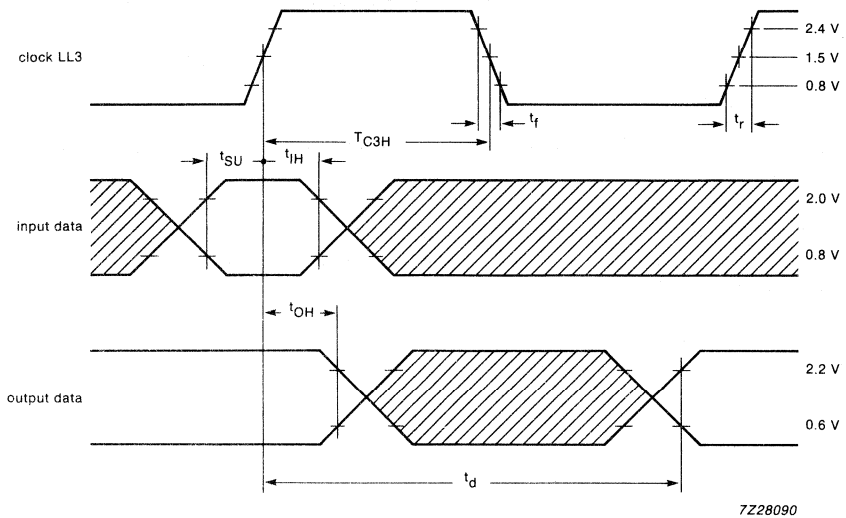


Fig.19 Timing diagram.

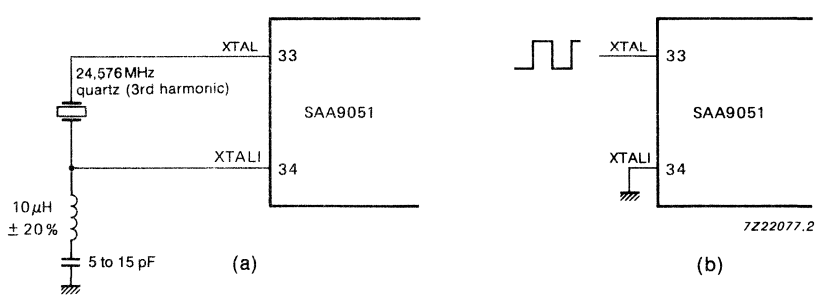


Fig.20 Oscillator circuit requirements; (a) with quartz crystal; (b) with external clock.

S-VHS DIGITAL SECAM DECODER (SDSD)

GENERAL DESCRIPTION

The SAA9056 is designed to provide colour difference signals for a digital TV signal processing system.

Features

- Phase-linear chrominance bandpass filter for cross-colour improvement
- Programmable filter characteristics for optimum adaption for different IF stages
- Recursive "Cloche" (Bell) filter
- Zero-crossing detection, FM demodulator with high AM rejection
- One demodulator for both carrier frequencies
- Base-band signal adjustment in gain and offset
- De-emphasis with recursive filter structure
- Line delay and cross-over switch for colour difference signals
- Output multiplexer for the UV format of the Digital Multistandard Secam Decoder
- Standard identification circuit with programmable sensitivity
- Programmable I^2C-bus address

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

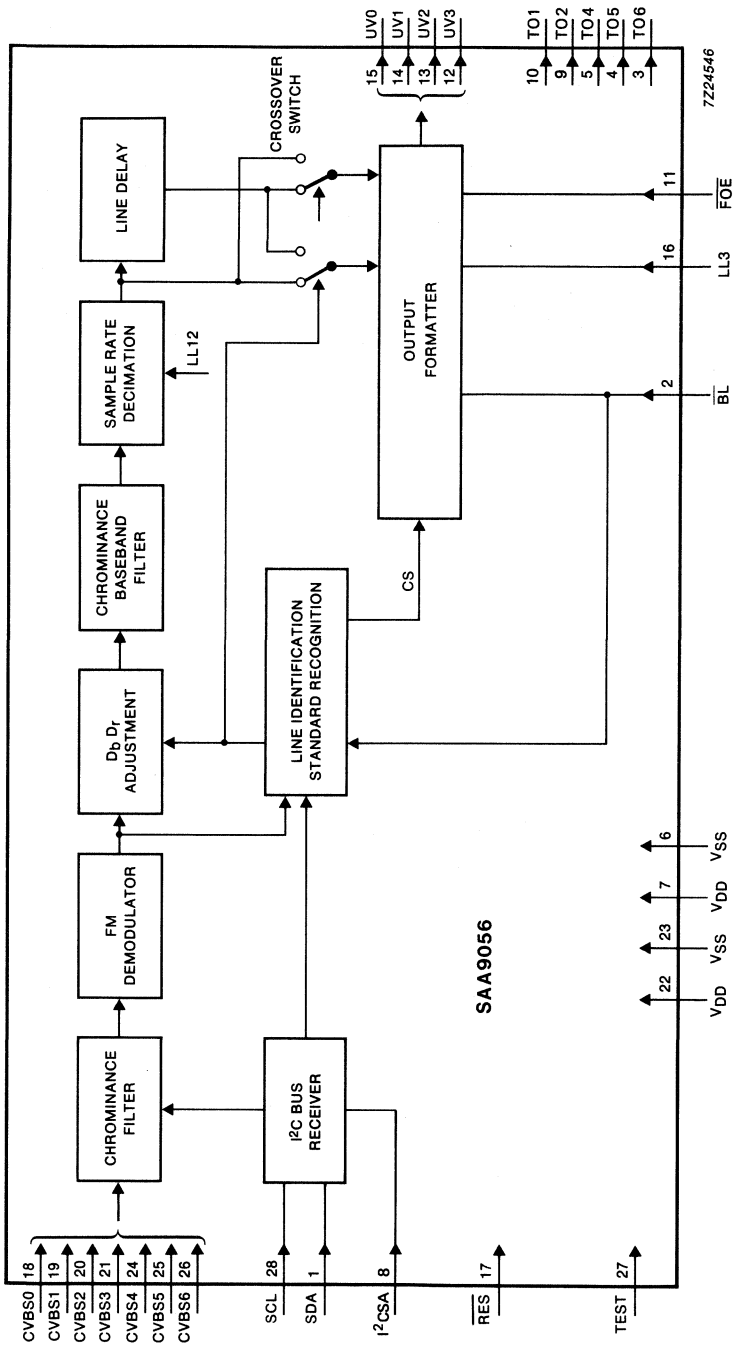


Fig. 1 Block diagram.

PINNING

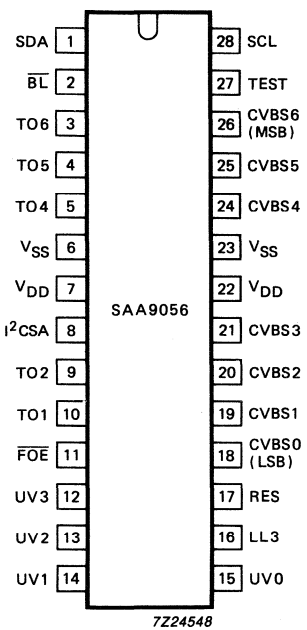


Fig.2 Pinning diagram.

1	SDA	I^2C-bus serial data input, receive only, no data is transmitted from the SDSD
2	$\overline{BL}$	This signal from the digital multistandard decoder indicates the active video and line blanking period
3	TO6	Test output pin, used during test mode only. Do not connect this pin
4	TO5	As pin 3
5	TO4	As pin 3
6	V_{SS}	Ground
7	V_{DD}	+ 5 V supply
8	I^2CSA	I^2C-bus select address. Input to select two different I^2C-bus slave addresses
9	TO2	As pin 3
10	TO1	As pin 3
11	$\overline{FOE}$	Fast output enable signal, forces the UV-outputs to High-Z state
12	UV3	UV colour difference signals, via this port the decoded colour difference signals are transmitted to the DMSD in a mixed parallel/serial format. Additionally the status flag CS (colour in SECAM detected) is encoded in the UV data stream. The output drivers can be set to high impedance (3-state) via the I^2C-bus.
13	UV2	As pin 12
14	UV1	As pin 12
15	UV0	As pin 12
16	LL3	LL3 is the line-locked system clock at 13.5 MHz
17	$\overline{RES}$	The reset signal (active LOW) disables the UV buffers. Minimum LOW-time on this input = 10 LL3-cycles
18	CVBS0	Composite video, blanking and synchronization (LSB) input
19	CVBS1	As pin 18
20	CVBS2	As pin 18
21	CVBS3	As pin 18
22	V_{DD}	As pin 7
23	V_{SS}	As pin 6
24	CVBS4	Composite video, blanking and synchronization
25	CVBS5	As pin 24
26	CVBS6	As pin 24 (MSB)
27	TEST	This signal (active HIGH) enables the scan test mode
28	SCL	I^2C-bus serial clock input

FUNCTIONAL DESCRIPTION

The S-VHS Digital SECAM Decoder (SDSD) forms an integral part of a digital TV signal processing system. The system incorporates a Video Processor and Input Selector (TDA9045), an A/D Converter (SAA9079), a Sample Rate Converter (SAA9058), a Digital Multi-Standard Decoder with separate chrominance and luminance input (SAA9051), a Digital Deflection Controller (SAA9062/3/4)*, a Clock Generator Circuit (SAA9057), a Video Processor with DACs (SAA9060), a Colour Transient Improvement Circuit (TDA4565), a Video Control Combination Circuit (TDA4580), and an Octuple 6-bit DAC and a Feature Box. Figure 9 illustrates the timing of the input and output signals relative to the input clock (LL3).

The S-DMSD (SAA9051) decodes and demodulates the colour information from all TV standards which employ a quadrature modulated colour carrier. The S-DMSD also processes the luminance and synchronization signals and generates auxiliary signals.

The SDSD separates the colour information which it demodulates and decodes to provide the colour difference signals. These signals are subsequently encoded to produce a serial/parallel data stream at the UV outputs. Figure 4 illustrates the formatting and timing of the UV output port.

To enable other sources (eg PIP-CO) to access the digital YUV-bus, a fast output enable signal ($\overline{FOE}$) is provided. Two LL3-cycles after the $\overline{FOE}$ becomes inactive (HIGH), the UV output port of the SDSD is forced to the High-Z state. When the $\overline{FOE}$ signal is active (LOW) again, it needs two LL3-cycles and the UV output port of the SDSD becomes active (see Fig.4).

The chrominance bandpass filter for separating the frequency modulated colour carrier consists of several phase-linear FIR filters which improve the cross-colour behaviour. The non-linear phase (Bell) filter has a recursive structure (IIR filter). Figure 3 illustrates the frequency response of the chrominance band-pass filter and Bell filter. One of the FIR filters can be programmed via the I^2C-bus to provide optimal adaption for the various IF stages. Different responses can be selected by means of a 7-bit control word. Figure 8 illustrates some examples of frequency responses of the programmable adaptive filer.

Only one FM demodulator is used to demodulate the chrominance signal; this accomodates both carrier frequencies regardless of the centre frequency. It is a zero-crossing demodulator with a real time divider which is a pipeline structure. After demodulation the baseband signal is adjusted, line sequentially, to the appropriate colour difference signal. During the clamping period, the demodulated reference carrier is compared with the previous reference signal by the line identification circuit. The identification circuit compares the phase of the two demodulated burst signals and, if the phase relationship is incorrect for several lines (not SECAM), the CS flag (colour in SECAM) will be reset.

The baseband filter consists of a linear phase low-pass filter together with a de-emphasis filter with a recursive structure. Figure 5 illustartes the frequency response of the de-emphasis and band-pass filters for the colour difference signals. After filtering, the sample rate is reduced to a quarter (LL12 = 3.375 MHz). The word length is truncated to seven bits. The resultant signal is delayed by one line period (64 μs = 216 clock periods of 3.375 MHz). The signals, delayed and non-delayed, can be switched either directly or cross-wise to two different outputs which correspond to the colour difference signals.

The cross-over switch is controlled by the line identification circuit. At the end of the chrominance path an output formatter transforms the 14 bits (2 x 7 bits clocked by 3.375 MHz) to a 4-bit wide channel which is clocked by 13.5 MHz (LL3). The bits are separated into odd and even and then serialized.

* The digital TV signal processing system has the option of using one of three Digital Deflection Controllers (SAA9062/3/4). The choice of DDC is dependent on the format of the CRT and the line/field frequency.

The format for the UV output is the same as that of the UV I/O port in the S-DMSD (SAA9051). The timing multiplexer is controlled by the external signal $\overline{BL}$ from the S-DMSD. Signal $\overline{BL}$ is also used as a line-locked synchronization signal to generate several internal burst gate pulses.

The CS flag is transmitted via the chrominance data-stream because the SDSD has no I^2C-bus transmitter. The CS bit is read once per line by the S-DMSD at LL3 clock cycle number 748 (see Fig.6). If no SECAM colour is detected the UV port will be set to zero. After reset the UV lines will be set to high impedance (3-state) and the SDSD must be re-initialized via the I^2C-bus to enable further operation.

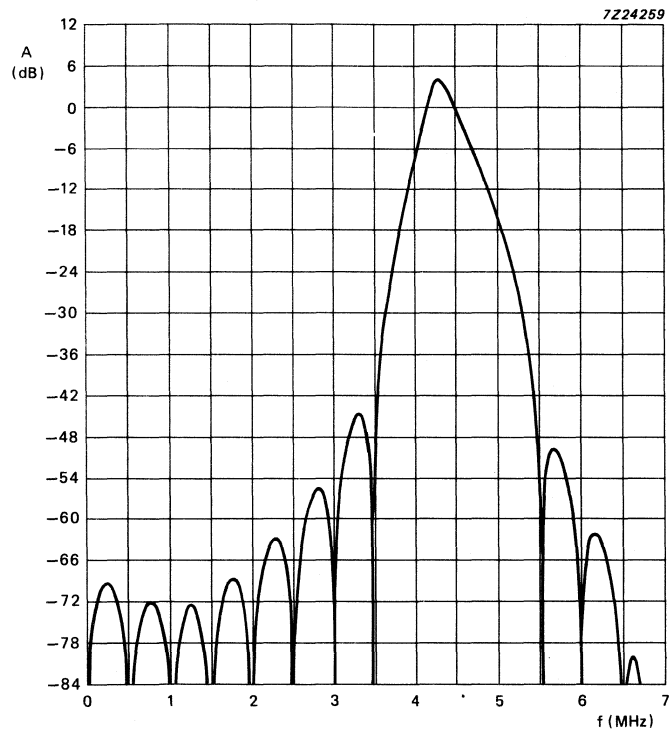


Fig. 3 Frequency response of chrominance bandpass and Bell filter.

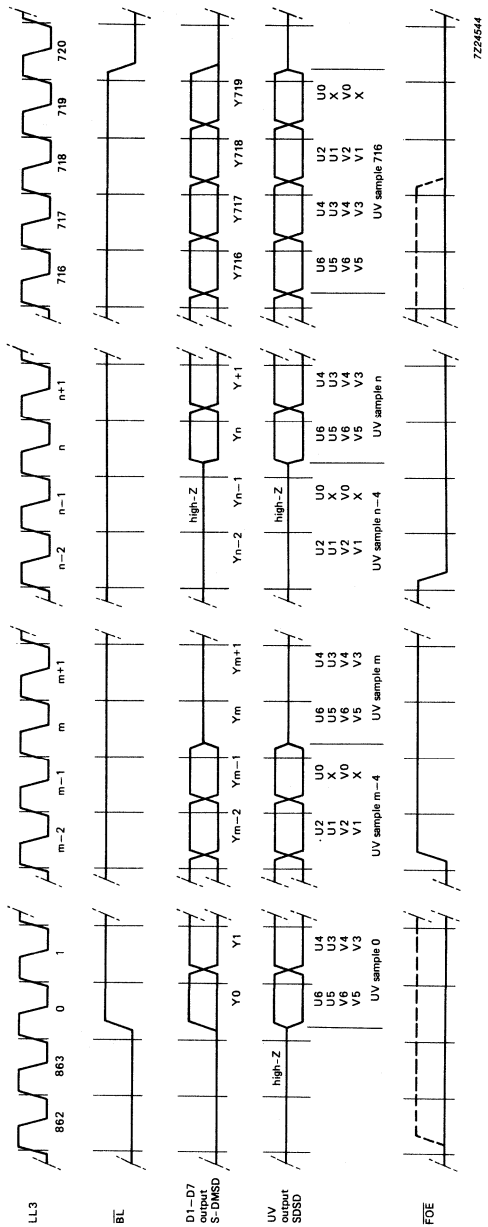


Fig.4 Timing of $\overline{FOE}$ signal.

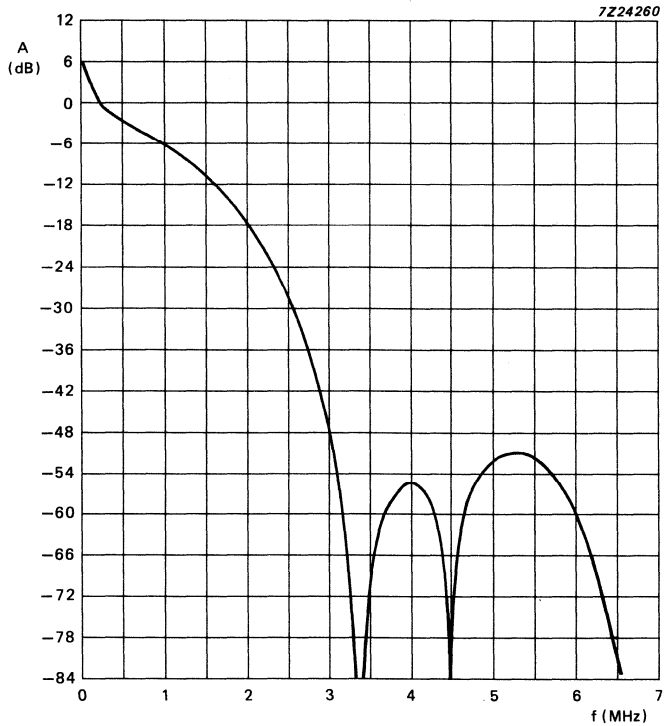
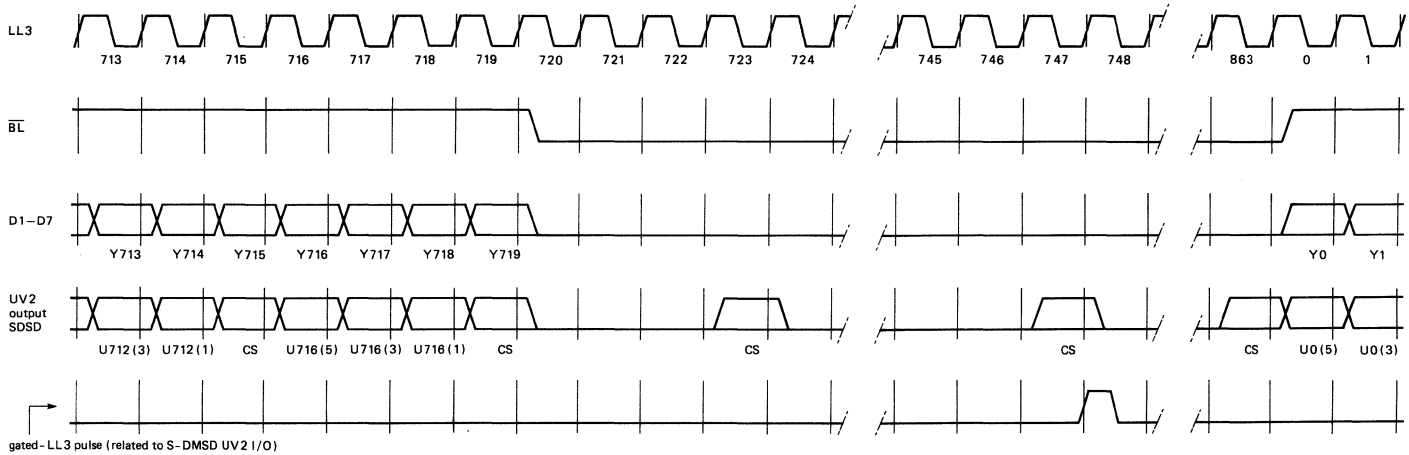
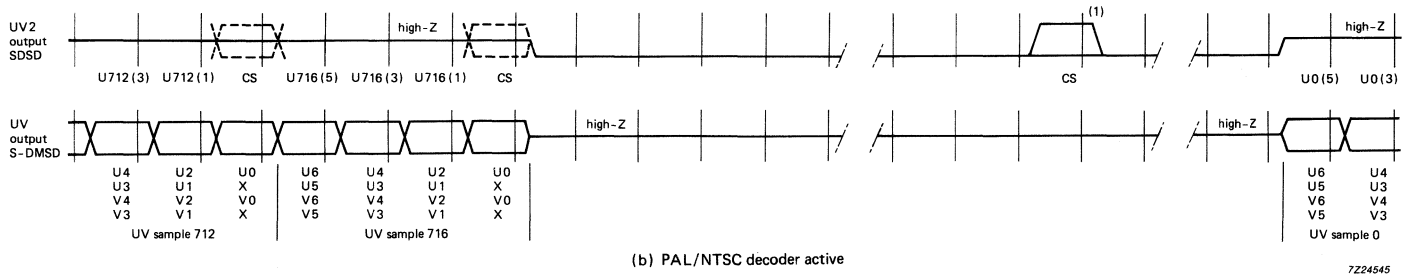


Fig. 5 Frequency response of the de-emphasis and base-band filter for the colour difference signals.

DEVELOPMENT DATA



(a) SECAM decoder active



(b) PAL/NTSC decoder active

7Z24545

(1) The CS signal is active only for ± 64 clock pulses (LL3) around the gate pulse.

Fig.6 Position of CS signal read by S-DMSD.

I²C-BUS PROTOCOL

Slave receiver organization

Two different slave addresses are programmable with the I²CSA input at pin 8

I²CSA	slave receiver addresses							
	A6	A5	A4	A3	A2	A1	A0	*)
0 or unconnected	1	0	0	0	1	0	1	0 (bin) = 8A (hex)
1	1	0	0	0	1	1	1	0 (bin) = 8E (hex)

*) 0 = receiver mode

Fig. 7 Slave receiver format.

Table 1 Subaddress definition

register function	subaddress (HEX)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Main counter start address (MA9..... MA0)	10	MA1	MA0	X	DT4	DT3	DT2	DT1	DT0
	11	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2
Burst gate begin	12	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Burst gate end	13	BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0
Standard recognition sensitivity	14	R7	R6	R5	R4	R3	R2	R1	R0
Programmable adaptive filter	15	X	P6	P5	P4	P3	P2	P1	P0
Control register	16	X	X	X	X	X	C2	C1	C0
Reserved	17–1F	X	X	X	X	X	X	X	X

Notes to Table 1

1. The subaddress is automatically incremented to enable quick initialization by the I²C-bus controller within one transmission.
2. All eight bits of the subaddress are decoded by the device.
3. The subaddresses shown are acknowledged by the device. Subaddresses 00 to 0F (reserved for the Digital Multi-Standard Decoder) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.
4. X = don't care.
5. After power-on-reset the control register (subaddress 16) is set to logic 0, all other registers are undefined.

Subaddress 10 and 11 (HEX)

Main counter start address.

Application dependent.

MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	delay time	
0	1	1	1	1	1	1	1	1	1	+511	outside central counter range
–										–	
–										–	
–										–	
–										–	
0	1	1	0	1	0	0	0	1	0	+418	
0	1	1	0	1	0	0	0	0	1	+417	417 x 74 ns ≈ +31 μs (maximum positive value)
–										–	
–										–	
–										–	
0	0	0	0	0	0	0	0	0	1	+1	+74 ns
0	0	0	0	0	0	0	0	0	0	0	reference point*

* Reference point position to be fixed.

MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	delay time	
1	1	1	1	1	1	1	1	1	1	–1	–74 ns
–										–	
–										–	
–										–	
1	0	0	1	0	0	0	0	1	0	–446	–446 x 74 ns ≈ –33 μs (maximum negative value)
1	0	0	1	0	0	0	0	0	1	–447	outside central counter range
–										–	
–										–	
–										–	
–										–	
1	0	0	0	0	0	0	0	0	0	–512	

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

Internal counter range: –446 to + 417

Subaddress 12 (HEX)

Burst gate begin (start time)

Application dependent.

BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0	dec	delay time
0	0	0	0	0	0	0	0	0	zero reference point
0	0	0	0	0	0	0	1	1	74 ns
—	—	—	—	—	—	—	—	—	
—	—	—	—	—	—	—	—	—	
1	1	1	1	1	1	1	1	255	18.89 μs

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

Subaddress 13 (HEX)

Burst gate end (stop time)

Application dependent.

BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0	dec	delay time
0	0	0	0	0	0	0	0	0	zero reference point
0	0	0	0	0	0	0	0	1	74 ns
—	—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—
1	1	1	1	1	1	1	1	255	18.89 μs

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

The stop time must be greater than the start time.

The reference point position of the burst gate start/stop time is identical with the main counter zero position.

Subaddress 14 (HEX)

Standard recognition sensitivity

Application dependent

R7	R6	R5	R4	R3	R2	R1	R0	function
								relationship between the number of line identification errors related to a window of 312 lines
0	0	0	0	0	0	0	0	0 : 312 theoretical highest sensitivity
0	0	0	0	0	0	0	1	1 : 312
0	0	0	1	1	0	0	1	25 : 312
1	1	1	1	1	1	1	1	255 : 312 theoretical lowest sensitivity

For programmed numbers from 0 to approximately 25 (dec) the colour signal is switched off. With the value 25 (dec) the colour signal will be enabled only when extremely good signal quality is present. If the colour signal quality is reduced, i.e. VCR signal source, bad S/N ratio, bad quantization, diminished colour carrier and insufficient IF adaption, the sensitivity should be set lower (higher programmed number up to 255 (dec) in order to prevent excessive switching and thus ensure constant colour.

Subaddress 15 (HEX)

Programmable adaptive filter PAF (P6–P0)

Application (IF stage) dependent

The programmable adaptive filter, together with the cloche and linear bandpass filter, forms a filter-curve that treats the chrominance frequency spectra with different gain but linear phase. The frequency characteristic is a system of sinusoidal waveforms which are described by:

- Reference "knots" of constant gain (0 dB)
- Frequency points ("tops") with maximum gain
- The amount of maximum gain
  (There is also a switchable pre-amplifier in another stage of the bandpass filter).

The components of the PAF can be programmed via the I^2C-bus by using device address 8A (or 8E) and subaddress 15 thereby producing 57 different transfer functions. An example of some transfer functions is given in Figure 8 (a) to (d).

MSB	P6	P5	P4	P3	P2	P1	P0	function			
								maximum gain at tops			
–	X	X	X	X	1	1	1	19 dB			
–	X	X	X	X	1	1	0	14 dB			
–	X	X	X	X	1	0	1	9.5 dB			
–	X	X	X	X	1	0	0	6 dB			
–	X	X	X	X	0	1	1	3.5 dB			
–	X	X	X	X	0	1	0	2 dB			
–	X	X	X	X	0	0	1	1 dB			
–	X	X	X	X	0	0	0	0 dB			
								position of tops and knots (MHz)			
								top	knot	top	Figs 8a–d
–	X	1	1	1	X	X	X	3.375	4.5	5.625	+ A/dB (d)
–	X	1	1	0	X	X	X	4.5	5.625	6.75	–A/dB (d)
–	X	1	0	1	X	X	X	4.219	5.063	5.906	–A/dB (c)
–	X	1	0	0	X	X	X	3.375	4.219	5.063	+ A/dB (c)
–	X	0	1	1	X	X	X	4.05	5.4	6.75	–A/dB (b)
–	X	0	1	0	X	X	X	2.7	4.05	5.4	+ A/dB (b)
–	X	0	0	1	X	X	X	2.89	3.86	4.82	+ A/dB (a)
–	X	0	0	0	X	X	X	3.86	4.82	5.79	–A/dB (a)
								additional pre-amplification			
–	1	X	X	X	X	X	X	times two			
–	0	X	X	X	X	X	X	times one			
*	X	X	X	X	X	X	X	* MSB not used			

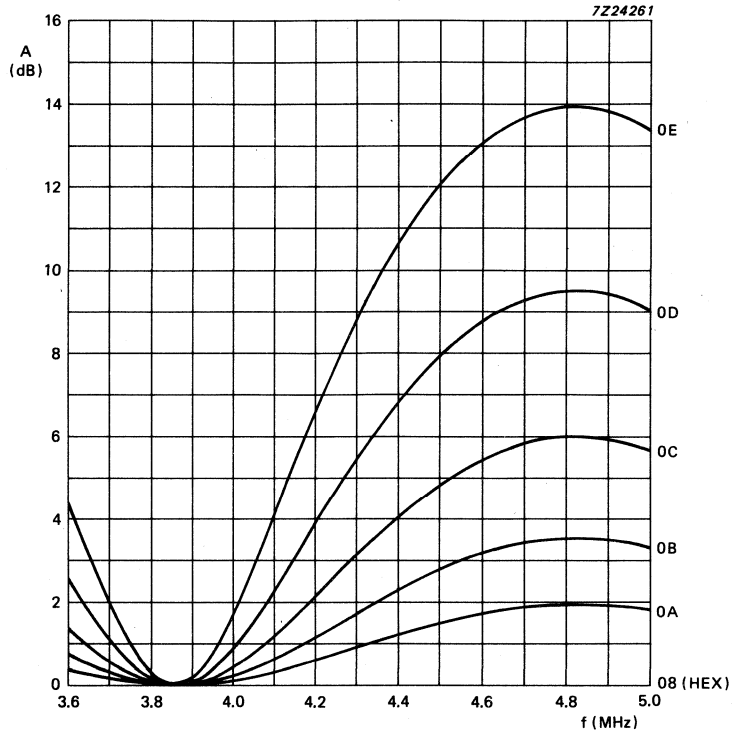


Fig. 8(a) Examples of frequency response for the programmable adaptive filter; from 08 to 0E (HEX).

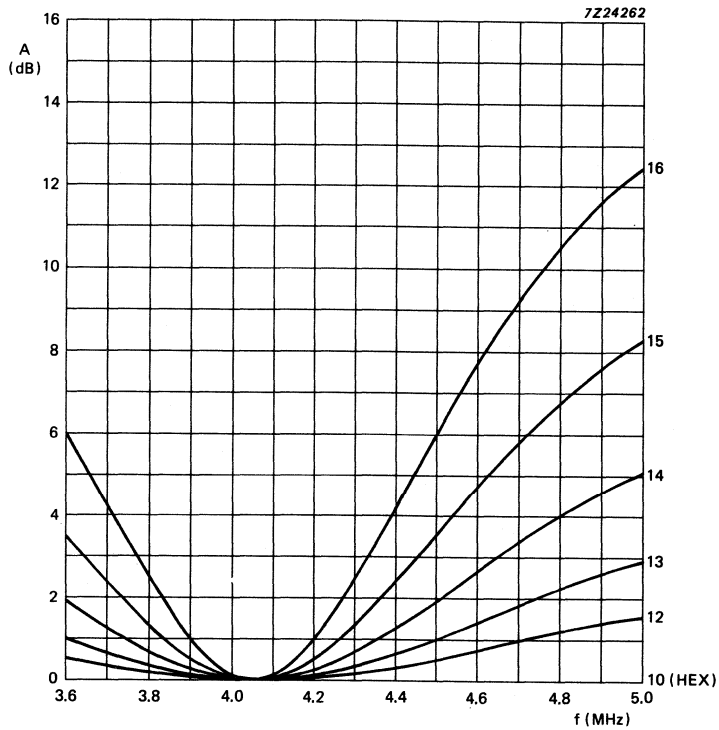


Fig. 8(b) Example of frequency response for the programmable adaptive filter; from 10 to 16 (HEX).

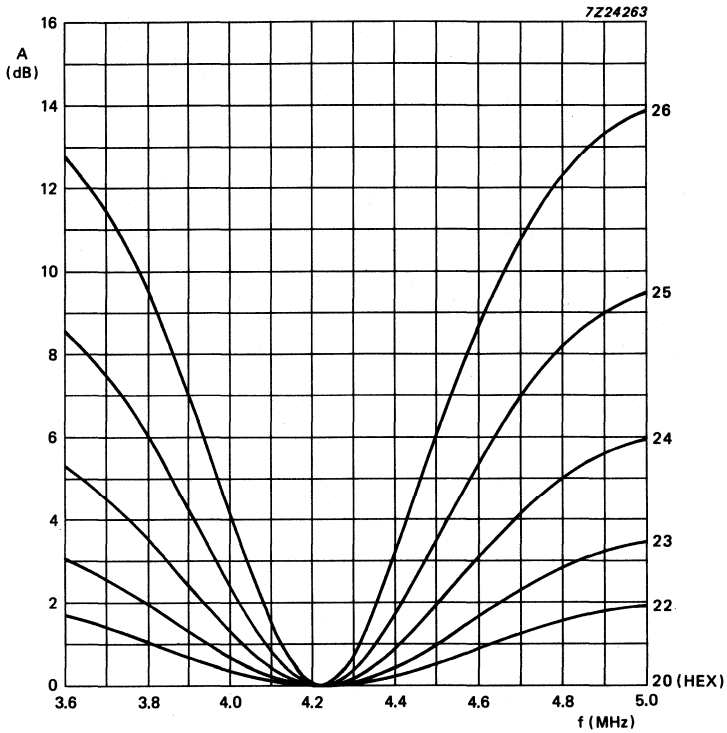


Fig. 8(c) Example of frequency response for the programmable adaptive filter; from 20 to 26 (HEX).

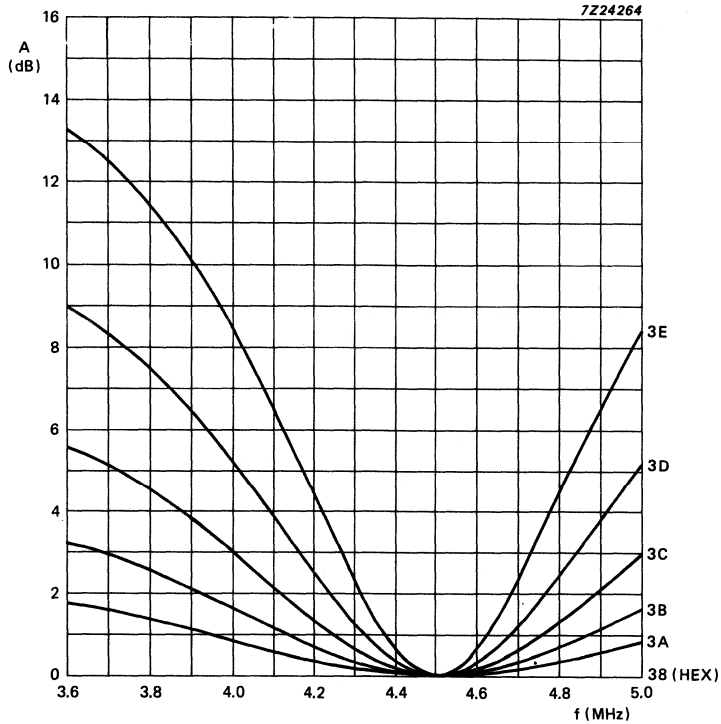


Fig. 8(d) Example of frequency response for the programmable adaptive filter; from 38 to 3E (HEX).

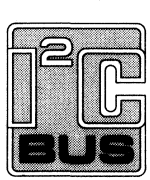
Subaddress 16 (HEX)

DSD control 3 register

C2	C1	C0	UV-output
X	0	1	active zero whole line
X	1	0	colour enable (if CS flag then colour on)
X	1	1	colour forced on (independent of CS flag)
0	X	X	positive UV
1	X	X	negative UV
0	0	0	3-state
1	0	0	UV2-output active during horizontal blanking period (CS-bit* transmission); high impedance in active line negative UV

After power-on reset the control register is set to logic 0.

* The position of the CS transmission is dependent on the start value of the main counter (Reg 10 and 11).



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.5	7.0	V
Voltage input		V_I	−0.5	7.0	V
Voltage output	I_{max} = 20 mA	V_O	−0.5	7.0	V
Total power dissipation		P_{tot}	−	1.2	W
Operating ambient temperature range		T_{amb}	0	70	°C
Storage temperature range		T_{stg}	−65	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified. All voltages are referenced to ground (pins 6 and 23) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	–	5.5	V
Supply current (f_{nom})	V_{DD} = 5.5 V					
Inputs LOW; outputs with maximum load		I_{DD}	–	–	180	mA
Inputs						
Input voltage LOW (clock data) pins 2, 16, 17 to 21; and 24 to 27		V_{IL}	0	–	0.8	V
Input voltage LOW (I^2C) pins 1 and 28		V_{IL}	0	–	1.5	V
Input voltage HIGH (data) pins 2, 17 to 21; and 24 to 27		V_{IH}	2	–	V_{DD}	V
Input voltage HIGH (LL3) pin 16		V_{IH}	2.4	–	V_{DD}	V
Input voltage HIGH (I^2C) pins 1 and 28		V_{IH}	3	–	V_{DD}	V
Input leakage current pins 1, 2, 12 to 21; and 24 to 27		I_{LI}	−10	–	+ 10	μA
Input current pins 8 and 11		I_I	−10	–	+ 60	μA
Input capacitance (data) pins 2, 18 to 21; and 24 to 27		C_I	2	–	7.5	pF
Input capacitance (clock) pin 16		C_I	5	–	10	pF
Input capacitance (reset) pin 17		C_I	2	–	10	pF
Outputs						
Output voltage LOW pins 3 to 5; 8 to 15	I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW SDA pin 1	I_{OL} = 5 mA	V_{OL}	0	–	0.45	V
Output voltage HIGH pins 3 to 5; 8 to 15	I_{OL} = −0.5 mA	V_{OH}	2.4	–	V_{DD}	V
Capacitive load of outputs in high impedance pins 12 to 15		C_Z	2	–	15	pF

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified. All voltages are referenced to ground (pins 6 and 23) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Clock timing (LL3)						
Cycle time	note 1	t_{C3}	69	–	80	ns
Duty factor		δ	43	–	57	%
Rise time	note 2	t_r	–	–	6	ns
Fall time	note 2	t_f	–	–	6	ns
Input timing						
Data set up time		t_{SU}	12	–	–	ns
Data hold time	note 3	t_{IH}	5	–	–	ns
Output timing						
Data load capacitance		C_L	7.5	–	50	pF
Data hold time	V_{IH}(CLK) = 3 V	t_{OH}	5	–	–	ns
Data delay time	C_L = 25 pF	t_{OD}	–	–	45	ns

Notes to the characteristics

1. Static deviation = ±2%; dynamic deviation = ±7% for signal path CVBS-DCVBS (this is required for the running-in of the DMSD sync processor).
2. The rising and falling edges of the clock signal are assumed to be smooth due to roll-off low-pass filtering.
3. Matches to SAA9058 for V_{IH}(LL3) ⩾ 3 V.

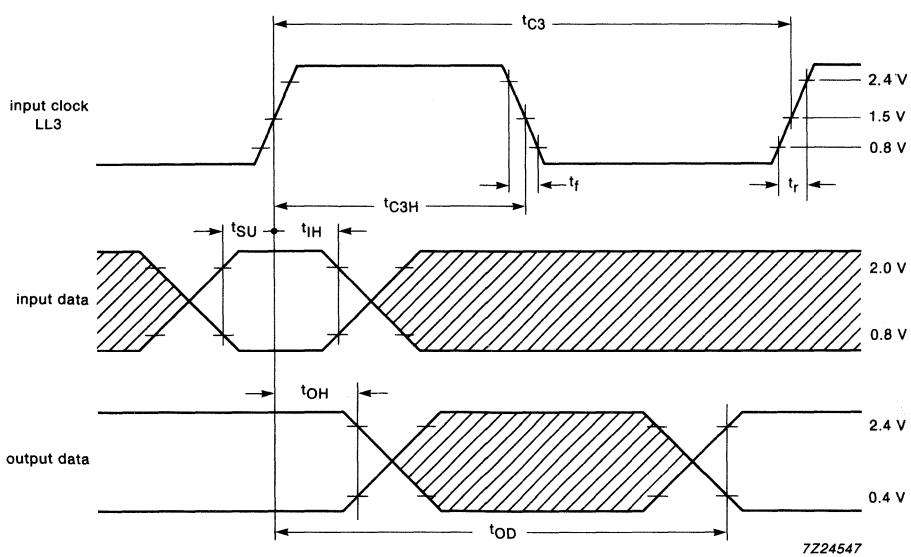


Fig. 9 Timing diagram.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1992

SAA9057B

Clock signal generator circuit for digital TV systems (CGC)

FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5, LL3 and LL3T (4th and 2nd multiples of input frequency)
- Reset control and power fail detection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	40	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.25	-	7.25	MHz
V_I	input voltage LOW input voltage HIGH	0 2.4	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA9057B generates all clock signals required for a digital TV system suitable for the SAA90xx family. Optional extras (feature box etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9057B	20	DIL	plastic	SOT146
SAA9057BT	20	mini-pack (SO20)	plastic	SOT163A

Clock signal generator circuit for digital TV systems (CGC)

SAA9057B

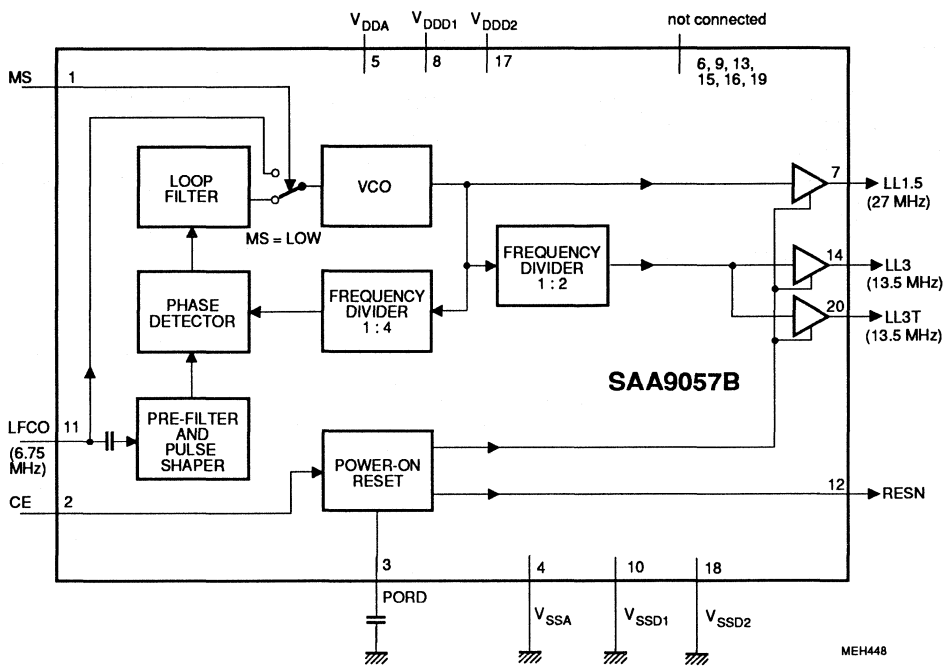


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA9057B generates all clock signals required for a digital TV system suitable for the SAA90xx family. Optional extras (feature box etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.
The 6.75 MHz input signal LFCO, coming from SAA 9051, is multiplied to 27 MHz by the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LL1.5 (pin7). 13.5 MHz frequency is also generated by 1:2 divider and output on LL3 and LL3T (pins 14 and 20).
The rectangular output signals have 50 % duty factor.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. MS function is not tested.

Chip enable CE

The buffer outputs are enabled and power-on reset is set to HIGH by CE = HIGH (Fig.4).
CE = LOW sets the clock outputs HIGH and RESN output LOW.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuit of this digital TV system.
The LFCO input signal has to be applied before RESN becomes HIGH.

Clock signal generator circuit for digital TV systems (CGC)

SAA9057B

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
n.c.	6	not connected
LL1.5	7	line-locked clock output signal (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
n.c.	9	not connected
V_{SSD1}	10	digital ground 1 (0 V)
LFCO	11	line-locked input frequency
RESN	12	reset output (active-LOW)
n.c.	13	not connected
LL3	14	line-locked clock output signal (2 times f_{LFCO})
n.c.	15	not connected
n.c.	16	not connected
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD2}	18	digital ground 2 (0 V)
n.c.	19	not connected
LL3T	20	line-locked clock output signal (2 times f_{LFCO})

PIN CONFIGURATION

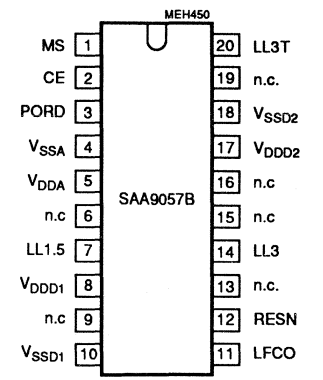


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	−0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	−0.5	V_{DDD}	V
P_{tot}	total power dissipation	0	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	tbf	V

* Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; $f_{LFCO} = 6.25$ to 7.25 MHz and $T_{amb} = 0$ to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	40	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		6.25	-	7.25	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS and CE (pins 1 and 2)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
I_{LI}	input leakage current		-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.4	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	-	V_{DDD}	V
I_{LI}	output leakage current		-	-	±10	µA
t_d	RESN delay time	$C_3 = 0.1$µF; Fig.4	20	-	200	ms
Output signals LL1.5, LL3 and LL3T (pins 7, 14 and 20)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.6	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.6	-	V_{DDD}	V
I_{LI}	output leakage current	high-impedance	-	-	±10	µA
t_{comp}	composite rise time	note 1; note 2	-	-	9	ns
f_{LL}	output frequency LL1.5	Figures 3 and 6	-	4 f_{LFCO}	-	MHz
	output frequency LL3		-	2 f_{LFCO}	-	MHz
	output frequency LL3T		-	2 f_{LFCO}	-	MHz
t_{LL}	duty factor LL1.5	note 1; Fig.3	40	50	60	%
	duty factor LL3 and LL3T	note 1; Fig.3	43	50	57	%
t_r, t_f	rise and fall times	note 1; Fig.3	-	-	6	ns

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF. V_{SSA} and V_{SSD} connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V.
3. MS function is not tested.

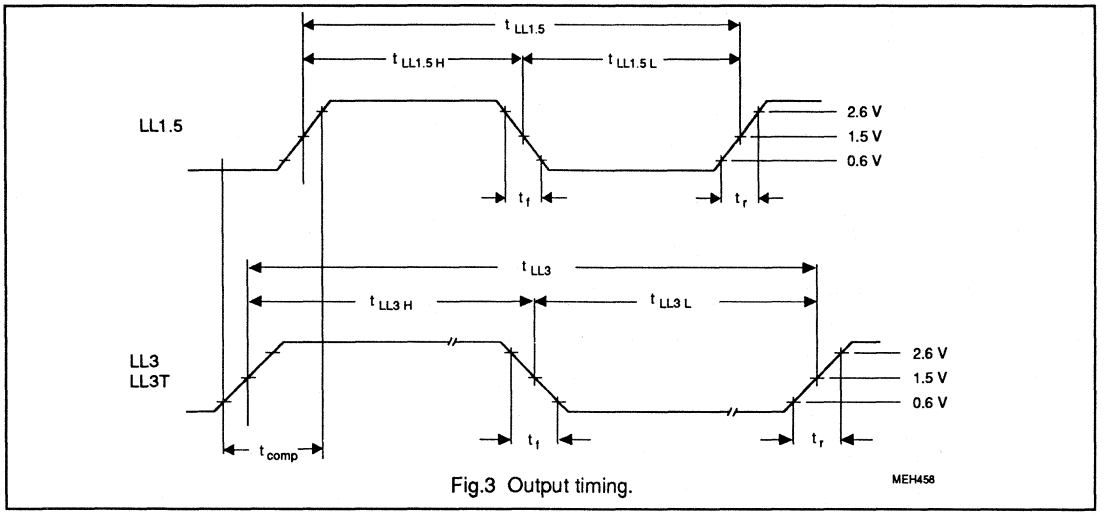


Fig.3 Output timing.

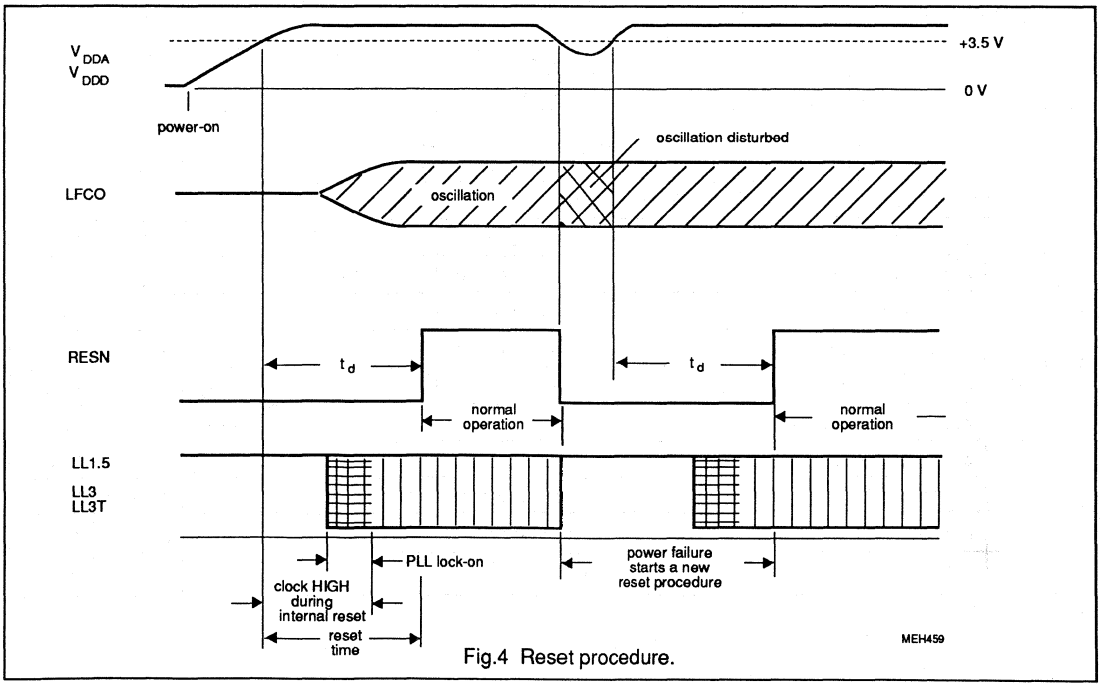
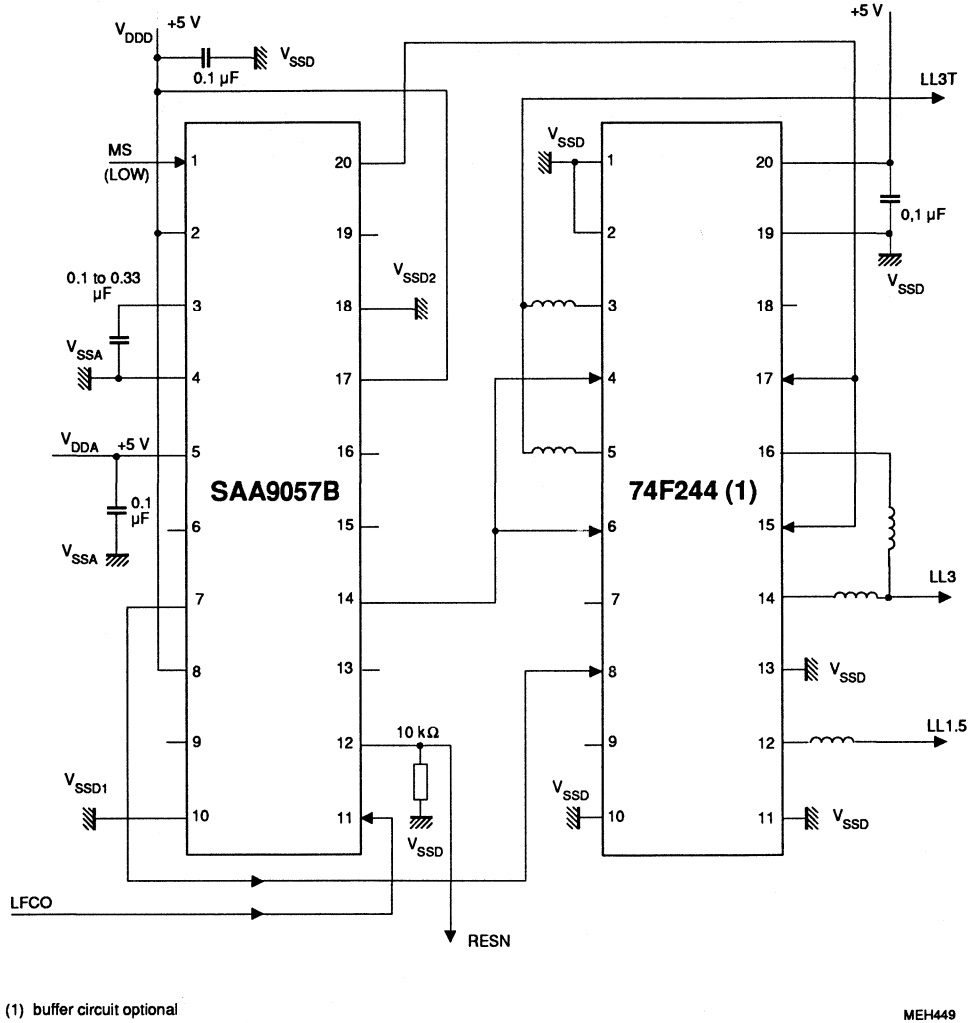


Fig.4 Reset procedure.



(1) buffer circuit optional

MEH449

Fig.5 Application circuit.

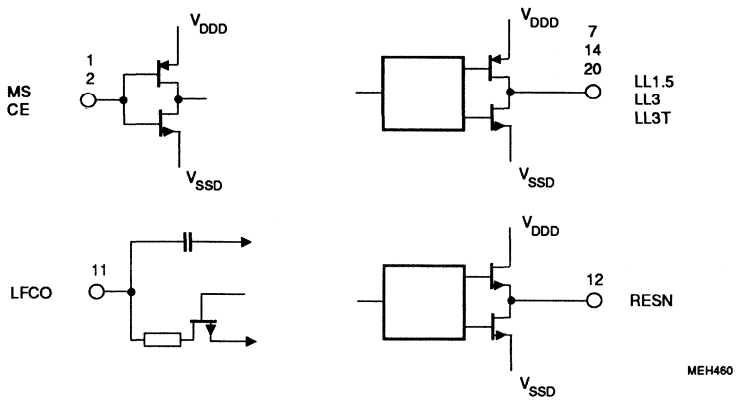


Fig.6 Internal circuit.

SAMPLE-RATE CONVERTER

GENERAL DESCRIPTION

The SAA9058 sample-rate converter (SRC) is for use in digital TV receiver applications. It converts the sampling rate of digital signals by a factor of 2/3, e.g. from 20,25 to 13,5 MHz, using a phase-linear, finite impulse response (FIR) filter with time-varying coefficients. Only two clocks are required; the data format is two's complement, and the word length at both input and output is seven bits.

The FIR filter creates a filter-algorithm to interpolate digitized composite video signals (DCVBS) into a slower sample rate that is suitable for video decoding. The circuit gives low attenuation of colour subcarrier, gives high rejection of aliasing components and has unity DC gain.

It is intended for use with the 7-bit analogue-to-digital converter PNA7509 and the digital multistandard decoder SAA9050, with DCVBS in PAL, NTSC or SECAM. Other applications are digital anti-aliasing filtering, rejection of harmonics caused by analogue-to-digital conversion and data reduction.

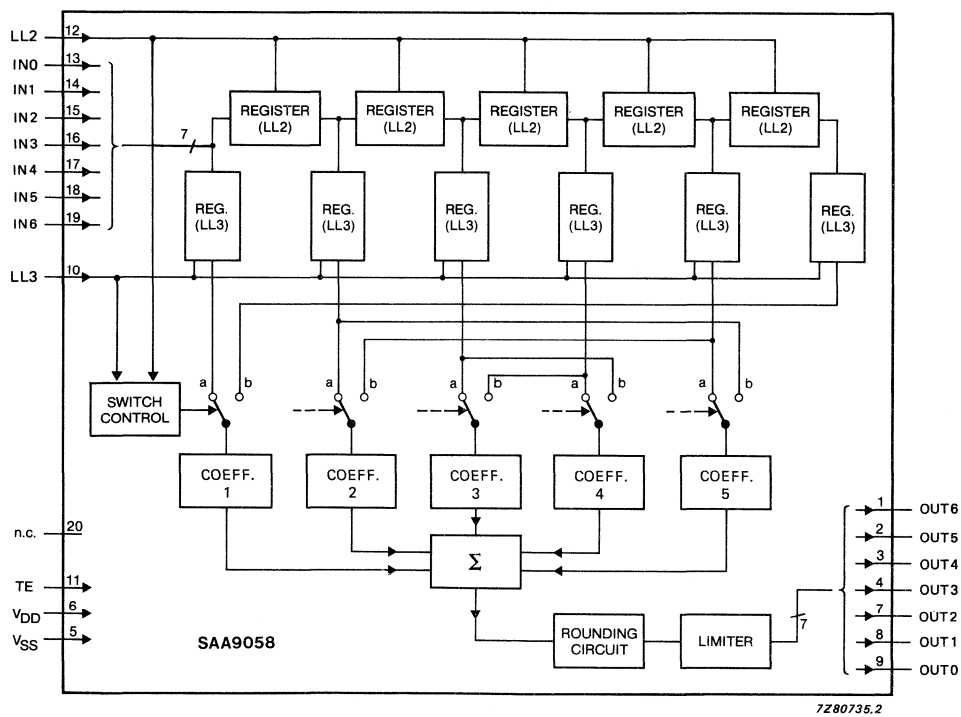


Fig. 1 Block diagram (see Fig. 3 for switch timing).

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

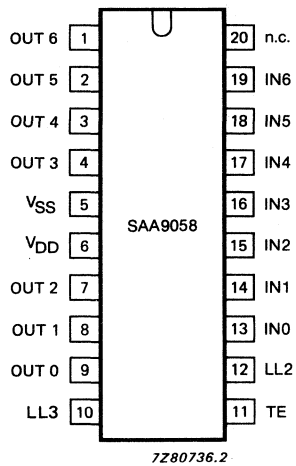


Fig. 2 Pinning diagram.

PINNING

1	OUT6	output data
2	OUT5	
3	OUT4	
4	OUT3	
5	V_{SS}	ground (0 V)
6	V_{DD}	positive supply voltage (+5 V)
7	OUT2	output data
8	OUT1	
9	OUT0	
10	LL3	output clock
11	TE	production test input; V_{SS} for all applications
12	LL2	input clock
13	IN0	input data
14	IN1	
15	IN2	
16	IN3	
17	IN4	
18	IN5	
19	IN6	
20	n.c.	not connected

OPERATION

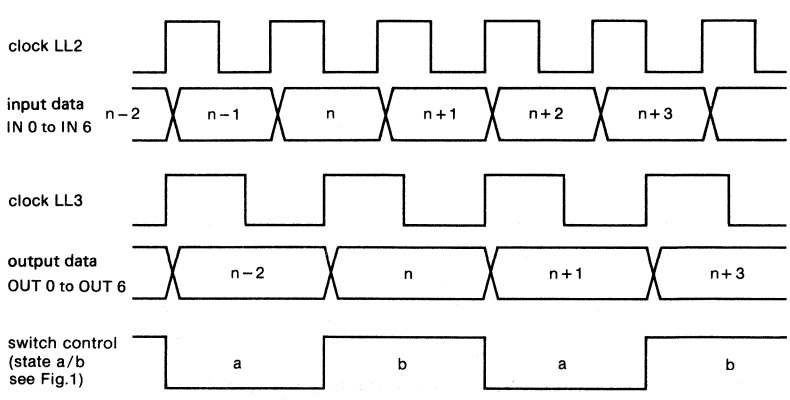


Fig. 3 Relationship of inputs to outputs.

Frequency response

The virtual frequency response in the 2 x LL2 (40,5 MHz) domain is interpreted as the characteristic of the interpolation filter directly before conversion to the LL3 (13,5 MHz) sample rate and the spectral components beyond LL3/2 are aliased into the baseband.

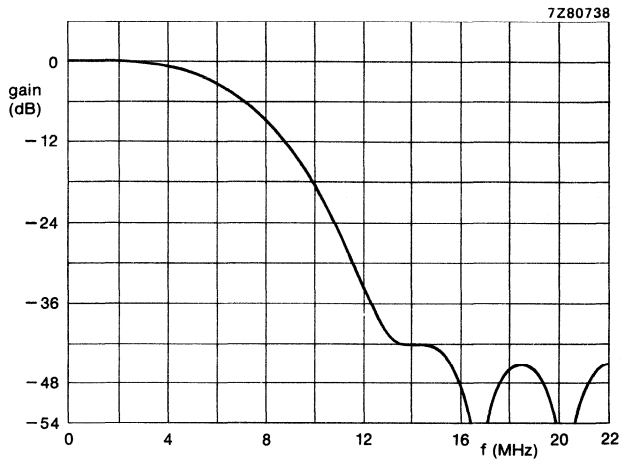


Fig. 4 Frequency response.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 7 V
Input voltage range	V_I	−0,5 to + 7 V
Output voltage range to $I_{O\,max}$ = 20 mA	V_O	−0,5 to + 7 V
Maximum power dissipation	P_{tot}	0,5 W
Operating ambient temperature range	T_{amb}	0 to + 70 °C
Storage temperature range	T_{stg}	−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

T_{amb} = 0 to +70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	5,0	5,5	V
Supply current at V_{DD} = 5,5 V, data outputs not connected, data inputs LOW and frequency nominal	I_{DD}	–	< 100*	65	mA
Inputs					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH (except LL2, LL3)	V_{IH}	2,0	–	V_{DD}	V
Input voltage HIGH (LL2, LL3)	V_{IH}	2,4	–	V_{DD}	V
Input leakage current	I_I	–	–	10	μA
Input capacitance (LL2)	C_I	–	–	10	pF
Input capacitance (LL3)	C_I	–	–	10	pF
Input capacitance (D0 to D6)	C_I	–	–	5	pF
Outputs					
Output voltage HIGH at I_{OH} = –0,5 mA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OH} = 2,0 mA	V_{OL}	0	–	0,6	V
Timing (Fig. 5)					
LL2 cycle time	t_{C2}	46	–	53	ns
LL2 duty factor t_{C2H}/t_{C2}	–	45	–	55	%
LL2 rise and fall time	t_r, t_f	–	–	6**	ns
LL3 cycle time	t_{C3}	69	–	80	ns
LL3 duty factor t_{C3H}/t_{C3}	–	45	–	55	%
LL3 rise and fall time	t_r, t_f	–	–	6**	ns
Skew time	t_{skew}	–2	–	+ 2	ns
Input data set-up time	t_{SU}	12	–	–	ns
Input data hold time	t_{HD}	3	–	–	ns
Output data load capacitance	C_L	7,5	–	15	pF
Output data hold time	t_{OH}	3	–	–	ns
Output data delay time	t_{OD}	–	–	33	ns

* For digital TV application.

** Difference between t_r, t_f of LL2 and t_r, t_f of LL3 shall be less than 2 ns. Rising and falling edges of clocks are assumed to be smooth due to low pass filtering.

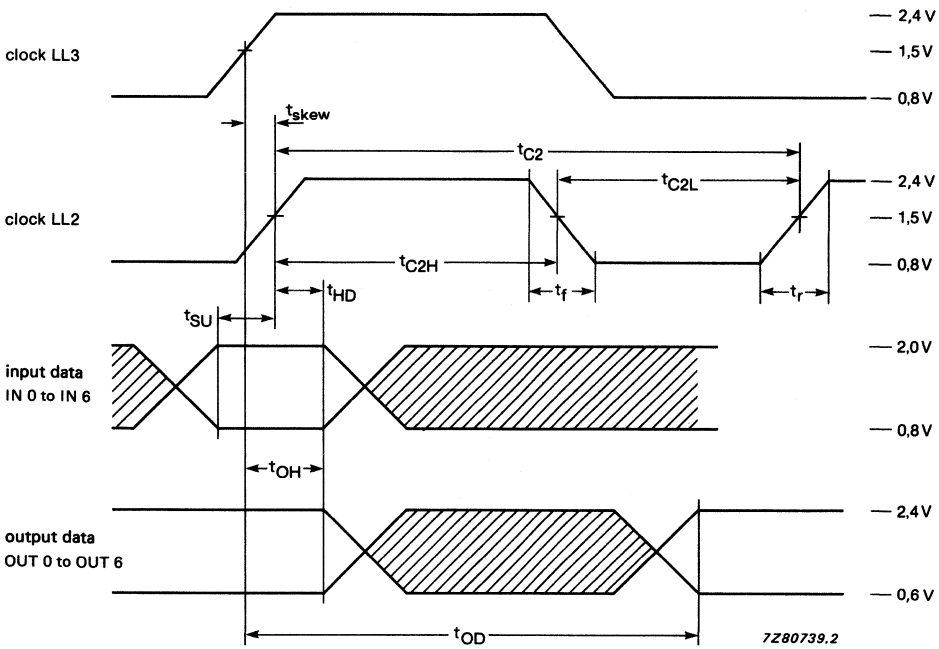


Fig. 5 Timing diagram.

VIDEO PROCESSOR WITH DACs (VDA)

GENERAL DESCRIPTION

The SAA9060 is a video processor with DACs (VDA), which converts the digital luminance and chrominance data into analogue information for a RGB controller. The SAA9060 forms part of a chip-set for digital TV systems.

Features

- Single scan or double scan applications
- Parallel data input
- 7-bit D/A conversion of the colour difference signals
- 8-bit D/A conversion of the luminance signal

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Input current		I_{DD}	–	170	250	mA
Power dissipation		P_{tot}	–	–	1.4	W
Back-bias voltage			−3	–	0	V
Operating ambient temperature range		T_{amb}	0	–	+ 70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

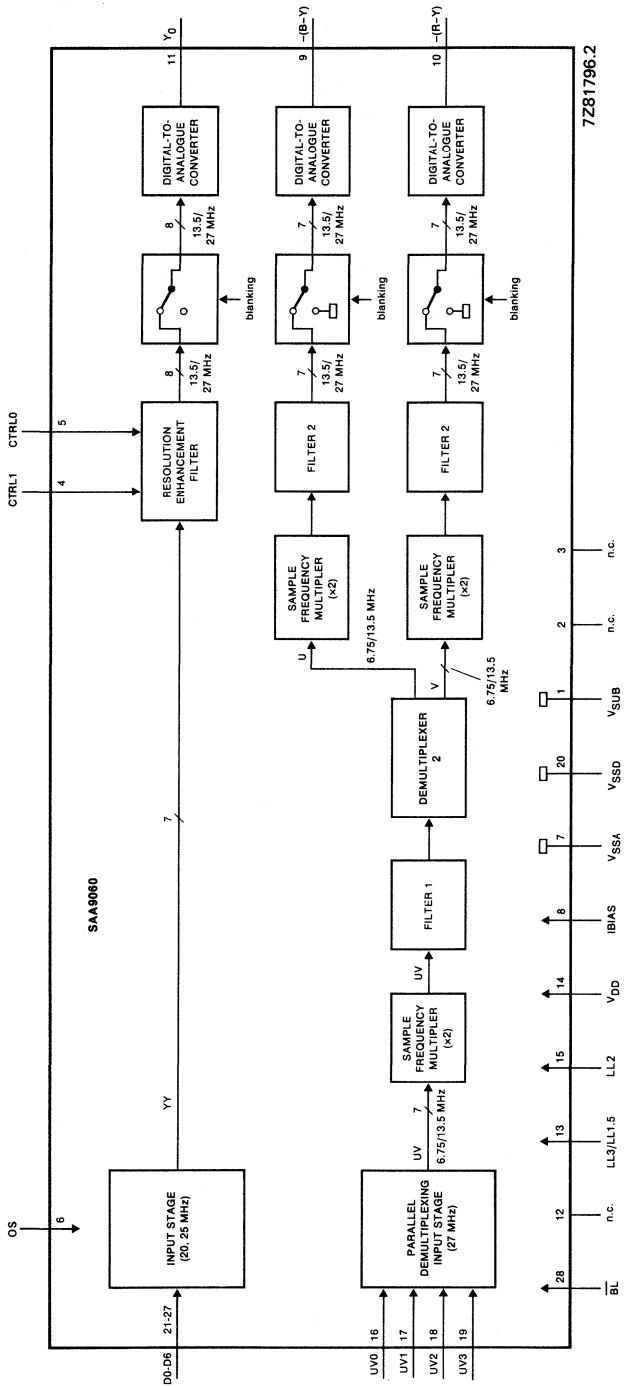


Fig.1 Block diagram.

PINNING

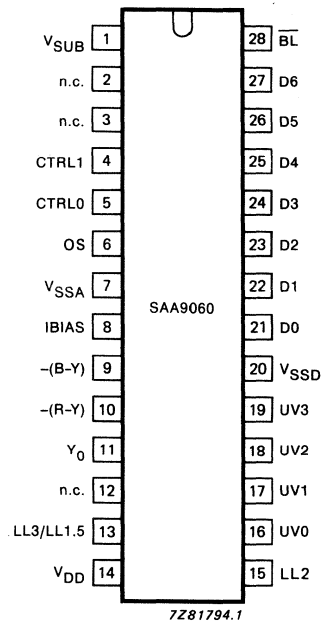


Fig.2 Pinning diagram.

1	V_{SUB}	Substrate pin for external capacitor, smooths internally generated voltages
2, 3	n.c.	Not connected
4	CTRL1	Control input for resolution enhancement filter
5	CTRL0	Control input for resolution enhancement filter
6	OS	Data format switch-over (from serial to parallel) at inputs DO...D6, UVO...UV3, BLN
7	V_{SSA}	Analogue ground
8	IBIAS	Reference current for the DACs
9	−(B-Y)	Chrominance analogue output; inverted colour difference signal B-Y
10	−(R-Y)	Chrominance analogue output; inverted colour difference signal R-Y
11	Y_O	Luminance analogue output
12	n.c.	Not connected
13	LL3/ LL1.5	Clock input: single scan parallel mode, f = 13.5 MHz double scan parallel mode, f = 27 MHz

PINNING (continued)

14	V_{DD}	Supply voltage
15	LL2	(Clock input for data word D0...D6) for serial data format only*/ f = 20.25 MHz; low-level version Do not connect pin when selecting parallel data format
16	UV0	Digital chrominance input; f = 13.5 MHz or 27 MHz
17	UV1	
18	UV2	
19	UV3	
20	V_{SSD}	Digital ground (0 V)
21	D0	Digital 7-bit luminance input; f = 13.5 MHz or 27 MHz
22	D1	
23	D2	
24	D3	
25	D4	
26	D5	
27	D6	
28	$\overline{BL}$	Format input; indicates the start of a transmission of a data line

FUNCTIONAL DESCRIPTION (see Fig. 1)

The VDA, DMSD/S-DMSD and a RGB controller form the video channel of a digital TV system. The VDA receives the luminance and chrominance data from the DMSD/S-DMSD and converts this data into an analogue output for a RGB controller.

Chrominance data signal

The chrominance data consist of alternating UV samples with a sample frequency of 3.375 MHz (single scan), the sample frequency is increased to 13.5 MHz by using two cascaded interpolation filters. The 7-bit chrominance data is then converted to an analogue signal (inverted colour difference signals B-Y and R-Y) for use in a RGB controller.

Luminance data signal

The luminance data frequency is clocked at 13.5 MHz or 27 MHz into the resolution enhancement filter (controlled by CTRL0 and CTRL1), this improves the quantization noise behaviour in areas with small variation and produces an 8-bit data output. The 8-bit data is converted into an analogue signal for use in a RGB controller.

$\overline{\text{BL}}$ signal (see Fig. 3)

The $\overline{\text{BL}}$ signal is used to indicate the active video length within the line and synchronizes the demultiplexing of the UV data.

Operating modes

There are two operating modes:

- parallel data transmission (single scan); LL3/LL1.5 = 13.5 MHz
- parallel data transmission (double scan), LL3/LL1.5 = 27 MHz.

Output signals

The output signals are AC-coupled to a RGB controller. During the horizontal synchronization gap the luminance and chrominance signals are blanked (black and no colour difference respectively) and the RGB controller clamps the input signals.

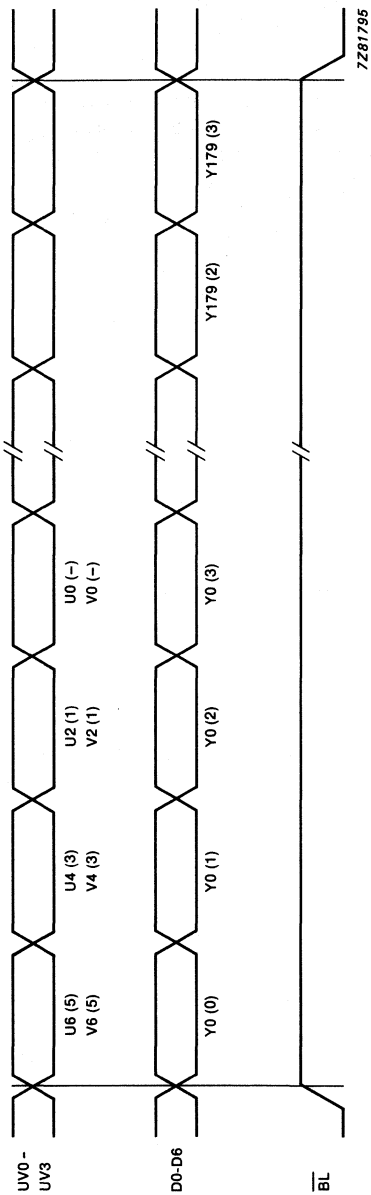


Fig.3 Data format.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.3	6.0	V
Input voltage		V_I	−0.5	6.0	V
Back-bias voltage		V_{BIAS}	−3	0	V
Storage temperature range		T_{stg}	−55	+ 125	°C
Operating ambient temperature range		T_{amb}	0	+ 70	°C

THERMAL RESISTANCE

Junction to ambient	$R_{th\ j\text{-}a}$	50 K/W

CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all values referred to V_{SS}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Supply current		I_{DD}	*	170	250	mA
Voltage on pin 1	with clock	V_{SUB}	−3.0	−2.5	−2.0	V
Current on pin 1	without clock	I_{SUB}	−	0.2	40	μA
Voltage ripple on pin 1		V_{ripple}	−	−	10	mV
Inputs						
LL3 input signal	note 1; see Fig. 4					
Input voltage HIGH		V_{IH}	2	−	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	−	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	−	−	10	pF
LL3 time period	f_{nom} = 13.5 MHz	t_{LL3}	69	74	80	ns
Duty factor		t_{PH}/t_{LL3}	43	50	57	%
LL1.5 input signal	note 2; see Fig. 5					
Input voltage HIGH		V_{IH}	2	−	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	−	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	−	−	10	pF
LL1.5 time period	f_{nom} = 27 MHz	$t_{LL1.5}$	35	37	40	ns
Duty factor		$t_{PH}/t_{LL1.5}$	43	50	57	%

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{BL}$ input signal	note 3; see Figs 6 and 7					
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	–	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	–	–	10	pF
Input current HIGH		I_{IH}	–	–	1	μA
Input current LOW		I_{IL}	–	–	100	μA
Pulse width HIGH		t_{PH}	–	720	–	*
Pulse width LOW	NTSC/PAL	t_{PL}	–	138/144	–	*
LL3 set-up time		t_{SU}	12	–	–	ns
D0-D6 and UV0 to UV3	note 2; see Fig. 8					
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	–	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	–	–	10	pF
Input current HIGH		I_{IH}	–	–	1	μA
Input current LOW		I_{IL}	–	–	100	μA
LL1.5 set-up time		t_{SU}	13	–	–	ns
LL1.5 hold time		t_{HD}	3	–	–	ns
CTRL0 and CTRL1 input signals	note 4					
Input voltage HIGH	note 5	V_{IH}	2	–	V_{DD}	V
Input voltage LOW	note 5	V_{IL}	V_{SS}	–	0.8	V
Input capacitance**	V_I = 0 V	C_I	–	–	10	pF
IBIAS input signal	Fig. 9					
Input current	note 6	I_{IBIAS}	–	100	–	μA
Bias resistance	note 7	R_{IBIAS}	–	39	–	kΩ
Input voltage	note 7	V_{IBIAS}	–	V_{DD}	–	V
Potential difference across R_{IBIAS}	note 8	U_{IBIAS}	–	1.5	–	V

* Clock periods of LL3.
** Referred to pin 20.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
OUTPUTS						
Y signal output	note 9					
Resolution			–	8	–	bits
Nominal range	max. 255		14	–	230	
Output current	max. 2.55	I_O	0.14	–	2.3	mA
Resolution per step	I_{IBIAS} = 100 μA	Res	–	10	–	μA
Load on pin 11		R_L	–	180	–	Ω
Coupling capacitance to RGB controller	see Fig. 10	C_{OC}	–	47	–	nF
Total output capacitance (pin 11)	note 10	C_O	–	7	–	pF
Conversion time		t_{DAC}	–	–	30	ns
Time constant	$\approx R_L (C_S + C_D + C_E)$	t_C	–	50	–	ns
Output voltage range		V_O	$V_{DD}-2$	–	V_{DD}	V
Differential non-linearity			–0.5	–	+ 0.5	LSB
Equality of converter output normalized to maximum level			–1	–	+ 1	LSB
Temperature dependency	$\Delta I_{IBIAS} = 0$		–0.5	–	+ 0.5	LSB
Glitch			–0.5	–	+ 0.5	LSB
–(B-Y) signal output	note 10					
Resolution			–	7	–	bits
Nominal range	max. 127		13	–	114	
Output current		I_O	0.26	–	2.28	mA
Resolution per step	I_{IBIAS} = 100 μA	Res	–	20	–	μA
Load on pin 9		R_L	–	750	–	Ω
Coupling capacitance to RGB controller	see Fig. 10	C_{OC}	–	10	–	nF
Total output capacitance (pin 9)	including pin capacitance and wiring	C_O	–	7	–	pF
Conversion time		t_{DAC}	–	–	30	ns
Time constant	$\approx R_L (C_S + C_D + C_E)$	t_C	–	50	–	ns

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage range		V_O	$V_{DD}-2$	–	V_{DD}	V
Differential non-linearity			−0.5	–	+ 0.5	LSB
Equality of converter output normalized to maximum level			−1	–	+ 1	LSB
Temperature dependency	$\Delta I_{IBIAS} = 0$		−0.5	–	+ 0.5	LSB
Glitch			−0.5	–	+ 0.5	LSB
−(R-Y) signal output	note 10					
Resolution			–	7	–	bits
Nominal range	max. 127		10	–	117	
Output current	max. 2.55		0.2	–	2.34	mA
Resolution per step	I_{IBIAS} = 100 μA	Res	–	20	–	μA
Load on pin 10		R_L	–	560	–	Ω
Coupling capacitance to RGB controller	see Fig. 10	C_{OC}	–	10	–	nF
Total output capacitance (pin 10)	including pin capacitance and wiring	C_O	–	7	–	pF
Conversion time		t_{DAC}	–	–	30	ns
Time constant	$\approx R_L (C_S + C_D + C_E)$	t_C	–	50	–	ns
Output voltage range		V_O	$V_{DD}-2$	–	V_{DD}	V
Differential non-linearity			−0.5	–	+ 0.5	LSB
Equality of converter output normalized to maximum level			−1	–	+ 1	LSB
Temperature dependency	ΔI_{IBIAS}		−0.5	–	+ 0.5	LSB
Glitch			−0.5	–	+ 0.5	LSB

Notes to the characteristics

1. 25/30 Hz picture frequency with interlace.
2. 50/60 Hz picture frequency, parallel data transmission.
3. 25/30 Hz picture frequency, f = 20.25 MHz.
4. Static input signal; input HIGH by means of an internal pull-up resistor of 100 kΩ.
5.

CTRL1	CTRL0	filter function
0	0	bypass (min.)
1	1	lowpass (max.)

6. When I_{IBIAS} = 100 μA the quantization steps of the Y output DAC is 10 μA and −(B-Y), −(R-Y) outputs are 20 μA. The maximum voltage at R_L is 2 V. If R_{IBIAS} is used, the temperature coefficients of I_{BIAS} and the DACs are compensated.
7. Effective voltage noise is ⩽ 1 mV.
8. $U_{IBIAS} = 1.2\ V + I_{IBIAS} \times 3\ k\Omega$.
9. Values measured from the Y output DAC.
10. Values measured from the −(B-Y) output DAC.

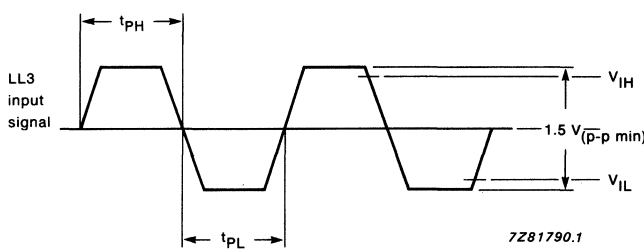


Fig. 4 LL3 timing waveform; 25/30 Hz picture frequency with interlace.

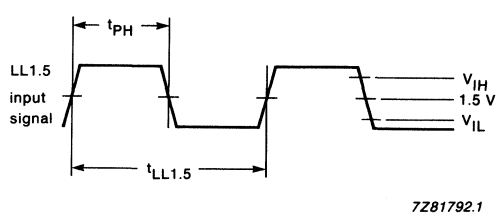


Fig. 5 LL1.5 timing waveform; 50/60 Hz picture frequency, parallel data transmission.

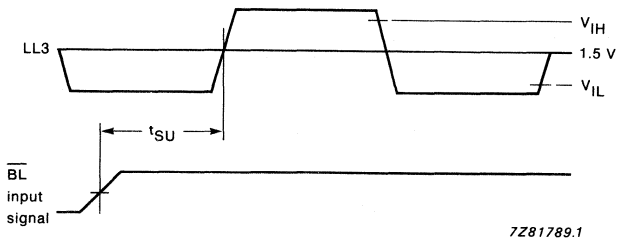


Fig. 6 $\overline{BL}$ timing waveform; 25/30 Hz picture frequency; f = 13.5 MHz.

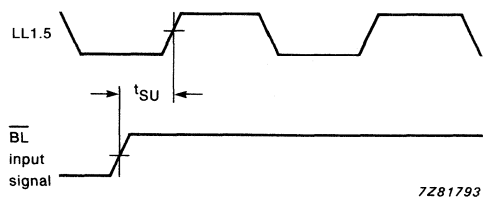


Fig. 7 $\overline{BL}$ timing waveform; 50/60 Hz picture frequency; f = 27 MHz.

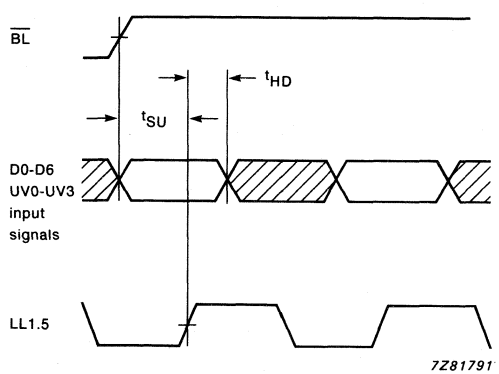


Fig. 8 D0 to D6 and UV0 to UV3 timing waveform; 50/60 Hz picture frequency, f = 27 MHz.

APPLICATION INFORMATION

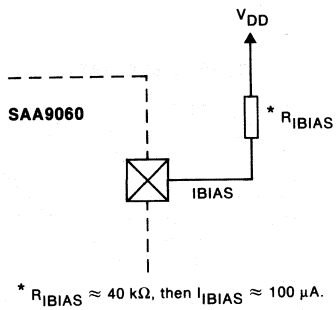
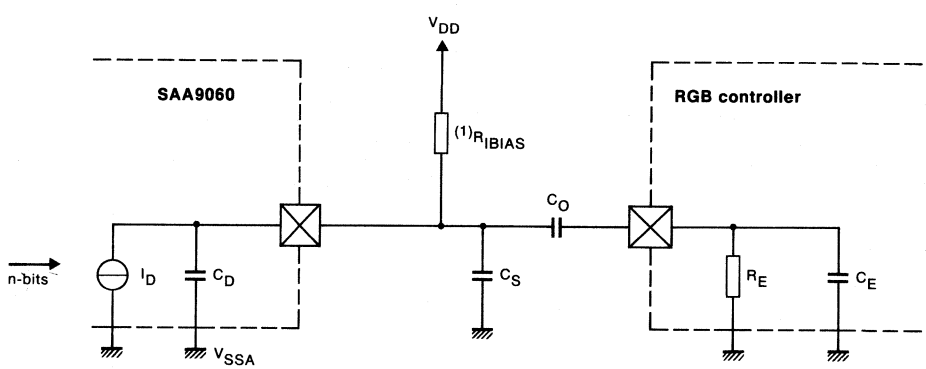


Fig. 9 IBIAS input circuit.



(1) $R_{IBIAS} = R_L$ (Y output), R_L (B-Y output), R_L (R-Y output)

Fig. 10 Application of the DACs.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	April 1992

SAA9065
Video enhancement and D/A processor (VEDA)

FEATURES

- CMOS circuit to enhance video data and to convert luminance and colour-difference signals from digital-to-analog
- 16-bit parallel input for YUV-bus
- Data clock input LLC (line-locked clock) for a data rate up to 30 MHz
- 8-bit luminance and 8-bit multiplexed colour-difference formats (optional 7-bit formats)
- MC input to enable input data, suitable for synchronization from an external source with a lower clock (LLC/2)
- Formatter for YUV input data; 4:2:2 format, 4:1:1 format and filter characteristics selectable
- HREF input to determine the active line (number of pixels)
- Controllable peaking of luminance signal to enhance internal data to 11 bits (signal improvement)
- Coring stage with controllable threshold to eliminate noise in luminance signal
- Interpolation filter suitable for both formats to increase the data rate in chrominance path
- Polarity of colour-difference signals selectable
- Separate digital-to-analog converters (9-bit solution for Y; 8-bit for colour-difference signals)
- 1 V (p-p)/ 75 Ω outputs realized by two resistors
- No external adjustments
- All functions controlled via I^2C-bus

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
I_{DD}	total supply current	-	tbf	-	mA
V_{IL}	input voltage LOW on YUV-bus	−0.5	-	0.8	V
V_{IH}	input voltage HIGH on YUV-bus	2	-	V_{DDD}+0.5	V
f_{LLC}	input data rate	-	-	32	MHz
$V_{o\ Y,CD}$	output signal Y, ±(R–Y) and ±(B–Y) (peak-to-peak value)	-	2	-	V
$R_{L\ Y,CD}$	output load resistance	125	-	-	Ω
ILE	DC integral linearity error in output signal (8-bit data)	-	-	1	LSB
DLE	DC differential error in output signal (8-bit data)	-	-	0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9065	44	PLCC	plastic	SOT187

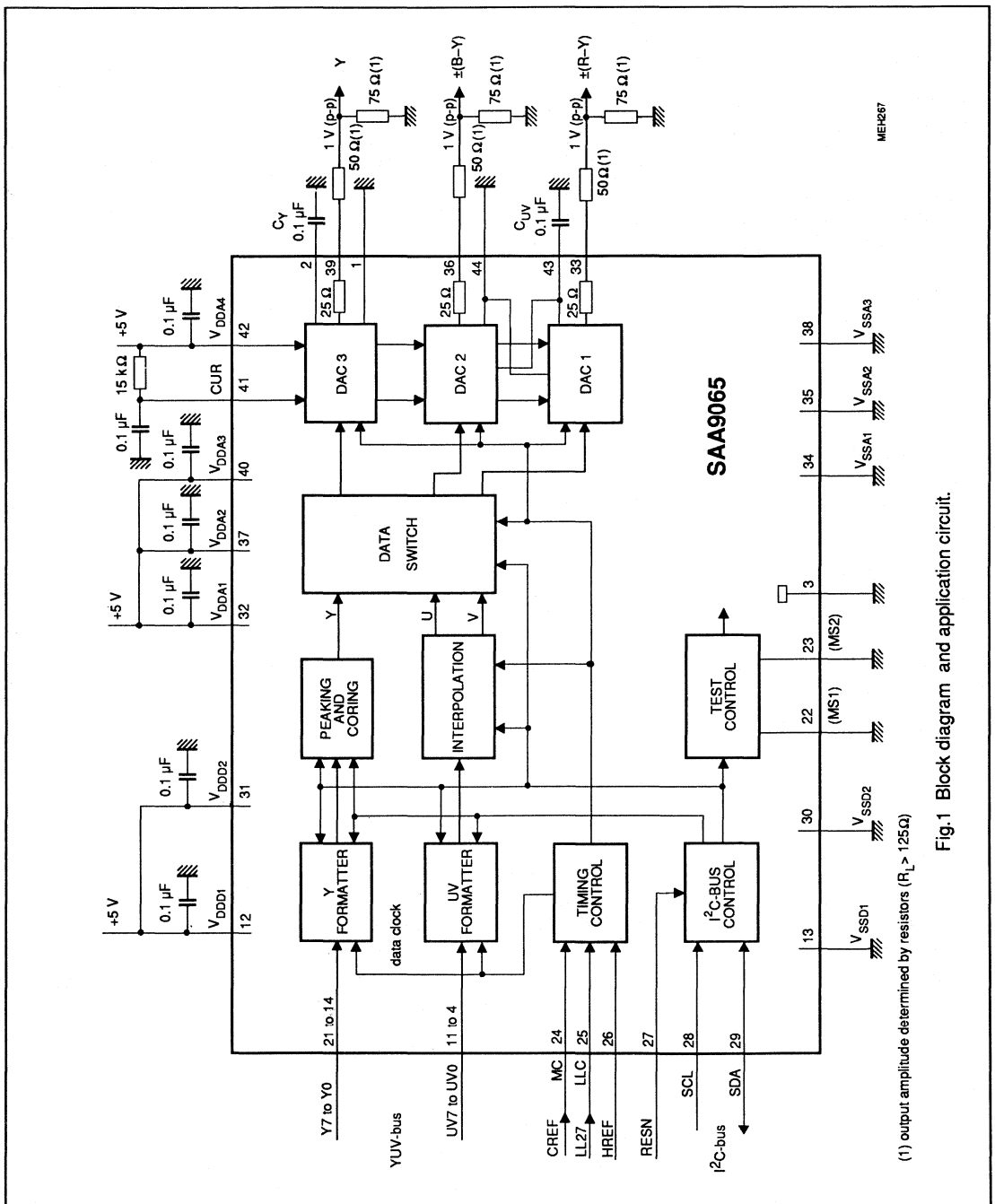


Fig.1 Block diagram and application circuit.

(1) output amplitude determined by resistors (R_L > 125Ω)

PINNING

SYMBOL	PIN	DESCRIPTION
$REFL_Y$	1	low reference of luminance DAC (connected to V_{SSA1})
C_Y	2	capacitor for luminance DAC (high reference)
SUB	3	substrate (connected to V_{SSA1})
UV0	4	UV signal input bits UV7 to UV0 (digital colour-difference signal)
UV1	5	
UV2	6	
UV3	7	
UV4	8	
UV5	9	
UV6	10	
UV7	11	
V_{DDD1}	12	+5 V digital supply voltage 1
V_{SSD1}	13	digital ground 1 (0 V)
Y0	14	Y signal input bits Y7 to Y0 (digital luminance signal)
Y1	15	
Y2	16	
Y3	17	
Y4	18	
Y5	19	
Y6	20	
Y7	21	
MS2	22	mode select 2 input for testing chip
MS1	23	mode select 1 input for testing chip
MC	24	data clock CREF (13.5 MHz e. g.); at MC = HIGH the LLC divider-by-two is inactive
LLC	25	line-locked clock signal (LL27 = 27 MHz)
HREF	26	data clock for YUV data inputs (for active line 768Y or 640Y long)
RESN	27	reset input (active LOW)
SCL	28	I^2C-bus clock line
SDA	29	I^2C-bus data line
V_{SSD2}	30	digital ground 2 (0 V)
V_{DDD2}	31	+5 V digital supply voltage 2
V_{DDA1}	32	+5 V analog supply voltage for buffer of DAC 1
(R–Y)	33	±(R–Y) output signal (analog signal)
V_{SSA1}	34	analog ground 1 (0 V)

SYMBOL	PIN	DESCRIPTION
V_{SSA2}	35	analog ground 2 (0 V)
(B–Y)	36	±(B–Y) output signal (analog colour-difference signal)
V_{DDA2}	37	+5 V analog supply voltage for buffer of DAC 2
V_{SSA3}	38	analog ground 3 (0 V)
Y	39	Y output signal (analog luminance signal)
V_{DDA3}	40	+5 V analog supply voltage for buffer of DAC 3
CUR	41	current input for analog output buffers
V_{DDA4}	42	supply and reference voltage for the three DACs
C_{UV}	43	capacitor for chrominance DACs (high reference)
$REFL_{UV}$	44	low reference of chrominance DACs (connected to V_{SSA1})

PIN CONFIGURATION

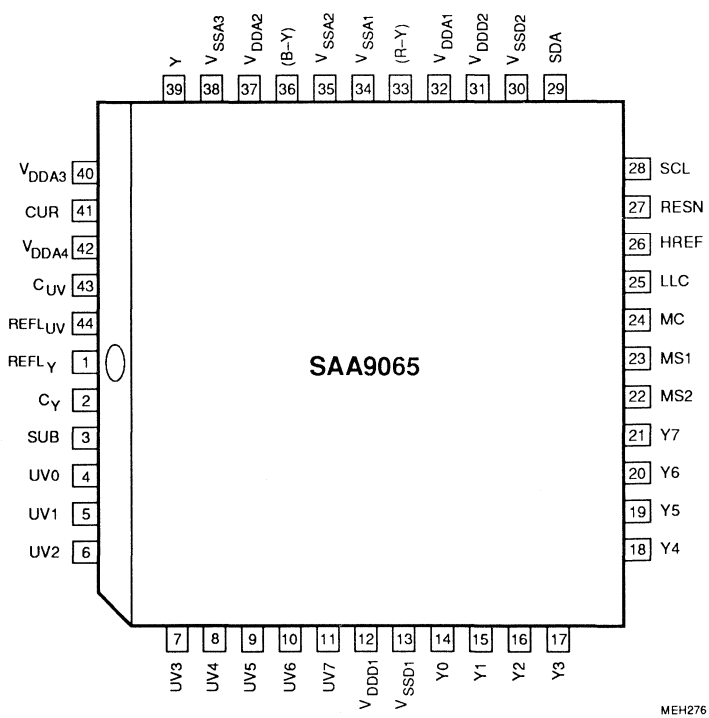


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The CMOS circuit SAA9065 processes digital YUV-bus data up to a data rate of 30 MHz. The data inputs Y7 to Y0 and UV7 to UV0 (Fig.1) are provided with 8-bit data. The data of digital colour-difference signals U and V are in a multiplexed state (serial in 4:2:2 or 4:1:1 format; Tables 2 and 3).

Data is read with the rising edge of LLC (line-locked clock) to achieve a data rate of LLC at MC = HIGH only. If MC is supplied with the frequency CREF (LLC/2 for example), data is read only at every second rising edge (Fig.3).The 8-bit input data can be reduced to 7-bit data words by means of the R78-bit (R78 = 0). Additionally, the luminance data format is converted for internal use into a two's complement format by inverting MSB. The Y input byte (bits Y7 to Y0) represent pixel information; the UV input byte (bits UV7 to UV0) one of the two digital colour-difference signals in 4:2:2 format (Table 2).

The HREF input signal (HREF = HIGH) determines the start and the end of an active line (Fig.3) the number of pixels respectively . The analog output Y is blanked at HREF = LOW, the (B–Y) and (R–Y) outputs are in a colourless state. The blanking level can be set by the BLV-bit. Nearly all characteristics are controllable via the I²C-bus

Y and UV formatters

The input data formats are formatted into the internally used processing formats (separate for 4:2:2 and 4:1:1 formats) employing a defined delay and a multiplexer cascade. The signals are prepared for interpolation, and the IFF, IFC and IFL bits switch to the input data format and determine the right interpolation filter (Figures 10 to 13).

Peaking and coring

Peaking is applied to the Y signal to compensate several bandwidth reductions of the previous analog receiver part. Y signals can be improved to obtain a better sharpness.

There are the two switchable bandpass filters BF1 and BF 2 controlled via the I²C-bus by the bits BP1, BP0 and BFB. Thus, a frequency response is achieved in combination with the peaking factor K (Figures 5 to 9; K is determined by the bits BFB, WG1 and WG0).

The coring stage with controllable threshold (4 states controlled by CO1 and CO0 bits) reduces noise disturbances (generated by the bandpass gain) by suppressing the amplitude of small signal components. The remaining high-frequent peaking component is available for a weighted addition after coring.

Table 1 LLC and MC configuration modes in DMSD applications

PIN	INPUT SIGNAL	COMMENT
LLC MC	LLC (LL27) CREF	The data rate on YUV-bus is half the clock rate on pin LLC, e. g. in SAA7151B, SAA7191 and SAA7191B single scan operation.
LLC MC	LLC (LL27) MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. in double scan applications.
LLC MC	LLC2/LL3 MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. SAA9051 single scan operation.
Note: YUV data are only latched with the rising edge of LLC at MC = HIGH.		

Table 2 Data format 4 : 2 : 2. (Fig.3)

INPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Note to Table 2

The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

Interpolation

The chrominance interpolation filter consists of various filter stages, multiplexers and de-multiplexers to increase the data rate of the colour-difference signals by a factor of 2 or 4. The switching of the filters by the bits IFF, IFC and IFL is described previously. Additional signal samples with significant amplitudes between two consecutive signal samples of the low data rate are generated. The time-multiplexed U and V samples are stored in parallel for converting.

Data switch

The digital signals are switched by the timing control, then adapted to the conversation range. U and V data have 8-bit formats again; Y can have 9 bits dependent on peaking. Blanking and switching to colourless level is applied here. Bits can be inverted by INV-bit to change the polarity of colour-difference output signals.

Digital-to-analog converters

Conversion is separate for Y, U and V. The converters use resistor chains with low-impedance output buffers. The minimum output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V floating. An application for 1 V/ 75 Ω on outputs is shown in Fig.1.

Each digital-to-analog converter has its own supply and ground pins suitable for decoupling. The reference voltage, supplying the resistor chain of all three DACs, is the supply voltage V_{DDA4}. The current into pin 41 is 0.3 mA ; a larger current improves the bandwidth but increases the integral non-linearity.

Table 3 Data format 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE							
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

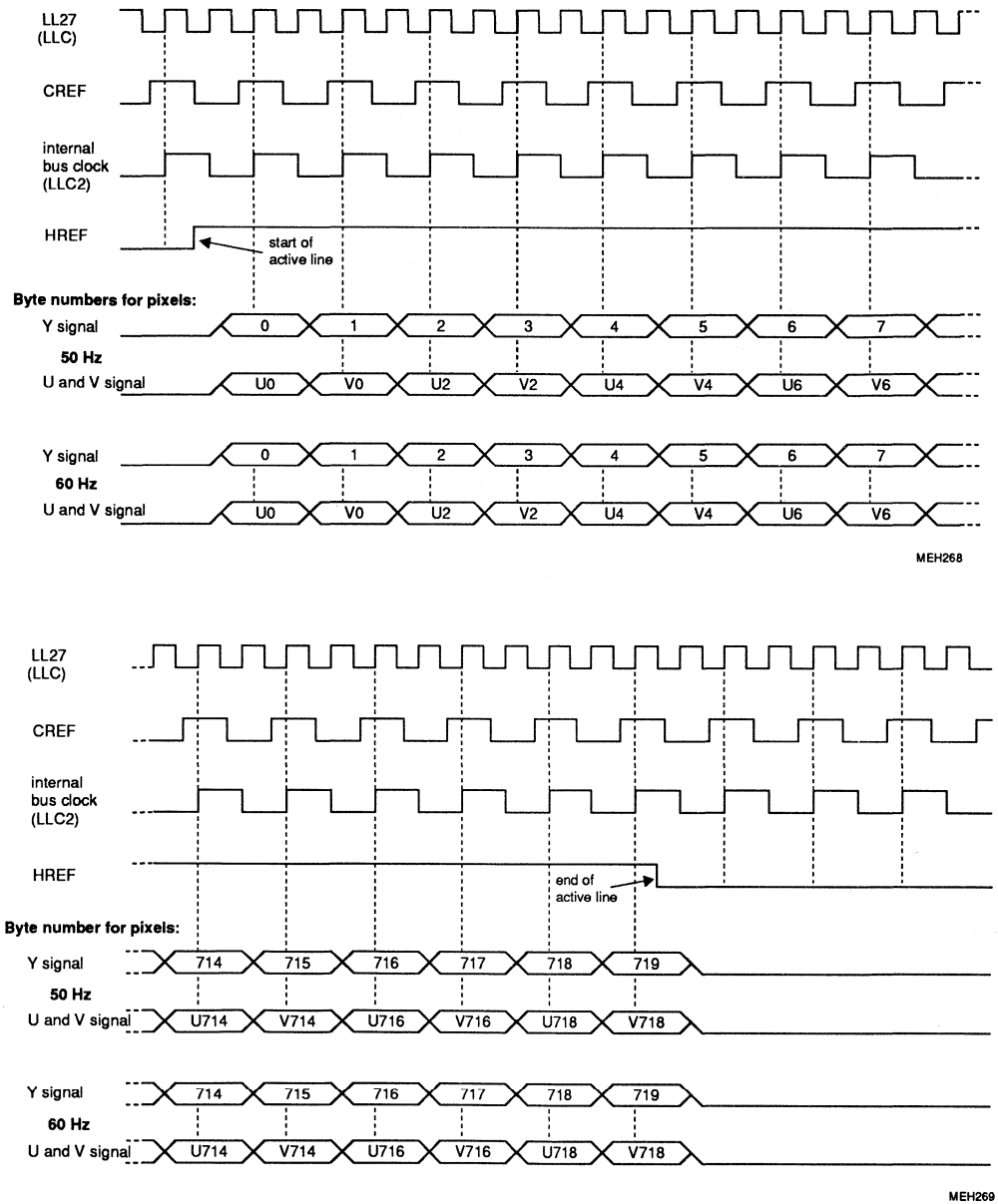


Fig.3 Line control by HREF for 4 : 2 : 2 format, CREF = 13.5 MHz; HREF = 720 pixel; 50 Hz and 60 Hz field.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	−0.3	7	V
V_{DDD2}	supply voltage range (pin 31)	−0.3	7	V
V_{DDA1}	supply voltage range (pin 32)	−0.3	7	V
V_{DDA2}	supply voltage range (pin 37)	−0.3	7	V
V_{DDA3}	supply voltage range (pin 40)	−0.3	7	V
V_{DDA4}	supply voltage range (pin 42)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD1} - V_{SSA}$	-	±100	mV
V_n	voltage on all input pins 4 to 11, 14 to 27 and 41	−0.3	V_{DDD}	V
V_n	voltage on analog output pins 33, 36 and 39	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	46 K/W

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; LLC = LL27; MC = CREF = 13.5 MHz; T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	for digital part	4.5	5	5.5	V
V_{DDD2}	supply voltage range (pin 31)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 32)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 37)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 40)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 42)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current (I_{DDD1} + I_{DDD2})	for digital part	-	tbf	tbf	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	for DACs and buffers	-	tbf	tbf	mA
YUV-bus inputs (pins 4 to 11 and 14 to 21)		Figures 3 and 4				
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
Inputs MS1, MS2, MC, LLC, HREF and RESN (pins 22 to 27)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
V_{24}	MC input voltage for LL27	27 MHz data rate	2.0	-	V_{DDD}+0.5	V
	CREF signal on MC input	CREF data rate; note 1	-	-	-	V
I²C-bus SCL and SDA (pins 28 and 29)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	µA
V_{OL}	SDA output voltage LOW (pin 29)	I_{29} = 3 mA	-	-	0.4	V
I_{29}	output current	during acknowledge	3	-	-	mA
Digital-to-analog converters (pins 1, 2, 41, 42, 43 and 44)						
V_{DAC}	input reference voltage for internal resistor chains (pin 42)		4.75	5	5.25	V
I_{CUR}	input current (pin 41)	$R_{41\text{-}42}$ = 15 kΩ	-	300	-	µA
$V_{1,44}$	reference voltage LOW	pin connected to V_{SSA1}	-	0	-	V
C_L	external blocking capacitor to V_{SSA1} for reference voltage HIGH (pins 2 and 43)		-	0.1	-	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LLC}	minimum data conversation rate (clock)	Fig.3	-	-	32	MHz
Res	resolution	luminance DAC	-	9	-	bit
		chrominance DACs	-	8	-	bit
ILE	DC integral linearity error	8-bit data	-	-	1.0	LSB
DLE	DC differential error	8-bit data	-	-	0.5	LSB
Y, ±(R–Y) and ±(B–Y) analog outputs (pins 39, 33 and 36)						
V_o	output signal voltage (peak-to-peak value)	without load	-	2	-	V
$V_{33,36,39}$	output voltage range	without load; note 2	0.2	-	2.2	V
V_{39}	output blanking level	Y output; note 3	-	16	-	LSB
$V_{33,36}$	output no-colour level	±(R–Y), ±(B–Y); note 4	-	128	-	LSB
$R_{33,36,39}$	internal serial output resistance		-	25	-	Ω
$R_{L\ 33,36,39}$	output load resistance	external load	125	-	-	Ω
B	output signal bandwidth	-3 dB	20	-	-	MHz
t_d	signal delay from input to Y output		-	tbf	-	ns
LLC timing (pins 25)		LLC; Fig.3				
t_{LLC}	cycle time		33	37	41	ns
$t_{p\ H}$	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
YUV-bus timing (pins 4 to 11 and 14 to 21)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
MC timing (pin24)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
RESN timing (pin 27)						
t_{SU}	set-up time after power-on or failure	active LOW; note 5	4 x t_{LLC}	-	-	ns

Notes to the characteristics

1. YUV-bus data is read at MC = HIGH (pin 24) clocked with LLC (Fig.5) . Data is read only with every second rising edge of LLC when CREF = LLC/2 on MC-pin 24.
2. 0.2 to 2.2 V ouput voltage range at 8-bit DAC input data. The data word can increase to 9-bit dependent on peaking factor.
3. The luminance signal is set to the digital black level: 16 LSB for BLV-bit = 0; 0 LSB for BLV-bit = 1.
4. The chrominance amplitudes are set to the digital colourless level of 128 LSB.
5. The circuit is prepared for a new data initialization.

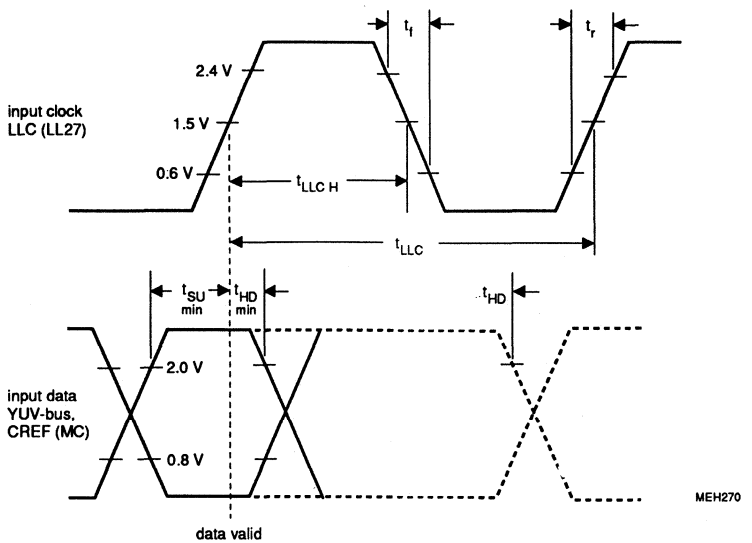


Fig.4 YUV-bus data and CREF timing.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 111X**
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus transmission

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Peaking and coring	01	0	CO1	CO0	BP1	BP0	BFB	WG1	WG0
Input formats; interpolation	02	IFF	IFC	IFL	0	0	0	0	0
Input/output setting	03	0	0	0	0	DRP	BLV	R78	INV

Bit functions in data bytes:

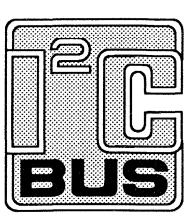
CO1 to CO0 — Control of coring threshold:

CO1	CO0	
0	0	coring off
0	1	small noise reduction
1	0	medium noise reduction
1	1	high noise reduction

BP1, BP0 and BFB — Bandpass filter selection:

BP1	BP0	BFB	
0	0	0	characteristic Fig.5
0	1	0	characteristic Fig.6
1	0	0	characteristic Fig.7
1	1	0	characteristic Fig.8
0	0	1	BF1 filter bypassed Fig.9
X	X	1	not recommended

BFB, WG1 and WG0	Peaking factor K:	BFB	WG1	WG0	
		0	0	0	K = 1/8; minimum peaking
		0	0	1	K = 1/4
		0	1	0	K = 1/2
		0	1	1	K = 1; maximum peaking
		1	0	0	K = 0; peaking off
		1	0	1	K = 1/4; minimum peaking
		1	1	0	K = 1/2
		1	1	1	K = 1; maximum peaking
IFF, IFC, IFL	Input format and filter control at 13.5 MHz data rate:	IFF	IFC	IFL	
		0	0	0	4 : 1 : 1 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		0	0	1	4 : 1 : 1 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		0	1	0	4 : 1 : 1 format; –3 dB attenuation at 1.2 MHz video frequency; Fig.12
		1	0	0	4 : 2 : 2 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		1	0	1	4 : 2 : 2 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		1	1	X	4 : 2 : 2 format; –3 dB attenuation at 2.5 MHz video frequency; Fig.13
DRP	UV input data code:	0 = two's complement; 1 = offset binary			
BLV	Blanking level on Y output:	0 = 16 LSB; 1 = 0 LSB			
R78	YUV input data solution:	0 = 7-bit data; 1 = 8-bit data			
INV	Polarity of colour-difference output signals:	0 = normal polarity equal to input signal 1 = inverted polarity			



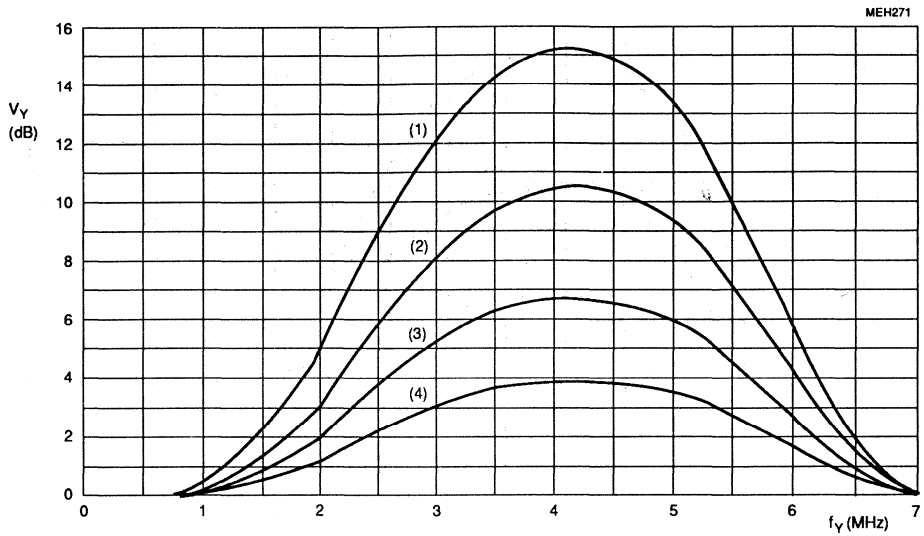


Fig.5 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

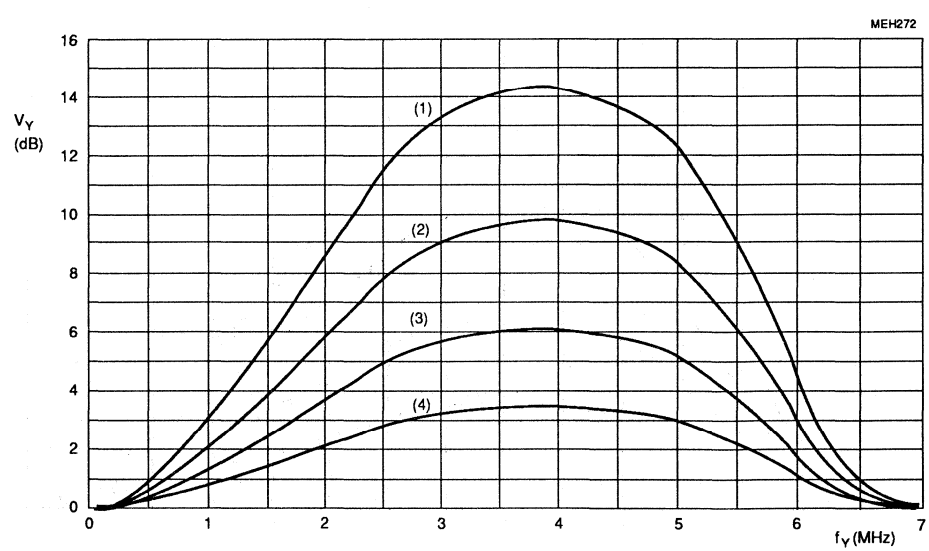


Fig.6 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

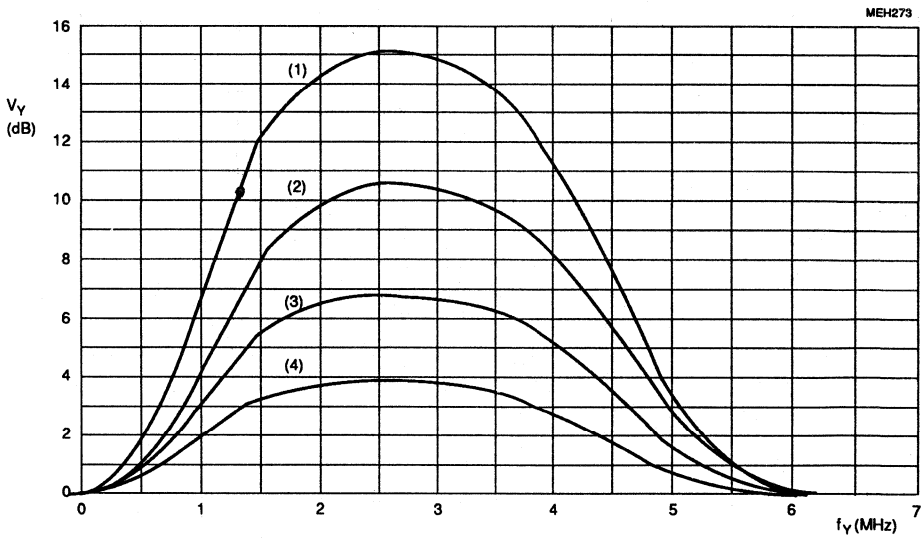


Fig.7 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

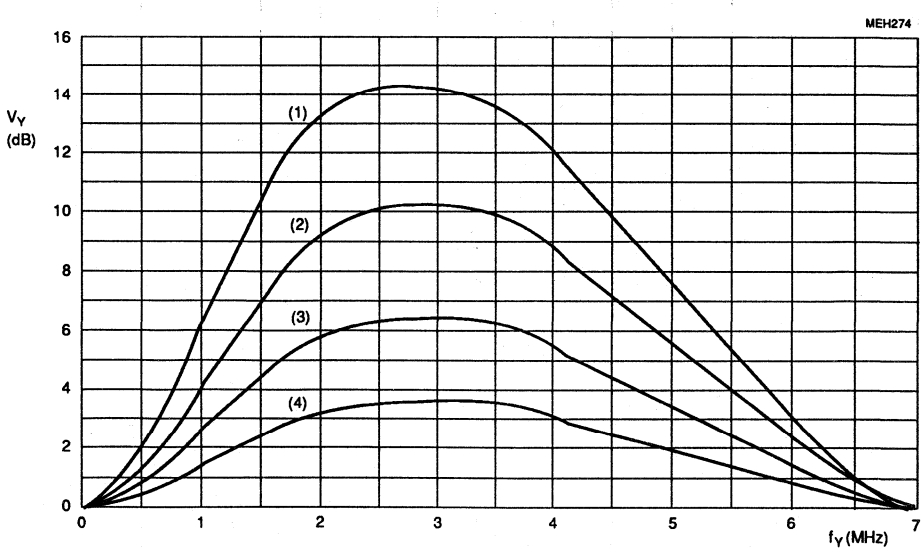


Fig.8 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

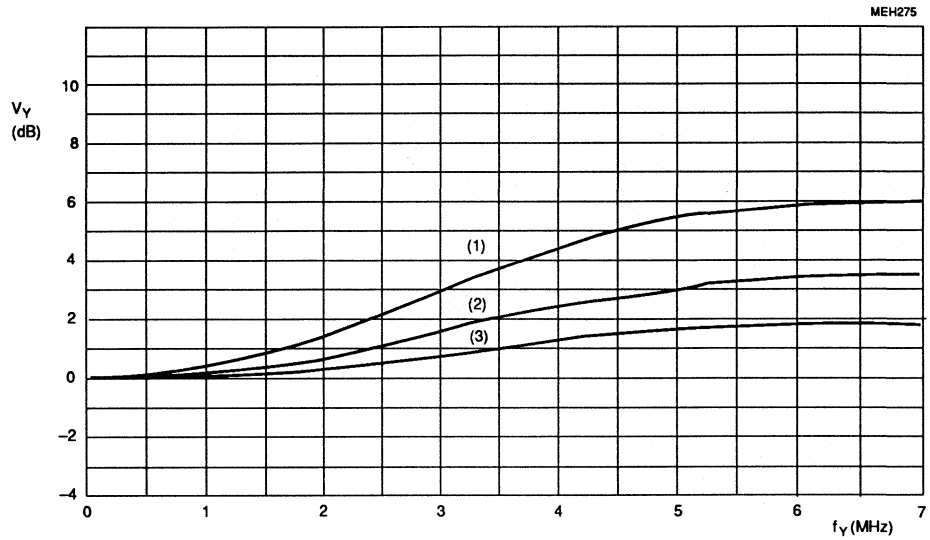


Fig.9 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1; (2) K = 1/2; (3) K = 1/4.

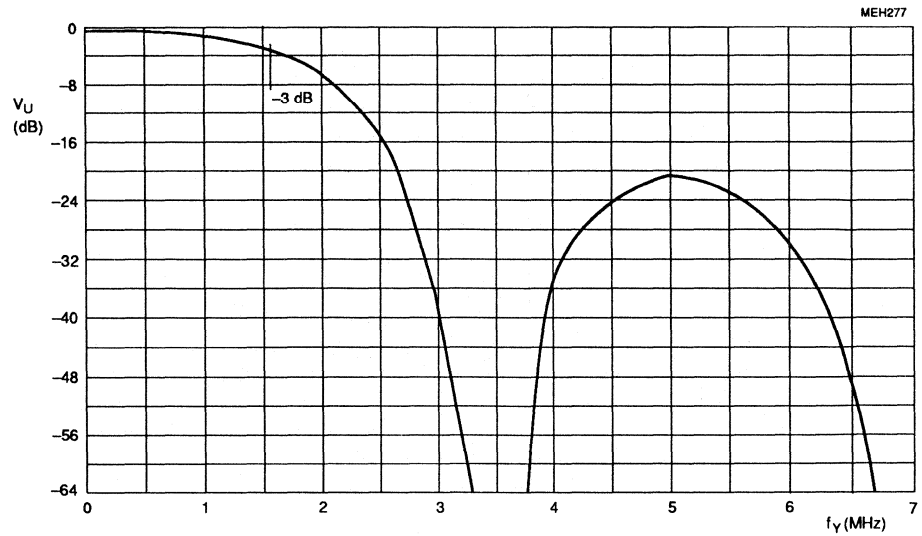


Fig.10 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 0 in 4:1:1 format, and control bits IFF = 1; IFC = 0 and IFL = 0 in 4:2:2 format; 13.5 MHz data rate.

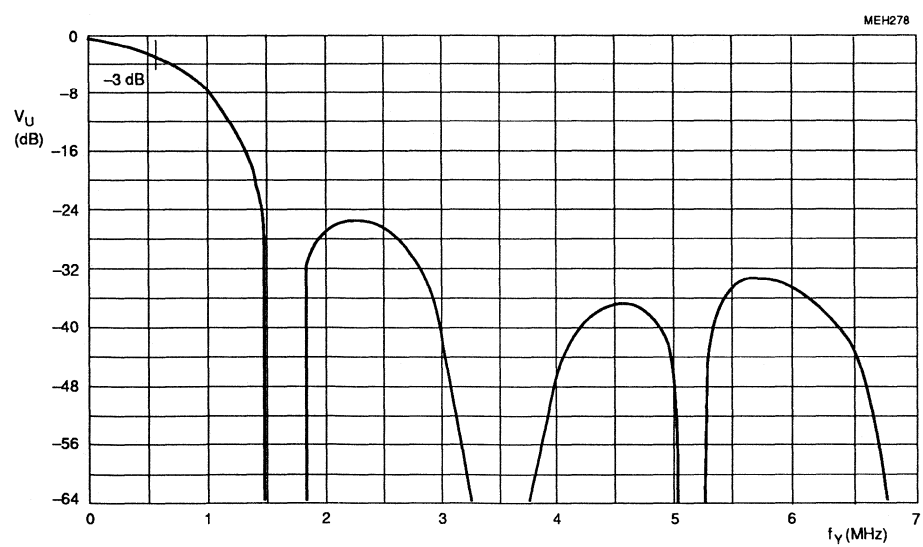


Fig.11 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 1 in 4:1:1 format, and control bits IFF = 1; IFC = 0 and IFL = 1 in 4:2:2 format; 13.5 MHz data rate.

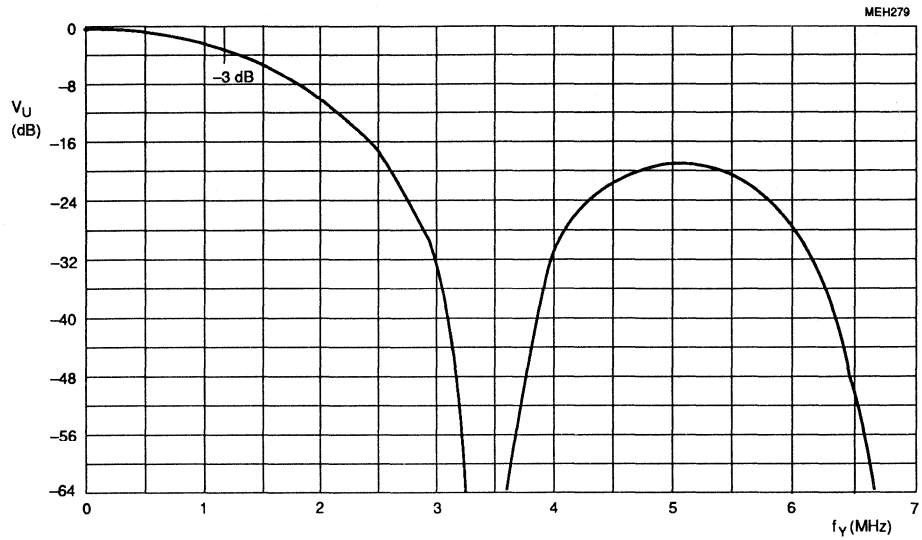


Fig.12 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 1 and IFL = 0 in 4:1:1 format; 13.5 MHz data rate.

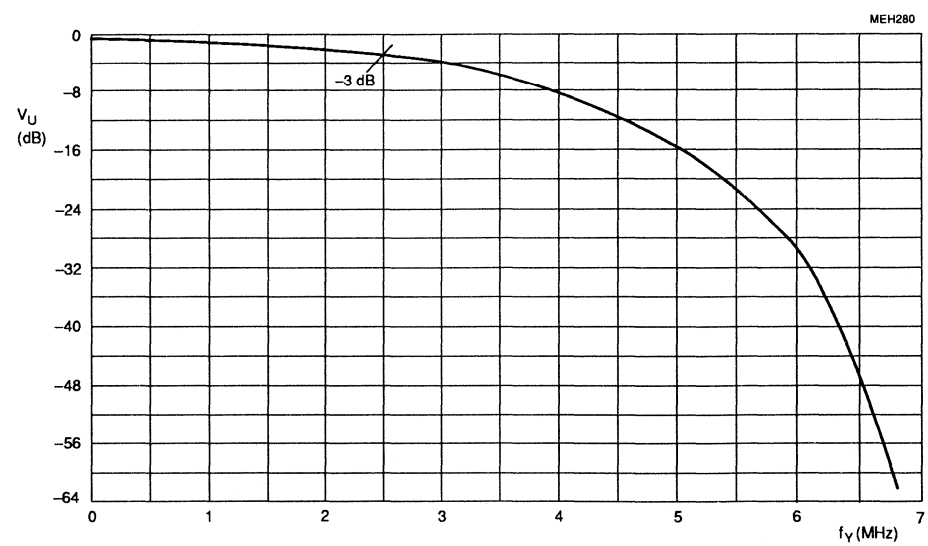


Fig.13 Interpolation filter with I²C-bus control bits IFF = 1; IFC = 1 and IFL = X in 4:2:2 format; 13.5 MHz data rate.

7-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC 7)

GENERAL DESCRIPTION

The SAA9079 is a monolithic NMOS 7-bit analogue-to-digital converter (ADC) designed for video applications. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 22 MHz.

The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- No external sample and hold required
- High input impedance
- Binary or two's complement 3-state TTL outputs
- Overflow and underflow 3-state TTL outputs
- All outputs positive-edge triggered
- Standard 24-pin package

Applications

- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

QUICK REFERENCE DATA

Measured over full voltage and temperature range unless otherwise specified

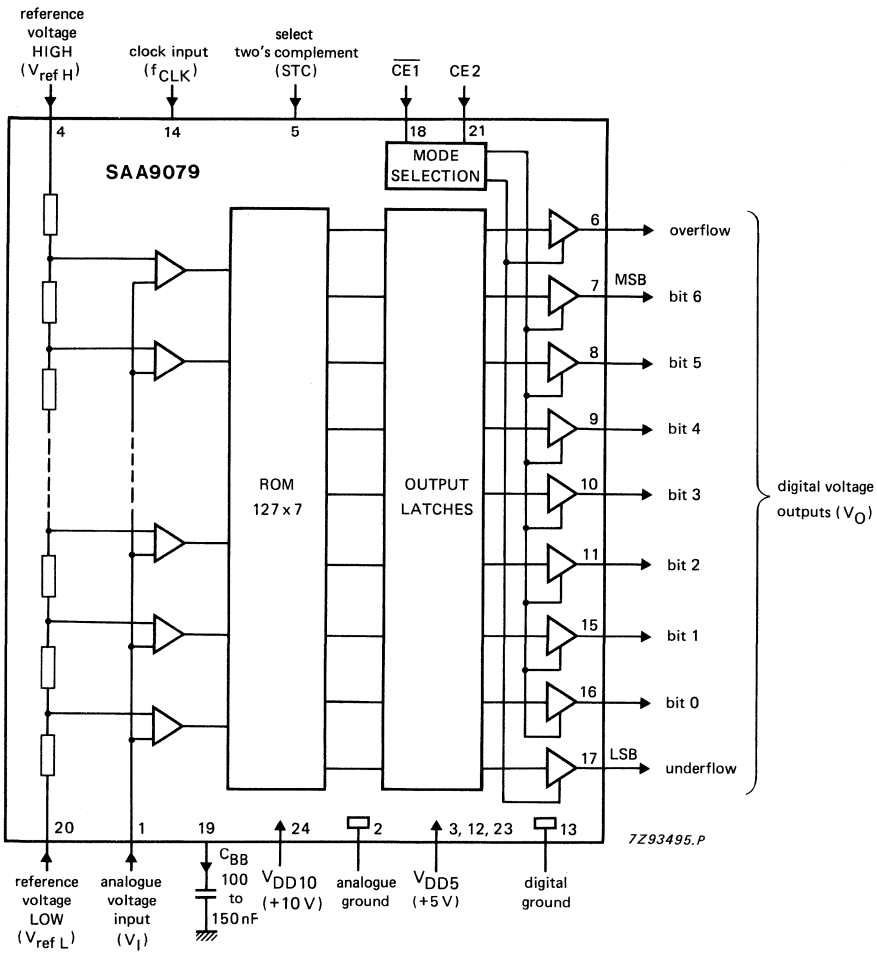
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pins 3, 12, 23)		V_{DD5}	4.5	–	5.5	V
Supply voltage (pin 24)		V_{DD10}	9.5	–	10.5	V
Supply current (pins 3, 12, 23)	note 1	I_{DD5}	–	–	65	mA
Supply current (pin 24)	note 1	I_{DD10}	–	–	13	mA
Reference current (pins 4, 20)		I_{ref}	150	–	450	μA
Reference voltage LOW (pin 20)		V_{refL}	2.4	2.5	2.6	V
Reference voltage HIGH (pin 4)		V_{refH}	5.0	5.1	5.2	V
Non-linearity	f_i = 1.1 kHz					
integral		INL	–	–	± ½	LSB
differential		DNL	–	–	± ½	LSB
–3 dB Bandwidth		B	11	–	–	MHz
Clock frequency (pin 14)		f_{CLK}	1	–	22	MHz
Total power dissipation	note 1	P_{tot}	–	–	500	mW

Note to quick reference data

1. Measured under nominal conditions: V_{DD5} = 5 V; V_{DD10} = 10 V; T_{amb} = 22 °C.

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).
24-lead mini-pack; plastic (SO24; SOT137A).



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

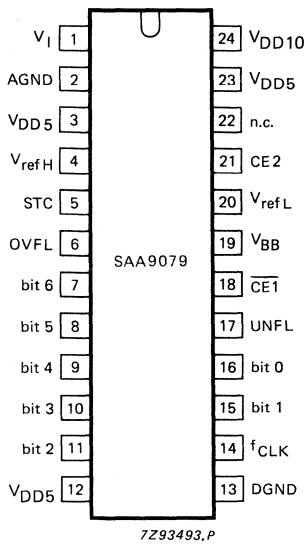


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD5}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD5}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	$\overline{CE1}$	chip enable input 1
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	CE2	chip enable input 2
22	n.c.	not connected
23	V_{DD5}	positive supply voltage (+ 5 V)
24	V_{DD10}	positive supply voltage (+ 10 V)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pins 3, 12, 23)	V_{DD5}	−0.5	+ 7.0	V
Supply voltage range (pin 24)	V_{DD10}	−0.5	+ 12.0	V
Input voltage range	V_I	−0.5	+ 7.0	V
Output current	I_O	−	5	mA
Total power dissipation	P_{tot}	−	1	W
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3, 12, 23-13} = 4.5$ to 5.5 V; $V_{DD10} = V_{24-2} = 9.5$ to 10.5 V; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD5}	4.5	–	5.5	V
Supply voltage (pin 24)	V_{DD10}	9.5	–	10.5	V
Supply current (pins 3, 12, 23)	I_{DD5}	–	–	85	mA
Supply current (pin 24)	I_{DD10}	–	–	18	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2.4	2.5	2.6	V
Reference voltage HIGH (pin 4)	V_{refH}	5.0	5.1	5.2	V
Reference current	I_{ref}	150	–	450	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	−0.3	–	0.8	V
Input voltage HIGH (note 1)	V_{IH}	3.0	–	V_{DD5}	V
Digital input levels (pins 5, 18, 21; note 2)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD5}	V
Input current					
at $V_5 = 0$ V; V_{13} = GND	$-I_5$	15	–	70	μA
at $V_{18} = 5$ V; V_{13} = GND	I_{18}	15	–	70	μA
at $V_{21} = 0$ V; V_{13} = GND	$-I_{21}$	15	–	120	μA
Input leakage current (except pins 5, 18 and 21)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at $V_{refL} = 2.5$ V; $V_{refH} = 5.1$ V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p-p)}$	–	2.6	–	V
Input capacitance (note 3)	C_{1-2}	–	–	30	pF

Notes to characteristics

1. Maximum input voltage must not exceed 5.0 V.
2. If pin 5 is LOW binary coding is selected.
   If pin 5 is HIGH two's complement is selected.
   If pin 5, 18 and 21 are open-circuit, pin 5, 21 are HIGH and pin 18 is LOW.
   For output coding see Table 1 and mode selection see Table 2.
3. Tested on sample base.

parameter	symbol	min.	max.	unit
Outputs				
Digital voltage outputs (pins 6 to 11 and 15 to 17)				
Output voltage LOW at I_O = 2 mA	V_{OL}	0	+0.4	V
Output voltage HIGH at $-I_O$ = 0.5 mA	V_{OL}	2.4	V_{DD5}	V

Table 1 Output coding (V_{refL} = 2.50 V; V_{refH} = 5.08 V)

step	V_{1-2} note 1	UNFL	OVFL	binary bit 6 — bit 0	two's complement bit 6 — bit 0
underflow	<2.51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2.51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2.53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
126	5.03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5.05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
overflow	$\geqslant 5.07$	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

steps 2-125

Note to Table 1

1. Approximate values.

Table 2 Mode selection

$\overline{CE1}$	CE2	bit 0 to bit 6	UNFL, OVFL
X	0	HIGH impedance	HIGH impedance
0	1	active	active
1	1	HIGH impedance	active

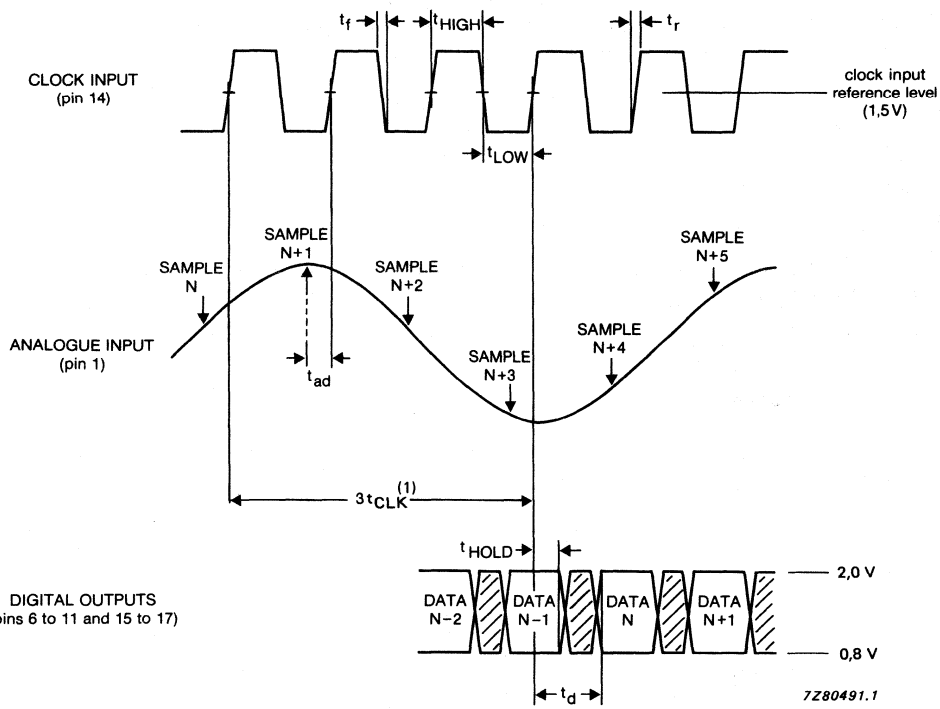
CHARACTERISTICS (continued)

$V_{DD5} = V_{3, 12, 23-13} = 4.5$ V to 5.5 V; $V_{DD10} = V_{24-2} = 9.5$ V to 10.5 V; $V_{refL} = 2.5$ V; $V_{refH} = 5.1$ V; $f_{CLK} = 22$ MHz; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

parameter	symbol	min.	max.	unit
Timing characteristics (see also Fig. 3)				
Clock input (pin 14)				
Clock frequency	f_{CLK}	1	22	MHz
Clock cycle time LOW	t_{LOW}	20	–	ns
Clock cycle time HIGH	t_{HIGH}	20	–	ns
Input rise and fall times (pin 1)				
rise time	t_r	–	5	ns
fall time	t_f	–	5	ns
Analogue input (note 1)				
Bandwidth (–3 dB)	B	11	–	MHz
Non-harmonic noise		–	–36	dB
Peak error (non-harmonic noise)		–	3	LSB
Harmonics (full scale)				
fundamental	f_0	–	0	dB
RMS (2nd and 3rd harmonic)	$f_{2.3}$	–	–28	dB
RMS (4th + 5th + 6th + 7th harmonic)	f_{4-7}	–	–35	dB
Digital outputs (notes 1 and 2)				
Output hold time	t_{HOLD}	6	–	ns
Output delay time at $C_L = 15$ pF	t_d	–	38	ns
Output delay time at $C_L = 50$ pF	t_d	–	48	ns
3-state delay time	t_{dt}	–	25	ns
Capacitive output load	C_{OL}	0	15	pF
Transfer function				
Non-linearity at $f_i = 1.1$ kHz				
integral	INL	–	± ½	LSB
differential	DNL	–	± ½	LSB

Notes to timing characteristics

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1.5 V.



(1) There is a delay of 3 clock cycles between sampling of an analogue input signal and the corresponding digital output.

Fig. 3 Timing diagram.

APPLICATION INFORMATION

The minimum and maximum values provided in the data sheet are guaranteed over the whole voltage and temperature range. This note gives additional information to the data sheet where the typical values indicate the behaviour under nominal conditions; V_{DD5} = 5 V, V_{DD10} = 10 V, T_{amb} = 22 °C.

parameter	symbol	typ.	unit
Supply			
Supply current (pins 3, 12, 23)	I_{DD5}	51	mA
Supply current (pin 24)	I_{DD10}	11	mA
Maximum clock frequency	f_{CLK}	25	MHz
Bandwidth (−3 dB)	B	20	MHz
Total power dissipation	P_{tot}	365	mW
Peak error (non-harmonic noise)		1.5	LSB
Suppression of harmonics			
sum of:			
$f_{2nd} + f_{3rd}$		31	dB
$f_{4th} + f_{5th} + f_{6th} + f_{7th}$		39	dB
Non-linearity			
integral	INL	± 1/4	LSB
differential	DNL	± 1/3	LSB
Differential gain	dG	± 3	%
Differential phase	dP	± 1	%
Large signal phase error	P_e	10	deg
Non-harmonic noise		40	dB
Duty factor (20.25 MHz)		50 ± 10	%

Typical values are measured on sample base.

Application recommendation

Spikes at the 10 V supply input must be avoided (e. g. overshoots during switching).
Even a spike duration of less than 1 μs can destroy the device.

Test philosophy

Fig. 4 is a block diagram showing analogue-to-digital testing with a phase locked signal source. The signal generator provides a 5 MHz sinewave for the device under test (except for the linearity test). The 22 MHz clock input is provided by the clock generator. The phase relationship between signal and clock generator is shifted by 100 pico sec. each signal period to provide an effective clock rate of 10 GHz for analysis.

Most calculations are carried out in the spectral domain using Fast Fourier Transformation (FFT) and the inverse FFT to return to time domain.

The successive processing completes the specific measurement (Fig. 5 and 6).

The non-linearities of the converter, integral (INL) and differential (DNL), are measured using a low frequency ramp signal. Within a general uncertain range of conversion between two steps the output signal of the converter randomly switches.

After low-pass filtering the different step width is used for calculating the line of least squares to obtain integral non-linearity.

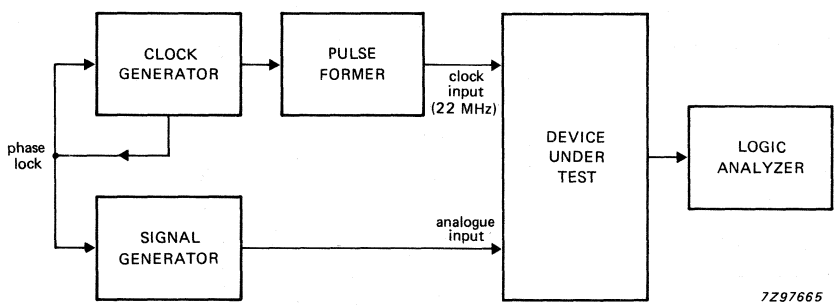
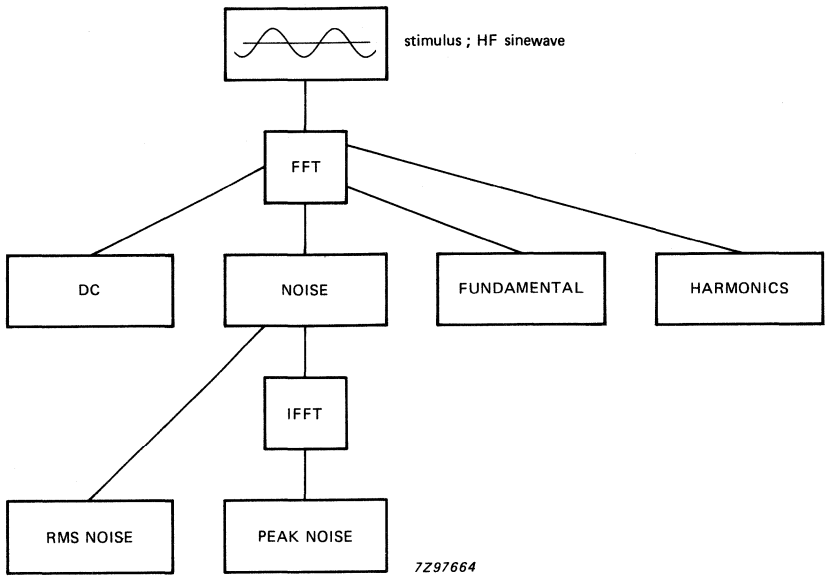


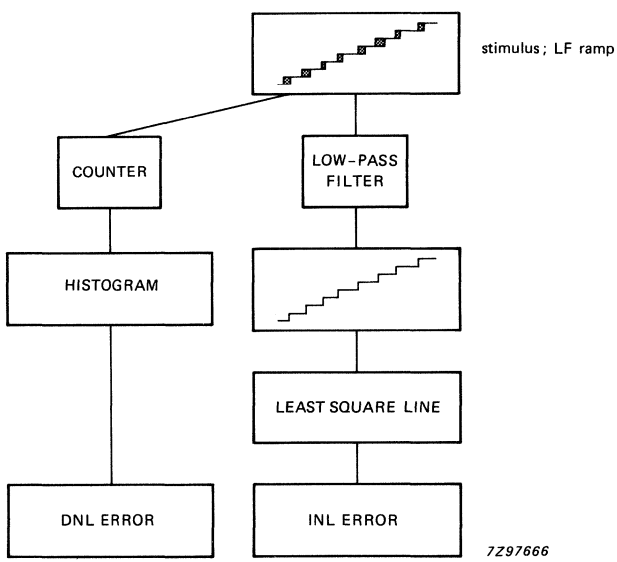
Fig. 4 Analogue-to-digital converter testing with locked signal source.

APPLICATION INFORMATION (continued)



Where: FFT = Fast Fourier Transformation.
IFFT = Inverse Fast Fourier Transformation.

Fig. 5 Sinewave test; non-harmonic noise and peak error.



Where: INL = Integral Non-Linearity.
DNL = Differential Non-Linearity.

Fig. 6 Low frequency ramp test; linearity.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3035 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 8 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 8 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 16)	V_{P1}	typ.	12 V
(pin 22)	V_{P2}	typ.	13 V
(pin 17)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 16)	I_{P1}	typ.	32 mA
(pin 22)	I_{P2}	typ.	0,1 mA
(pin 17)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	400 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

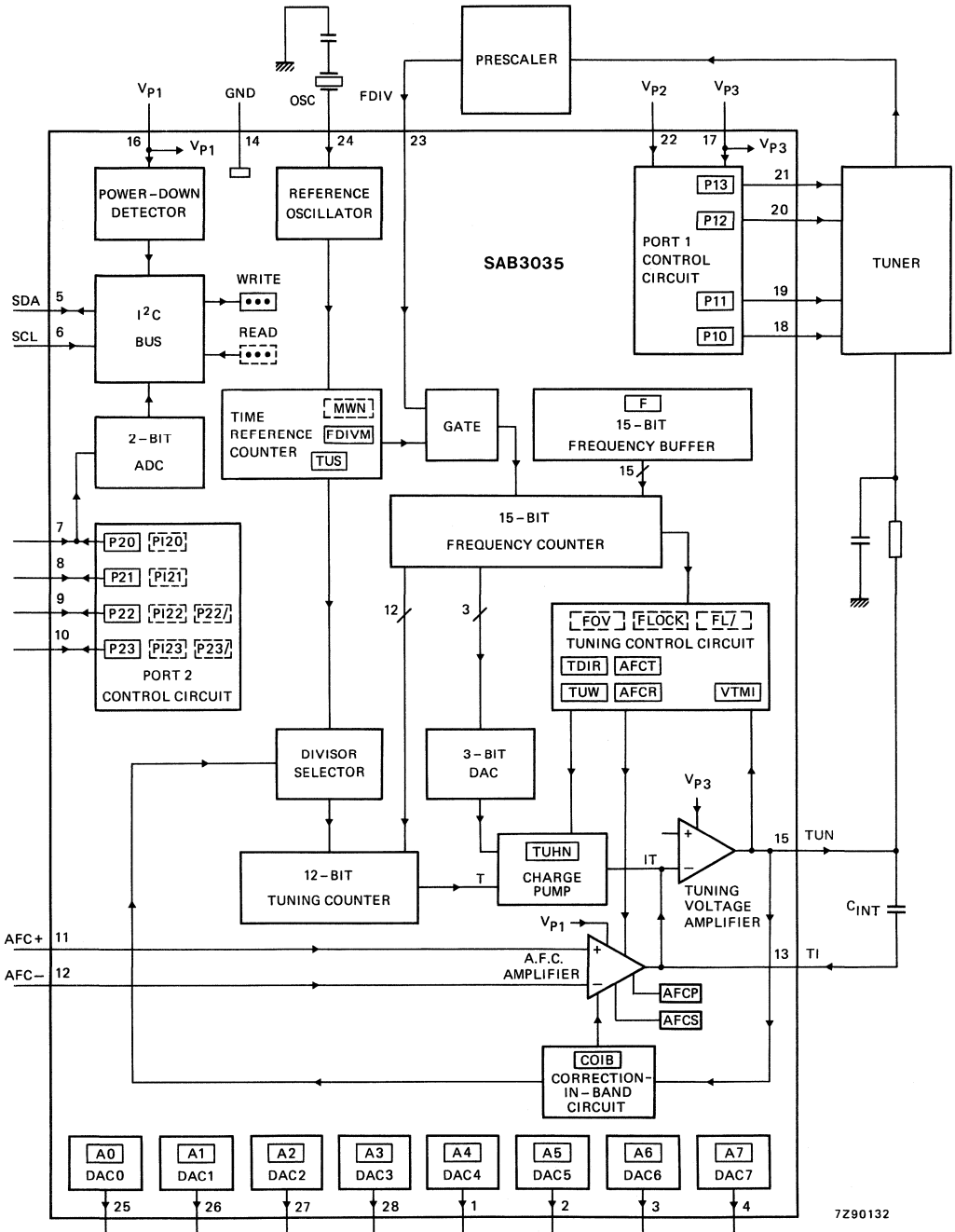


Fig. 1 Block diagram.

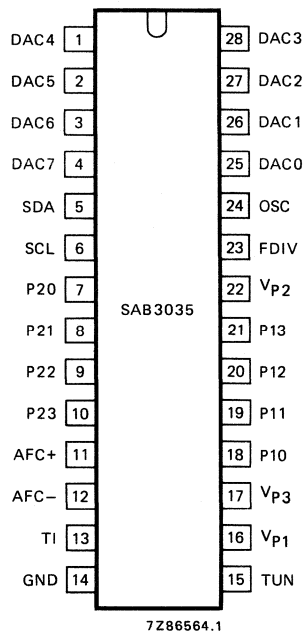


Fig. 2 Pinning diagram.

PINNING

1	DAC4	outputs of static DACs
2	DAC5	
3	DAC6	
4	DAC7	
5	SDA	serial data line (I^2C bus)
6	SCL	serial clock line (I^2C bus)
7	P20	general purpose input/output ports
8	P21	
9	P22	
10	P23	
11	AFC+	a.f.c. inputs
12	AFC–	
13	TI	tuning voltage amplifier inverting input
14	GND	ground
15	TUN	tuning voltage amplifier output
16	V_{P1}	+12 V supply voltage
17	V_{P3}	+32 V supply for tuning voltage amplifier
18	P10	High-current band-selection output ports
19	P11	
20	P12	
21	P13	
22	V_{P2}	positive supply for high-current band-selection output circuits
23	FDIV	input from prescaler
24	OSC	crystal oscillator input
25	DAC0	outputs of static DACs
26	DAC1	
27	DAC2	
28	DAC3	

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The SAB3035 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50$ kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50$ kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Eight 6-bit digital-to-analogue converters DAC0 to DAC7 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

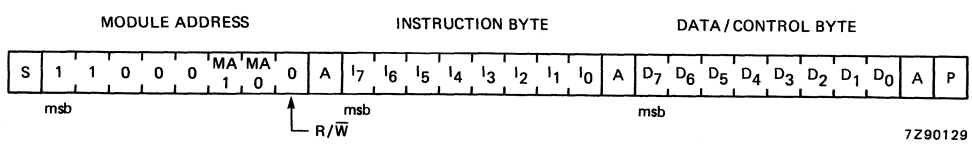


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X2, X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

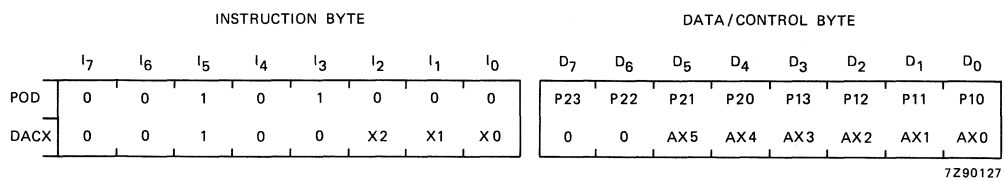


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

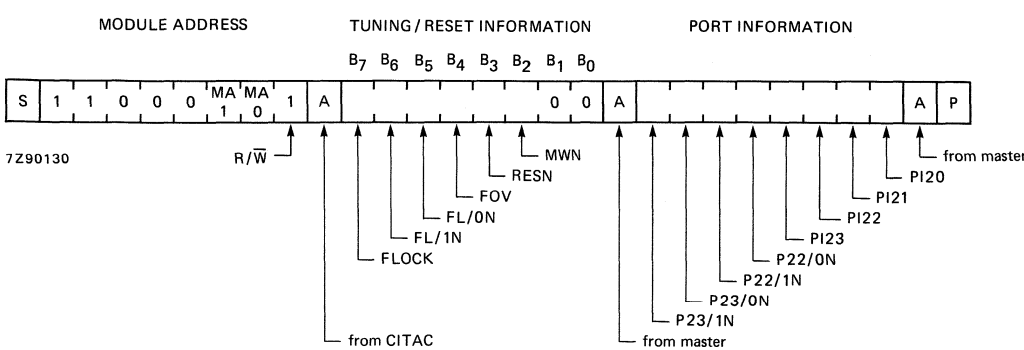


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

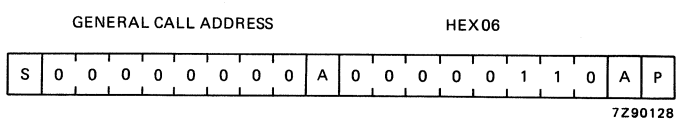


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 16)	V_{P1}	−0,3 to +18	V
(pin 22)	V_{P2}	−0,3 to +18	V
(pin 17)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 5)	V_{SDA}	−0,3 to +18	V
(pin 6)	V_{SCL}	−0,3 to +18	V
(pins 7 to 10)	V_{P2X}	−0,3 to +18	V
(pins 11 and 12)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 13)	V_{TI}	−0,3 to V_{P1}*	V
(pin 15)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 18 to 21)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 23)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 24)	V_{OSC}	−0,3 to +5	V
(pins 1 to 4 and 25 to 28)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	20	32	50	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	−2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	400	–	mW
Operating ambient temperature	T_{amb}	−20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 5); SCL input (pin 6)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 5, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 7 to 10, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 11, 12)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 13, 15)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 18 to 21)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 23)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 7 (pins 25 to 28 and 1 to 4)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 7) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

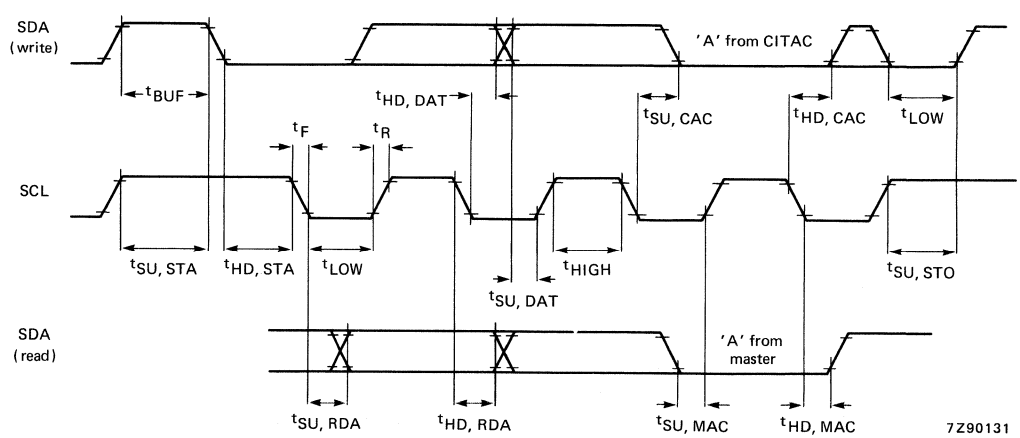


Fig. 8 I²C bus timing SAB3035.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3036 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I²C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I²C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 5)	V_{P1}	typ.	12 V
(pin 14)	V_{P2}	typ.	13 V
(pin 9)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 5)	I_{P1}	typ.	23 mA
(pin 14)	I_{P2}	typ.	0,1 mA
(pin 9)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	300 mW
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

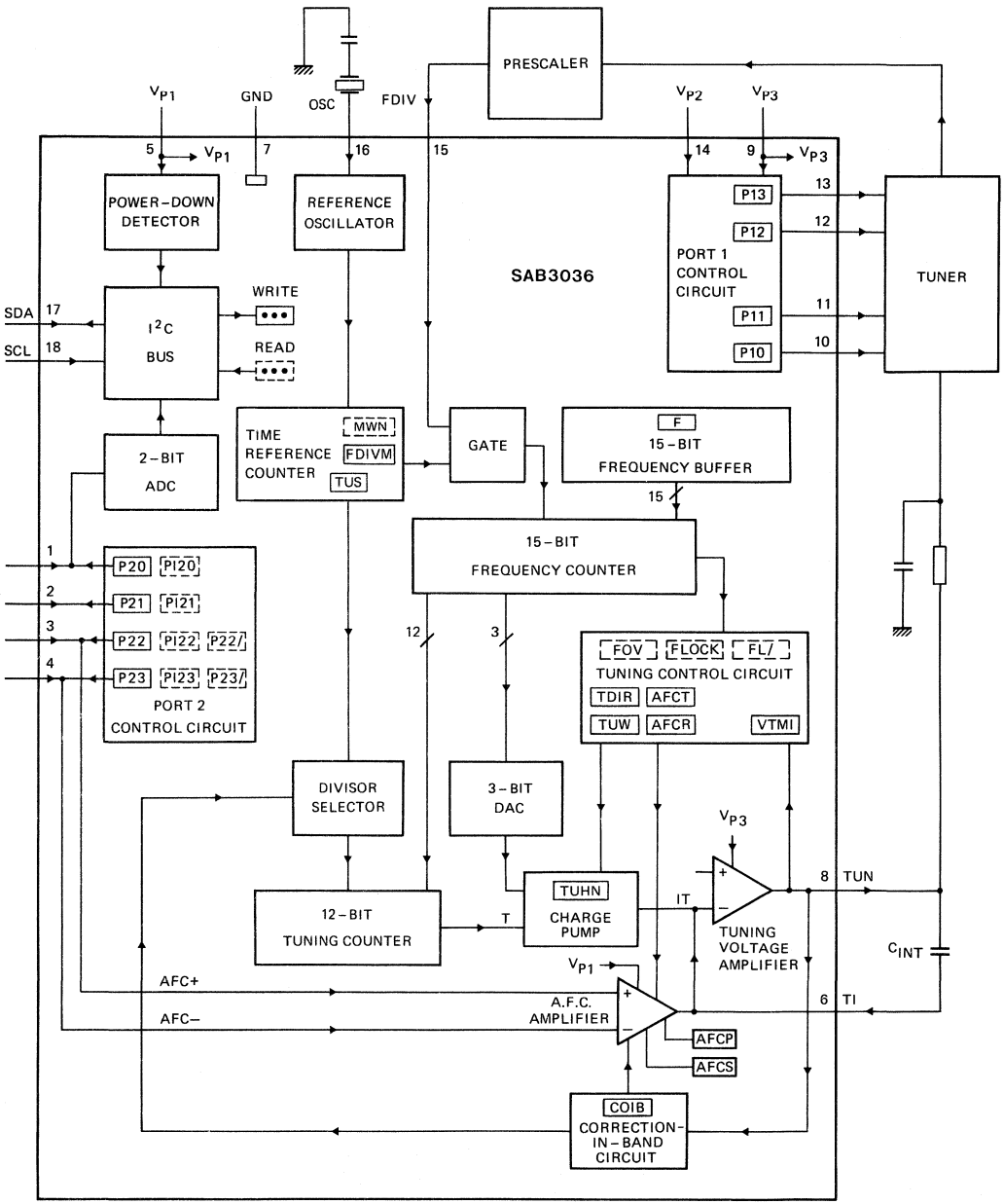


Fig. 1 Block diagram.

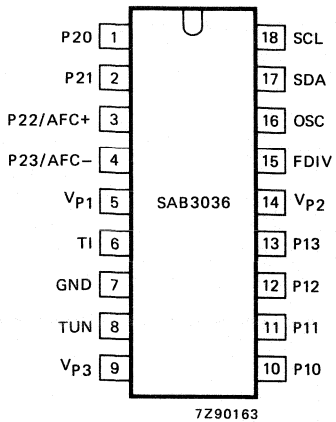


Fig. 2 Pinning diagram.

PINNING

1	P20	general purpose input/output ports
2	P21	
3	P22/AFC+	general purpose input/output ports and a.f.c. inputs
4	P23/AFC−	
5	V_{P1}	+ 12 V supply voltage
6	TI	tuning voltage amplifier inverting input
7	GND	ground
8	TUN	tuning voltage amplifier output
9	V_{P3}	+ 32 V supply for tuning voltage amplifier
10	P10	high-current band-selection output ports
11	P11	
12	P12	
13	P13	
14	V_{P2}	positive supply for high-current band-selection output circuits
15	FDIV	input from prescaler
16	OSC	crystal oscillator input
17	SDA	serial data line, I^2C bus
18	SCL	serial clock line, I^2C bus

FUNCTIONAL DESCRIPTION

The SAB3036 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 $\mu A\ \mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250\ \mu A\ \mu s$ (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals and are connected with the AFC+ and AFC− inputs respectively. The a.f.c. amplifier must be switched off when P22 and/or P23 are used. When a.f.c. is used, P22 and P23 must be programmed HIGH (high impedance state). With the aid of port P20, up to three independent module addresses can be programmed.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

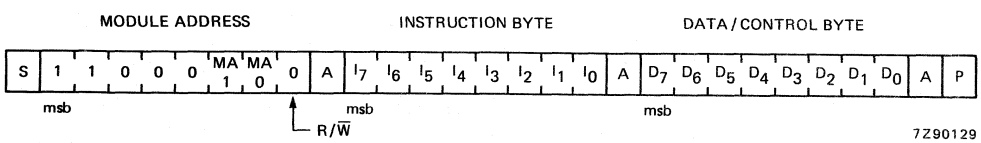


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

OPERATION (continued)

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at $\Delta f = 50$ kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at $C_{INT} = 1\ \mu F$ μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at $\Delta f = 50$ kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

$\Delta f = 50$ kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at $C_{INT} = 1\ \mu F$ mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at: < 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

OPERATION (continued)

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction byte POD (port output data) is shown in Fig. 5, together with the corresponding data/control byte. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

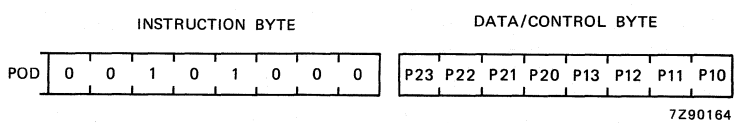


Fig. 5 Control programming.

OPERATION (continued)

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

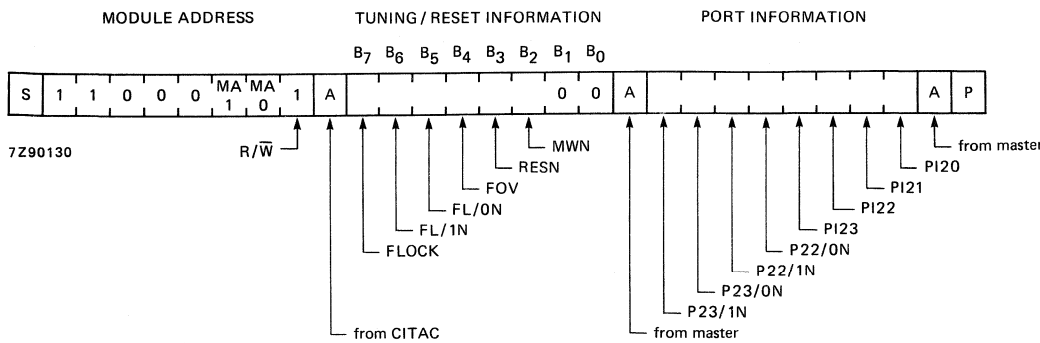


Fig. 6 Information byte format.

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

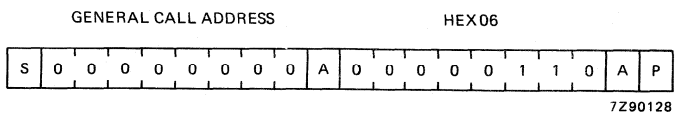


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:

(pin 5)	V_{P1}	−0,3 to + 18 V
(pin 14)	V_{P2}	−0,3 to + 18 V
(pin 9)	V_{P3}	−0,3 to + 36 V
Input/output voltage ranges:		
(pin 17)	V_{SDA}	−0,3 to + 18 V
(pin 18)	V_{SCL}	−0,3 to + 18 V
(pins 1 and 2)	$V_{P20, P21}$	−0,3 to + 18 V
(pins 3 and 4)	$V_{P22, P23, AFC}$	−0,3 to V_{P1}* V
(pin 6)	V_{TI}	−0,3 to V_{P1}* V
(pin 8)	V_{TUN}	−0,3 to V_{P3}* V
(pins 10 to 13)	V_{P1X}	−0,3 to V_{P2}** V
(pin 15)	V_{FDIV}	−0,3 to V_{P1}* V
(pin 16)	V_{OSC}	−0,3 to + 5 V
Total power dissipation	P_{tot}	max. 1000 mW
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature	T_{amb}	−20 to + 70 °C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	14	23	40	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	300	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I^2C bus inputs/outputs					
SDA input (pin 17); SCL input (pin 18)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 17, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 1 to 4, open collector)					
Input voltage HIGH (P20, P21)	V_{IH}	2	–	16	V
Input voltage HIGH (P22, P23) AFC switched off	V_{IH}	2	–	$V_{P1}-2$	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 3, 4)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current (P22 and P23 programmed HIGH)	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 6, 8)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 10 to 13)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 15)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	16	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 1) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification.
After reset has been activated, transmission may only be started after a 50 μs delay.

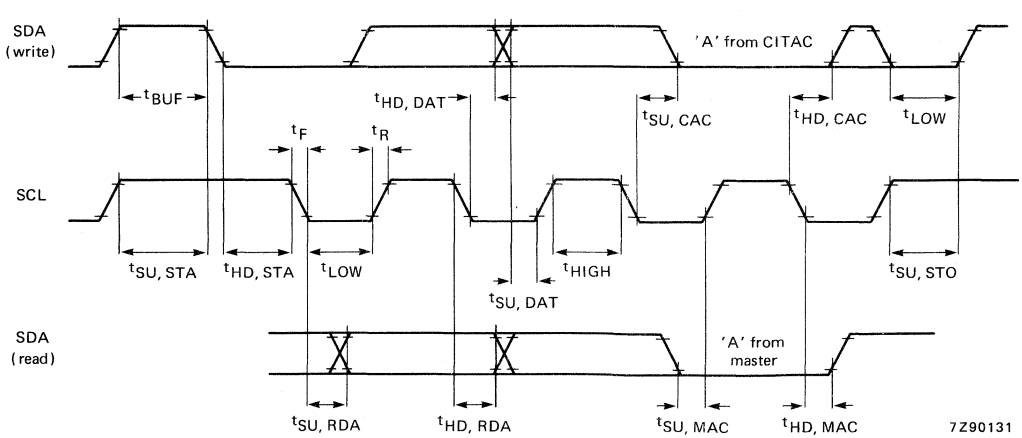


Fig. 8 I²C bus timing SAB3036.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 4 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 4 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages				
(pin 13)	V_{P1}	typ.	12	V
(pin 19)	V_{P2}	typ.	13	V
(pin 14)	V_{P3}	typ.	32	V
Supply currents (no outputs loaded)				
(pin 13)	I_{P1}	typ.	30	mA
(pin 19)	I_{P2}	typ.	0,1	mA
(pin 14)	I_{P3}	typ.	0,6	mA
Total power dissipation	P_{tot}	typ.	380	mW
Operating ambient temperature range	T_{amb}	−20 to +70		°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT 101A).

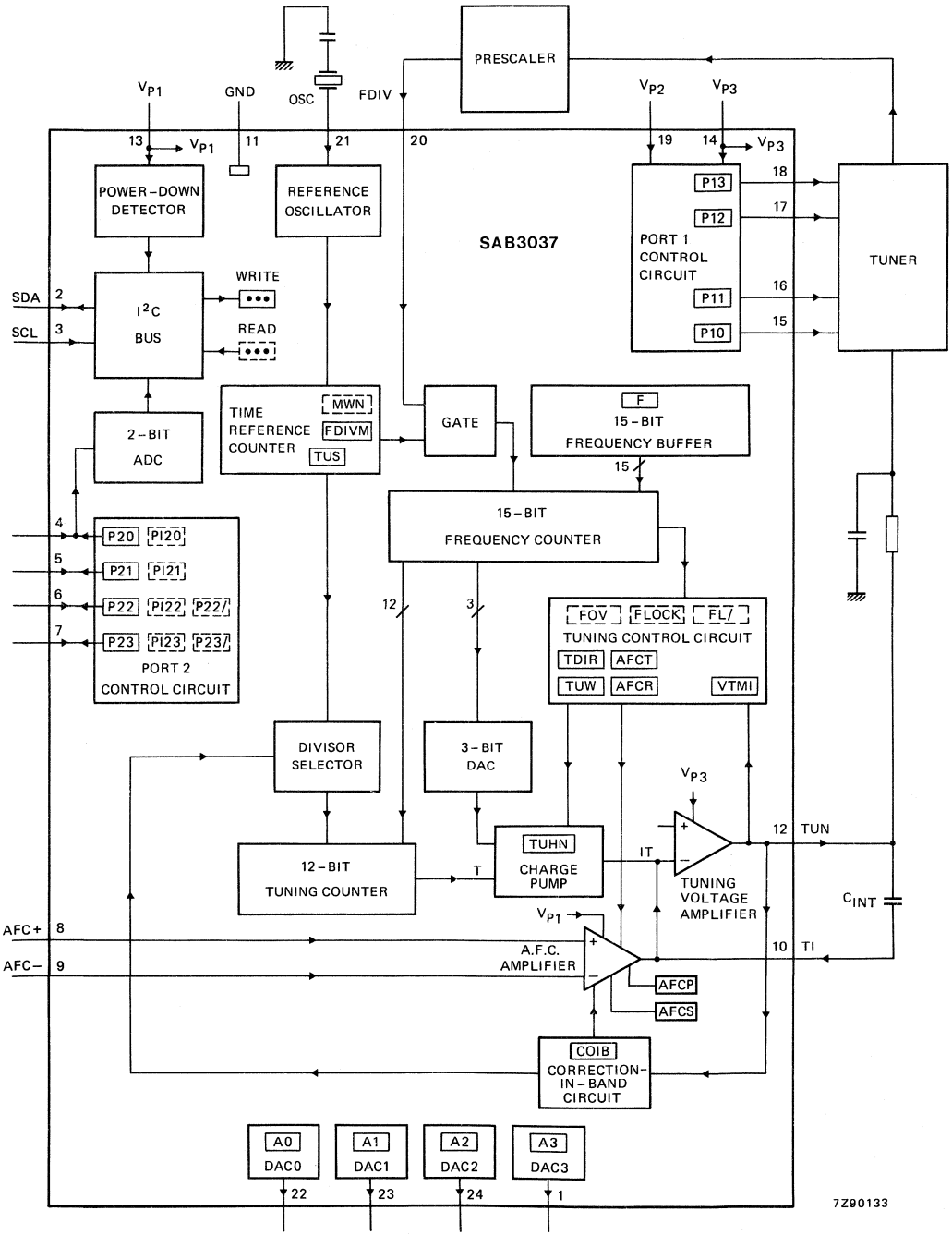


Fig. 1 Block diagram.

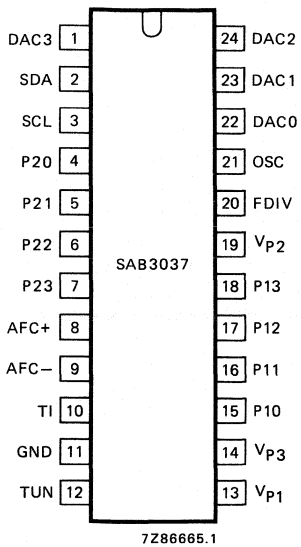


Fig. 2 Pinning diagram.

PINNING

1	DAC3	output of static DAC
2	SDA	serial data line (I²C bus)
3	SCL	serial clock line (I²C bus)
4	P20	general purpose input/output ports
5	P21	general purpose input/output ports
6	P22	general purpose input/output ports
7	P23	general purpose input/output ports
8	AFC+	a.f.c. inputs
9	AFC−	a.f.c. inputs
10	TI	tuning voltage amplifier inverting input
11	GND	ground
12	TUN	tuning voltage amplifier output
13	V_{P1}	+ 12 V supply voltage
14	V_{P3}	+ 32 V supply for tuning voltage amplifier
15	P10	high-current band-selection output ports
16	P11	high-current band-selection output ports
17	P12	high-current band-selection output ports
18	P13	high-current band-selection output ports
19	V_{P2}	positive supply for high-current band-selection output circuits
20	FDIV	input from prescaler
21	OSC	crystal oscillator input
22	DAC0	outputs of static DACs
23	DAC1	outputs of static DACs
24	DAC2	outputs of static DACs

FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analogue converters DAC0 to DAC3 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

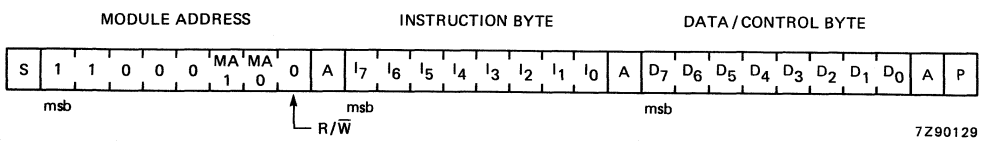


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

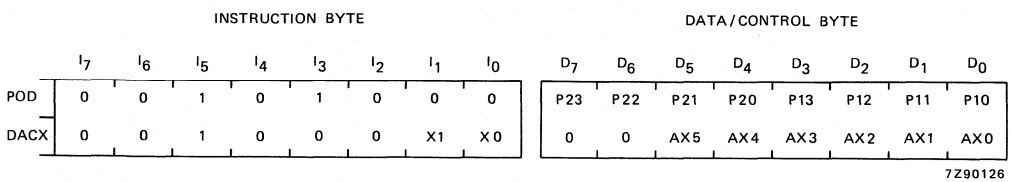


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

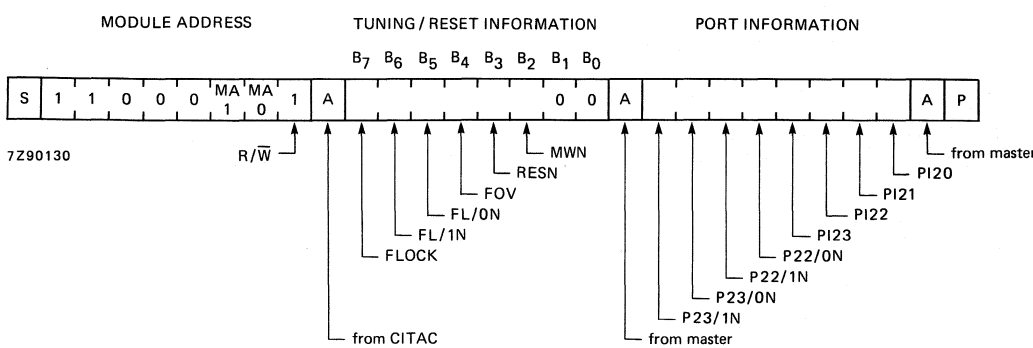


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

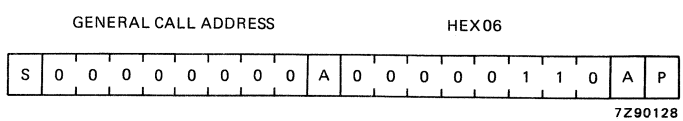


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 13)	V_{P1}	−0,3 to +18	V
(pin 19)	V_{P2}	−0,3 to +18	V
(pin 14)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 2)	V_{SDA}	−0,3 to +18	V
(pin 3)	V_{SCL}	−0,3 to +18	V
(pins 4 to 7)	V_{P2X}	−0,3 to +18	V
(pins 8 and 9)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 10)	V_{TI}	−0,3 to V_{P1}*	V
(pin 12)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 15 to 18)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 20)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 21)	V_{OSC}	−0,3 to +5	V
(pins 1 and 22 to 24)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	18	30	45	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	380	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 2); SCL input (pin 3)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 2, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 4 to 7, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 8, 9)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 10, 12)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current i into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 15 to 18)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 20)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 21)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 3 (pins 22 to 24 and pin 1)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 4) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I^2C BUS TIMING (Fig. 8)

I^2C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I^2C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

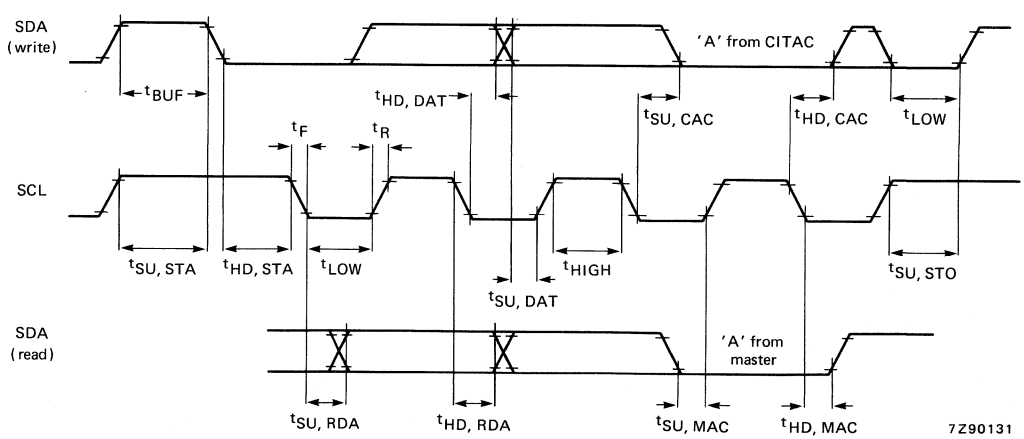


Fig. 8 I^2C bus timing SAB3037.

SENSITIVE 1 GHz DIVIDE-BY-64/DIVIDE-BY-256 SWITCHABLE PRESCALER

GENERAL DESCRIPTION

The SAB6456/SAB6456T is a prescaler for UHF/VHF tuners. It can be switched to divide-by-64 or divide-by-256 by the mode-control (MC) pin. The circuit has an input frequency range of 70 MHz to 1 GHz, has high input sensitivity and good harmonic suppression.

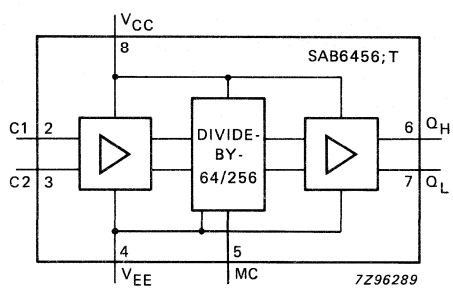


Fig. 1 Block diagram.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 8 to pin 4	V_{CC}	4,5	5,0	5,5	V
Supply current	pin 8	I_{CC}	–	21	–	mA
Input frequency range	pins 2 and 3	f_i	70	–	1000	MHz
Sensitivity to input voltage (r.m.s. value)		$V_{i(rms)}$	–	–	10	mV
Output voltage (peak-to-peak value)	pins 6 and 7	$V_{o(p-p)}$	–	1	–	V
Operating ambient temperature range		T_{amb}	0	–	80	°C

PACKAGE OUTLINES

SAB6456 : 8-lead DIL; plastic (SOT97).
SAB6456T: 8-lead mini-pack (SO8; SOT96A).

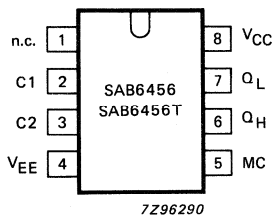


Fig. 2 Pinning diagram.

PINNING

1.	n.c.	not connected
2.	C1	differential inputs
3.	C2	
4.	V_{EE}	ground (0 V)
5.	MC	mode control
6.	Q_H	complementary outputs
7.	Q_L	
8.	V_{CC}	positive supply voltage

FUNCTIONAL DESCRIPTION

The circuit comprises an input amplifier, a divider stage with selectable division ratio and an output stage.

The input amplifier is driven by a sinusoidal signal from the local oscillator of a television tuner. The inputs (C1, C2) are differential and are biased internally to permit capacitive coupling. When driven asymmetrically the unused input should be connected to ground via a capacitor.

The mode-control (MC) input to the divider stage is intended for static control of the division ratio, selection is made as follows:

divide-by-64 : MC pin open-circuit

divide-by-256: MC pin connected to ground

The divider stage may oscillate during no-signal conditions but this oscillation is suppressed when input signals are received.

Two complementary signals (Q_H, Q_L) are provided by the output differential amplifier stage. The voltage-edges of the output signals are slowed internally to reduce harmonics in the television intermediate frequency band.

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection according to specification MIL-883C, class B.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC-134)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 8 to pin 4	V_{CC}	–	–	7,0	V
Input voltage		V_i	–	–	V_{CC}	V
Storage temperature range		T_{stg}	−55	–	+150	°C
Junction temperature		T_j	–	–	+150	°C

THERMAL RESISTANCE

From junction to ambient

8-lead DIL; plastic (SOT-97A)	$R_{th\ j\text{-}a}$	120 K/W
8-lead mini-pack (SO-8; SOT-96A)		
on printed circuit board	$R_{th\ j\text{-}a}$	260 K/W
on ceramic substrate	$R_{th\ j\text{-}a}$	170 K/W

D.C. CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; test IC mounted in a test socket or on a printed circuit board; measurements taken after thermal equilibrium is established

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC} −0,8	V
Supply current		I_{CC}	–	21	28	mA
Mode-control (MC)						
Input voltage LOW (divide-by-256)		V_{IL}	0	–	0,2	V
Input current LOW		$-I_L$	–	25	60	μA
Input voltage HIGH (divide-by-64)	pin 5 open-circuit	V_{IH}	1,4	–	3,0	V

A.C. CHARACTERISTICS

V_{CC} = 4,5 to 5,5 V; V_{EE} = 0 V; T_{amb} = 0 to +80 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity to input voltage (r.m.s. value)	50 Ω system					
	f_i = 70 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 150 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 300 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 500 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 900 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 1000 MHz	$V_{i(rms)}$	–	–	10	mV
Input overload voltage (r.m.s. value)	50 Ω system; f_i = 70 MHz to 1000 MHz	V_i	300	–	–	mV
Input parallel resistance	f_i = 70 MHz	R_i	–	560	–	Ω
	f_i = 1000 MHz	R_i	–	30	–	Ω
Input capacitance	f_i = 70 MHz	C_i	–	5	–	pF
	f_i = 1000 MHz	C_i	–	1,5	–	pF
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC} –0,8	V
Output voltage swing (peak-to-peak value)	f_i = 70 MHz	$V_{o(p\text{-}p)}$	0,8	1,0	1,2	V
	f_i = 1000 MHz; R_L = 820 Ω; C_L = 60 pF	$V_{o(p\text{-}p)}$	0,17	–	–	V
Attenuation of third harmonic at output	f_i = 800 MHz; R_L = 820 Ω; C_L = 60 pF		–15	–23	–	dB
Output unbalance	see Fig. 3	ΔV_o	–	–	0,1	V
Output resistance		R_o	–	500	–	Ω

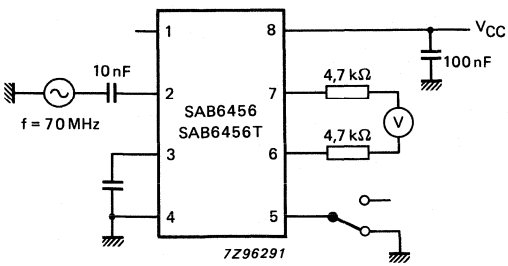


Fig. 3 Test circuit for output unbalance measurement.

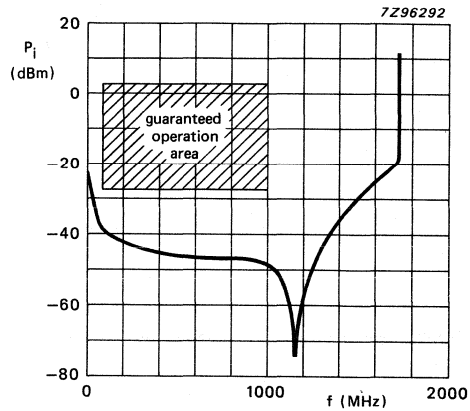


Fig. 4 Typical input sensitivity curve: V_{CC} = 5 V; T_{amb} = 25 °C.

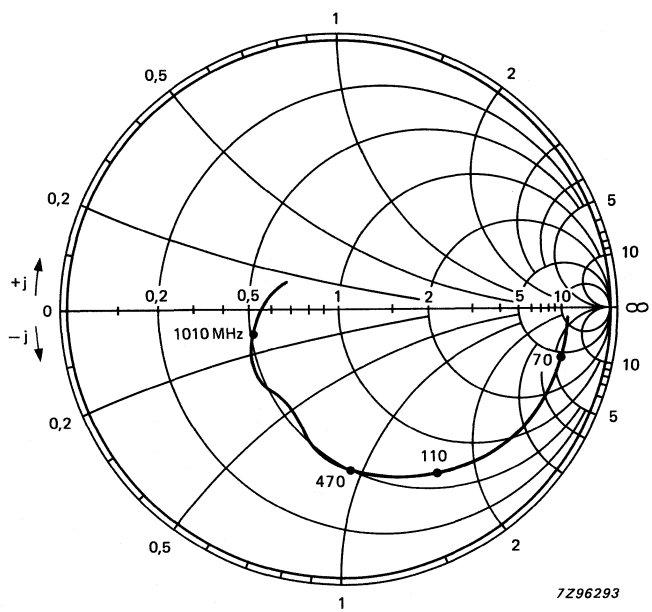


Fig. 5 Smith chart of typical input impedance: $V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 50 Ω.

SENSITIVE 2.6 GHz DIVIDE-BY-2 PRESCALER

GENERAL DESCRIPTION

The SAB8726 is a prescaler for satellite television applications. It has an input frequency range of 1 GHz to 2.6 GHz with high input sensitivity.

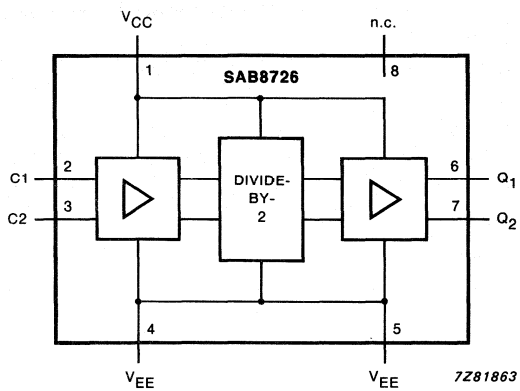


Fig. 1 Block diagram.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 1 to pins 4, 5	V_{CC}	4.5	5.0	5.5	V
Supply current	pin 1	I_{CC}	–	35	–	mA
Input frequency range	pins 2 and 3	f_i	1	–	2.6	GHz
Input sensitivity						
Input voltage (RMS value)		$V_{i(rms)}$	–	–	70	dBm/mV
Output voltage (RMS value)	pins 6 and 7	$V_{o(rms)}$	–	90	–	dBm/mV
Operating ambient temperature range		T_{amb}	0	–	80	°C

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

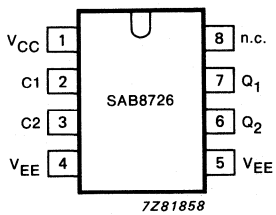


Fig. 2 Pinning diagram.

PINNING

1	V_{CC}	positive supply voltage
2	C1	differential inputs
3	C2	
4	V_{EE}	ground (0 V)
5	V_{EE}	ground (0 V)
6	Q_1	complementary outputs
7	Q_2	
8	n.c.	not connected

FUNCTIONAL DESCRIPTION

This IC is designed to be driven by a sinusoidal 1 GHz to 2.6 GHz signal from the local-oscillator of a satellite TV tuner.

The inputs (C1, C2) are differential and are internally biased to permit capacitive coupling (Fig. 5a). When driven asymmetrically the unused input should be connected to ground via a capacitor (Fig. 5b).

The divider stage will oscillate without an input signal but this oscillation will be suppressed when an input signal within the specified range is applied.

Two complementary signals (Q_1, Q_2) are provided by the output differantial amplifier stage (Fig. 5c).

For asymmetrical output, the unused output should be connected to ground via a 50 Ω resistor and a capacitor (Fig. 5d).

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection in accordance with specification MIL-STD-883C, class A.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (DC)	V_{CC}	–	7.0	V
Input voltage	V_i	0	V_{CC}	V
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 80	°C
Junction temperature	T_j	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a} = 120$ K/W

DC CHARACTERISTICS

V_{CC} = 5 V ± 10%; V_{EE} = 0 V; T_{amb} = 0 to 80 °C; test IC mounted in a test socket or on a printed circuit board; measurements taken after thermal equilibrium is established; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply current		I_{CC}	–	35	45	mA
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC}−0.4	V

AC CHARACTERISTICS

V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 80 °C; f_{in} = 1 to 2.6 GHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Input						
Input frequency range		f_i	1	–	2.6	GHz
Input sensitivity						
Input voltage (RMS value)	50 Ω system					
	f_i = 1 GHz	$V_{i(rms)}$	–	–	–10/70	dBm/mV
	f_i = 2.6 GHz	$V_{i(rms)}$	–	–	–10/70	dBm/mV
Input overload voltage (RMS value)	50 Ω system					
	f_i = 1 GHz	$V_{i(rms)}$	7/500	–	–	dBm/mV
	f_i = 2.6 GHz	$V_{i(rms)}$	7/500	–	–	dBm/mV
Output						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC}–0.4	V
Output voltage level	V_i = 0 dBm; f_i = 2 GHz; R_L = 50 Ω	V_o	–	–8/90	–	dBm/mV
Output resistance		R_o	–	50	–	Ω

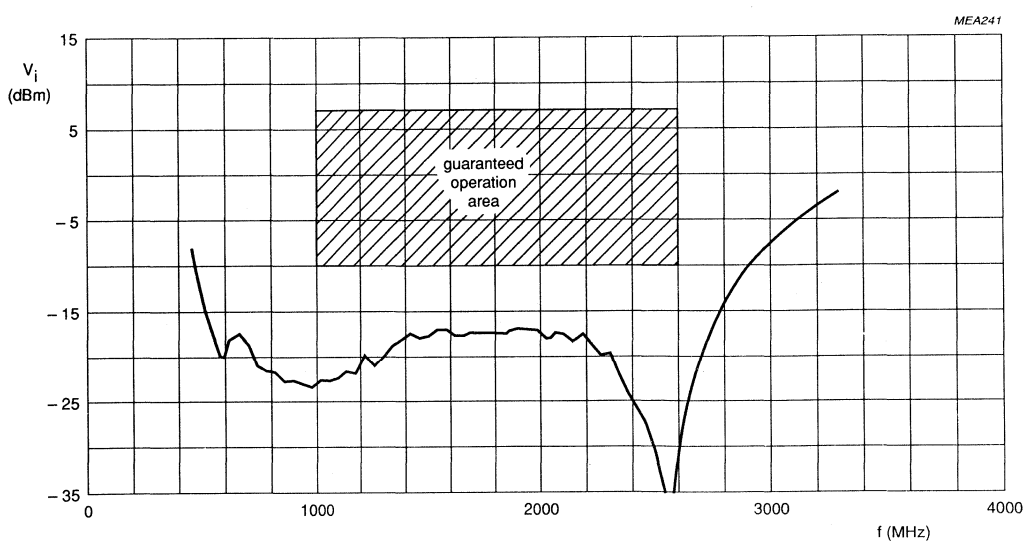


Fig.3 Typical input sensitivity curve: V_{CC} = 5 V; T_{amb} = 25 °C.

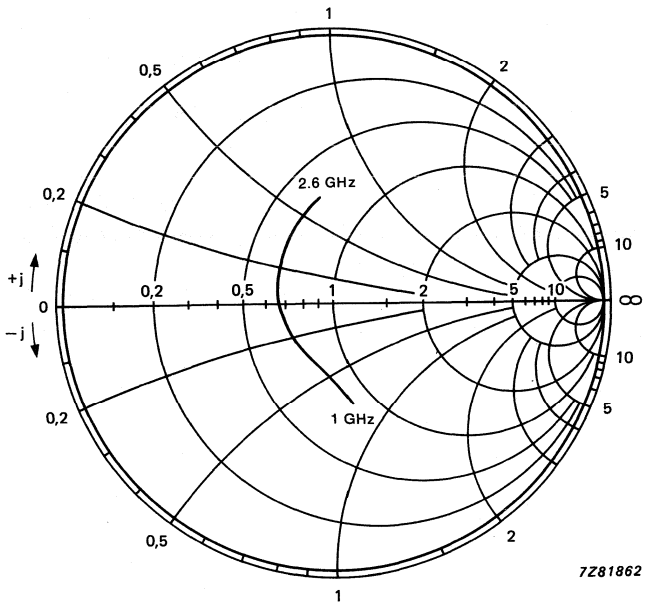
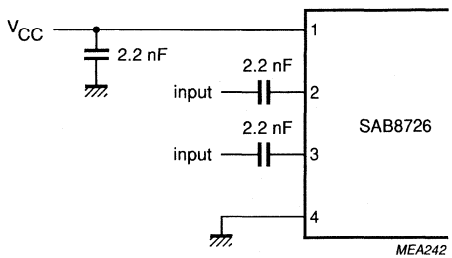
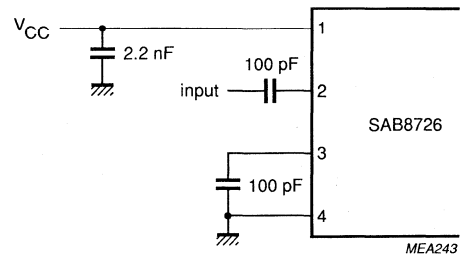


Fig. 4 Smith chart of typical input impedance: input level = −10 dBm; V_{CC} = 5 V; reference value = 50 Ω.

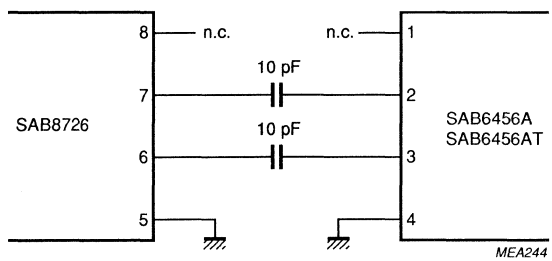
APPLICATION INFORMATION



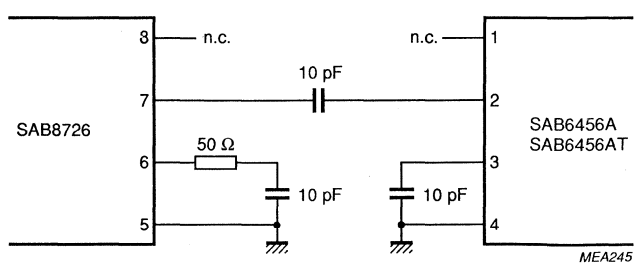
(a) Symmetrical input.



(b) Asymmetrical input.



(c) Symmetrical output.



(d) Asymmetrical output.

Fig. 5 Pin configurations for symmetrical/asymmetrical input and output.

Note to Fig. 5

To minimize possible harmonics the symmetrical output is preferred.

UNIVERSAL DAC (UDAC)

GENERAL DESCRIPTION

The SAD1009 is intended as a peripheral to a microcontroller-based servo system in video cassette recorders. The device relieves the microcontroller of some of the real time functions. These functions include; generation of programmable pulse width signals (duty factor etc.) and accurate measurement of time period signals (tacho signal etc.). The SAD1009 has nine programmable output ports. All functions of the UDAC are programmable. Commands and data from the microcontroller are loaded via a bidirectional bus using a 16-bit format. Data from the time period measurement is transferred to the microcontroller via the same bidirectional bus, also using a 16-bit format. The clock signal for this device is provided by the quartz oscillator of the microcontroller.

Features

- Generation of programmable pulse width signals
- Measurement of time period signals
- All functions are programmable

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4,75	5,0	5,25	V
Inputs						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
Outputs						
Output voltage						
LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = –1,0 mA	V_{OH}	V_{DD} –0,4	–	–	V
Output sink current		I_O	–	–	1,6	mA
Output source current		$-I_O$	–	–	1,0	mA

PACKAGE OUTLINES

SAD1009P: 24-lead DIL; plastic (SOT101A).
SAD1009T: 24-lead mini-pack; plastic (SO24; SOT137A).

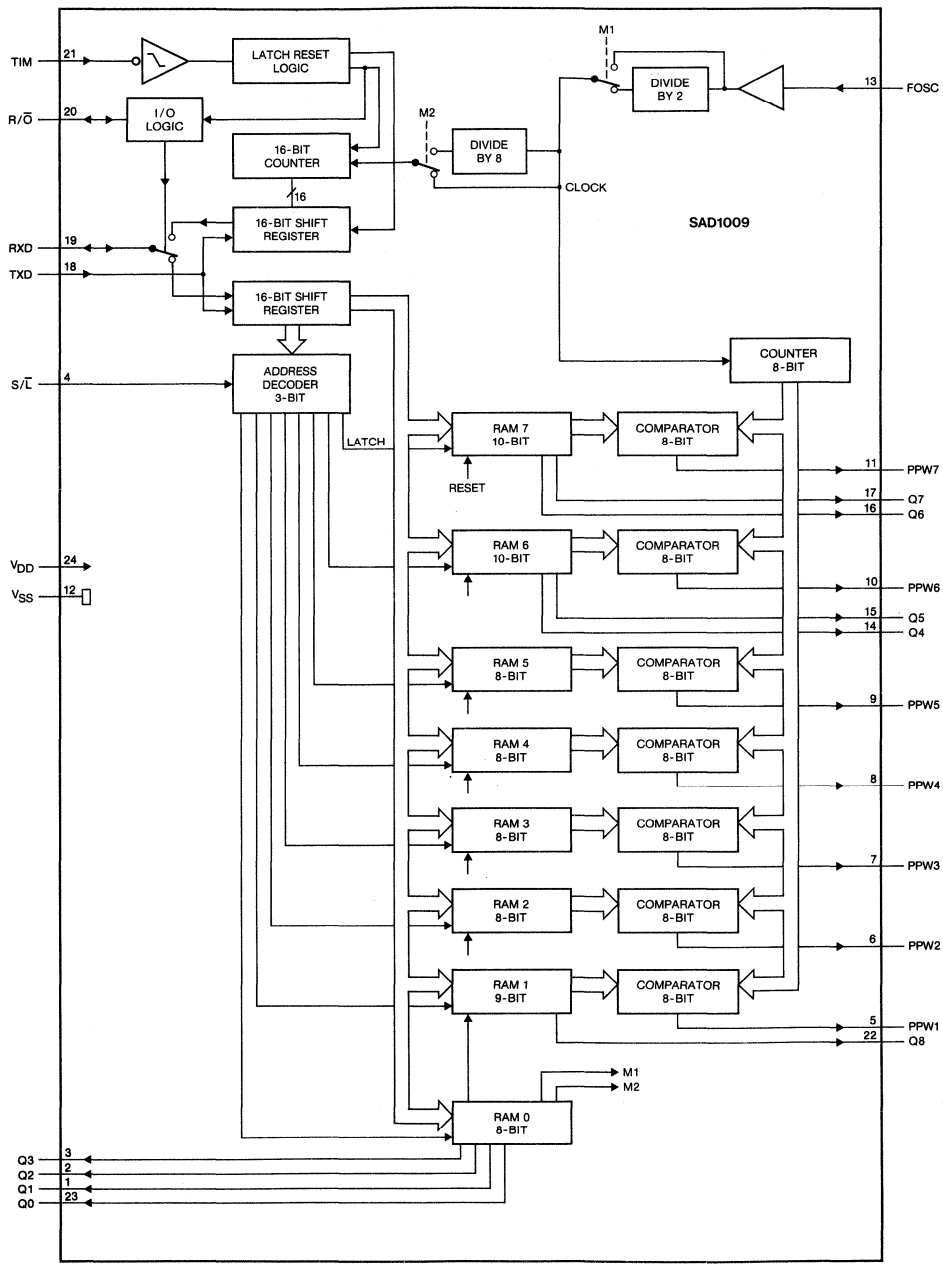


Fig. 1 Block diagram.

PINNING

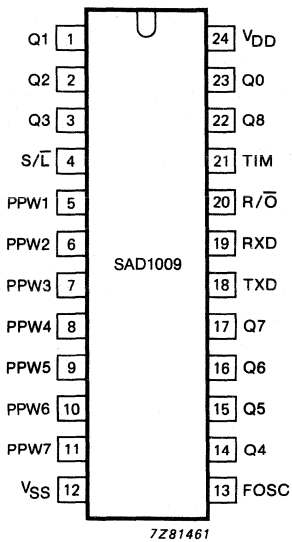


Fig. 2 Pinning diagram.

Power supply

V_{DD}	positive supply voltage (+5 V)
V_{SS}	ground (0 V)

Inputs

S/$\overline{L}$	shift/$\overline{\text{latch}}$ input
FOSC	oscillator input
TXD	serial clock

Special inputs

TIM	timer input

Outputs

Q0 to Q8	programmable output ports
PPW1 to PPW7	programmable pulse width outputs

Input/outputs

RXD	serial data
R/$\overline{O}$	handshake

FUNCTIONAL DESCRIPTION

Loading data

All commands and data are loaded into the SAD1009 via the bidirectional bus (TXD, RXD). The bidirectional bus is compatible with the serial interface of the '8051' microcontroller, using mode 0.

A 16-bit word is used to program a function of the UDAC. The first 3-bits received from the RAM constitute the address and the remaining 13-bits are data (LSB first, MSB last). None of the functions require all 13-bits of data, therefore, 16-bit words contain a number of immaterial bits (x). The programming format is shown in Table 1.

To shift a program word into the input buffer of the UDAC the S/$\overline{L}$ line (shift/latch not) must be HIGH. The contents of the input buffer are transferred to the appropriate RAM on the HIGH-to-LOW transition of the S/$\overline{L}$ signal. When S/$\overline{L}$ is LOW the input buffer is disabled and cannot accept new incoming information. Fig. 3 illustrates the program reception cycle.

Table 1 Programming format

bit	status	PPW1	PPW2	PPW3	PPW4	PPW5	PPW6	PPW7
1	L	H	L	H	L	H	L	H
2	L	L	H	H	L	L	H	H
3	L	L	L	L	H	H	H	H
4	$\overline{\text{RESET}}$	Q8	X	X	X	X	Q4	Q6
5	X	X	X	X	X	X	Q5	Q7
6	X	X	X	X	X	X	X	X
7	X	X	X	X	X	X	X	X
8	X	X	X	X	X	X	X	X
9	Q0	D8	D8	D8	D8	D8	D8	D8
10	Q1	D7	D7	D7	D7	D7	D7	D7
11	Q2	D6	D6	D6	D6	D6	D6	D6
12	Q3	D5	D5	D5	D5	D5	D5	D5
13	X	D4	D4	D4	D4	D4	D4	D4
14	X	D3	D3	D3	D3	D3	D3	D3
15	M1	D2	D2	D2	D2	D2	D2	D2
16	M2	D1	D1	D1	D1	D1	D1	D1

Where:

X : don't care
D1 to D8: data for programming pulse width, D1 = MSB and D8 = LSB

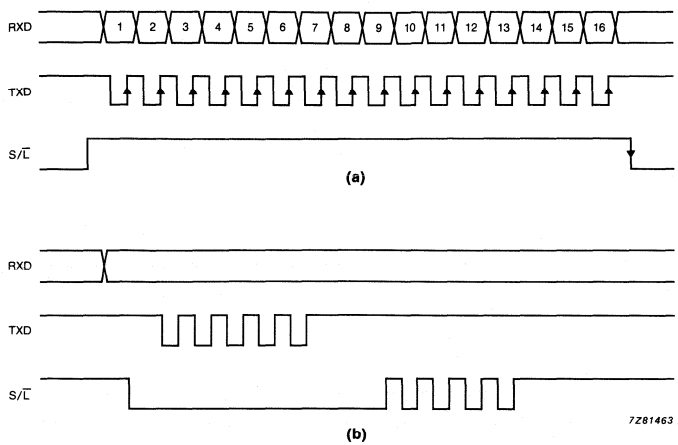


Fig. 3 Program reception cycle: a) normal reception cycle; b) no information is loaded into the input buffer, the RAMs contents remain unchanged.

Pulse width modulated outputs

The UDAC has seven pulse width modulated outputs (PPW1 to PPW7). The output PPW1 is slightly different to outputs PPW2 to PPW7, the difference is explained below. Each output produces a pulse width modulated signal with a duty factor programmable in steps of 1/256 and has a repetition frequency of approximately 23 kHz. These pseudo analogue signals are used to control the capstan and reel drives. Motor control can be performed in the following ways:

- convert the pulse width modulated signal into an analogue signal using filtering and analogue power amplification
- by feeding the pulse width modulated signal to the motor via a power switch and a switch mode filter

To conserve power use the second method for control of the capstain and reel motors. For the scanner control two outputs are available, so that by weighted addition a higher resolution can be achieved.

PPW1 is also an 8-bit programmable output, with a repetition frequency of 23 kHz. The difference is the low frequency contents of the signal are reduced by changing the distribution of the HIGH and LOW level portions. This redistribution means that a filter with two poles; each at 43 μs, is sufficient to reduce the peak-to-peak ripple to less than 1 LSB. This output is for use in applications where long filter delays are not tolerated.

Clock frequency

The clock signal of the UDAC is derived from the quartz oscillator of the microcontroller. The clock frequency should not exceed 6 MHz. The device also contains a programmable 'divide by two' circuit which allows these frequencies to be doubled, thus 6 MHz or 12 MHz microcontrollers can be used. The FOSC signal can be divided by two using bit M1 of RAM 0 (see Table 2).

Table 2 UDAC adjustment

bit M1	quartz frequency (MHz)
L	12
H	6

Programmable output ports

A total of nine output ports can be programmed to supply a HIGH or LOW level signal. Four of these outputs (Q4 to Q7) are intended to supply information about the breaking and direction of the capstan and reel motors, therefore these output ports must be programmed at the same time as the pulse widths of PPW6 and PPW7. Output port Q8 is programmed at the same time as PPW1. The other four output ports (Q0 to Q3) are programmed by RAM 0.

Measurement of the time period

To facilitate accurate measurement of the time period (falling edge to falling edge) of a signal applied to TIM, the UDAC contains a 16-bit counter and a buffer to store the contents of the previous counter measurement. The counter operates at a frequency of $f_{CLOCK}/2$ or $f_{CLOCK}/16$, the counter can be programmed using bit M2 of RAM 0. This timer can record periods of up to 21,8 ms and 175 ms respectively (see Table 3). When the time period is too long and the timer overflows, the microcontroller is loaded with a hex 'FFFF' when it reads the time period after the next pulse.

Table 3 Counter frequency

M2	division ratio	time period (max.)	frequency	resolution
L	2	21,8 ms	46 Hz	333 ns
H	6	175 ms	5,7 Hz	2,67 μs

Data from the timer can be transferred to the microcontroller via a bidirectional bus when the handshaking signal pin R/$\overline{O}$ is pulled LOW by the microcontroller. The LSB is transferred first and the MSB last. After the data has been transferred pin R/$\overline{O}$ remains in a LOW state (pulled down by the UDAC) until a new measurement of the time period is concluded. Note that each measurement of a time period can only be read once. After the next input pulse the 'data ready' state is signalled to the microcontroller by releasing the R/$\overline{O}$ pin, so that the microcontroller reads a HIGH level on this pin.

Note

During the 'data not ready' state the R/$\overline{O}$ is in a low impedance state and during the 'data ready' state the R/$\overline{O}$ is in a high impedance state (= HIGH). To speed up the transition from LOW-to-HIGH, the high impedance state is preceded by a short period of low impedance HIGH state.

Reset

The device can be reset by software by loading a LOW into the $\overline{\text{RESET}}$ bit of RAM 0. The effect of this reset is as follows:

- RAM 0; not influenced
- RAM 1; duty factor = 50%, Q8 = LOW
- RAM 2 to 5; duty factor = 50%
- RAM 6 to 7; duty factor = 0 and Q4 to Q7 = LOW

The reset is de-activated automatically on the next LOW-to-HIGH transition of S/$\overline{L}$. This allows new program information to be loaded and transferred to any RAM without having finished the reset. Due to RAM 0 not being influenced by the reset, the data required after the reset can be loaded along with the reset command.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	–	7	V
Input voltage range	note 1	V_I	−0,5	V_{DD} + 0,5	V
Input voltage at S/$\overline{L}$		$V_{4\text{-}12}$	−0,5	V_{DD} + 2,0	V
D.C. current into any input		$\pm I_I$	–	10	mA
D.C. current from any output		$\pm I_O$	–	10	mA
D.C. current into V_{DD}		$\pm I_I$	–	25	mA
D.C. current into V_{SS}		$\pm I_I$	–	25	mA
Total power dissipation	note 2	P_{tot}	–	200	mW
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−20	+70	°C

Notes to ratings

1. Input voltage should not exceed 7 V unless otherwise specified.
2. Diminishes by 5 mW/K from 60 °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{DD} = 4,75 to 5,25 V; T_{amb} = −20 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4,75	5,0	5,25	V
Supply current range	$V_O = V_{DD}$, I_O = 0 mA on all outputs; $V_I = V_{SS}$ on all inputs	I_{DD}	–	100	–	μA
TXD, RXD, S/$\overline{L}$, R/$\overline{O}$						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current	note 1	$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
RXD, R/$\overline{O}$, Q0 to Q7						
Output voltage	note 2					
LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = −1,0 mA	V_{OH}	V_{DD}−0,4	–	–	V
Output sink current		I_O	–	–	1,6	mA
Output source current		$-I_O$	–	–	1,0	mA
FOSC						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF

D.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RXD	used as input					
Input leakage current		$\pm I_I$	–	–	10	μA
TIM						
Input voltage						
LOW		V_{IL}	–	–	$0,3 \times V_{DD}$	V
LOW	V_{DD} = 5 V at 20 °C	V_{IL}	–	1,8	–	V
HIGH		V_{IH}	$0,7 \times V_{DD}$	–	–	V
HIGH	V_{DD} = 5 V at 20 °C	V_{IH}	–	2,9	–	V
Hysteresis	used as input	V_{hys}	–	730	–	mV
R/$\overline{O}$	used as input					
Output resistance		R_O	500	–	1000	Ω
Input leakage current		$\pm I_I$	–	–	10	μA
R/$\overline{O}$	used as output; open drain output; note 3; see Fig. 7					
Output voltage						
LOW	I_{OL} = 0,4 mA	V_{OL}	–	–	0,8	V
HIGH	I_{OH} = –0,4 mA	V_{OH}	$V_{DD}-0,8$	–	–	V
PPW1 to PPW7						
Output voltage						
LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = –4 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output sink current		I_O	–	–	4	mA
Output source current		$-I_O$	–	–	4	mA

Notes to the d.c. characteristics

1. This value applies to TXD and S/$\overline{L}$, the input leakage current for RXD and R/$\overline{O}$ is shown above.
2. This value applies to RXD and Q0 to Q7, the output voltage for R/$\overline{O}$ is shown above.
3. After a LOW-to-HIGH transition of the R/$\overline{O}$ output, the port is held HIGH for approximately one clock cycle. This low impedance HIGH period is followed by the high impedance OFF-state.

A.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
RXD, R/$\overline{O}$, Q0 to Q7						
Output transition time	C_L = 50 pF					
LOW-to-HIGH		t_{TLH}	–	–	30	ns
HIGH-to-LOW		t_{THL}	–	–	30	ns
FOSC						
Maximum pulse frequency	M1 = L	f_{max}	–	–	12	MHz
	M1 = H	f_{max}	–	–	6	MHz
Minimum pulse width						
LOW		t_{WL}	20	–	–	ns
HIGH		t_{WH}	20	–	–	ns
TXD						
Pulse frequency		f_{max}	–	–	6	MHz
Pulse width						
LOW		t_{WL}	50	–	–	ns
HIGH		t_{WH}	50	–	–	ns
RXD	used as input; see Fig. 5					
Set-up time						
RXD to TXD		t_{SURXD}	50	–	–	ns
Hold time						
RXD to TXD		t_{HDRXD}	50	–	–	ns
RXD	used as output; see Fig. 6					
Propagation delay						
TXD to RXD		t_{PRXD}	–	–	50	ns
R/$\overline{O}$ to RXD		$t_{PR/O}$	–	–	50	ns
S/$\overline{L}$	see Fig. 7					
Pulse width LOW						
Set-up time						
TXD to S/$\overline{L}$		t_{SUTXD}	50	–	–	ns
Hold time						
TXD to S/$\overline{L}$		t_{HDTXD}	50	–	–	ns
Propagation delay						
S/$\overline{L}$ to Q0 - Q7		t_p	–	–	50	ns
TIM						
Pulse width						
LOW	M2 = LOW	t_{WL}	700	–	–	ns
LOW	M2 = HIGH	t_{WL}	5,4	–	–	μs
HIGH		t_{WH}	100	–	–	ns

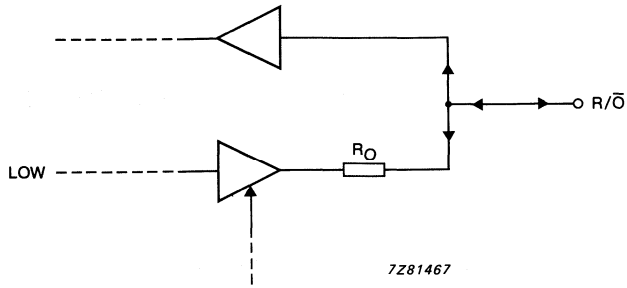


Fig. 4 Equivalent R/$\overline{O}$ output port.

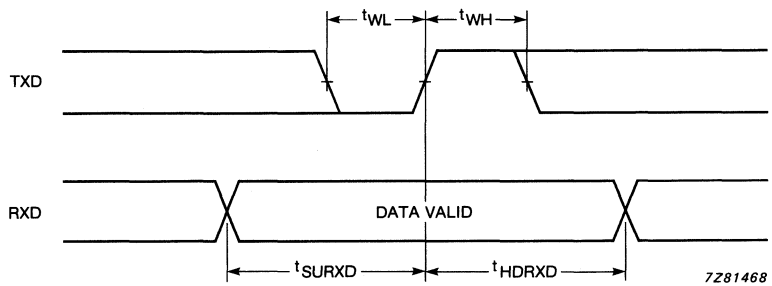


Fig. 5 RXD input waveform.

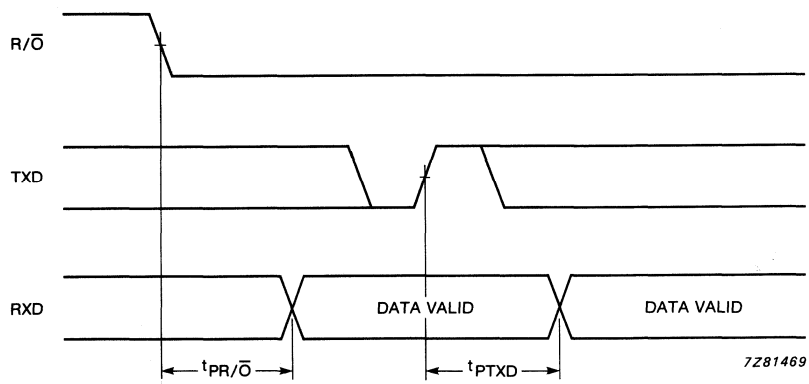


Fig. 6 RXD output waveform.

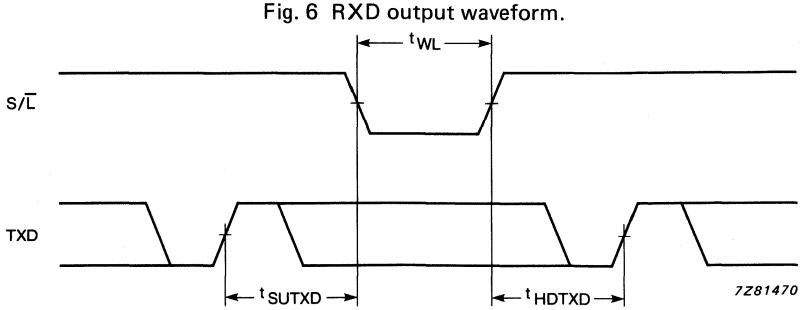


Fig. 7 S/$\overline{L}$ input waveform.

MULTI-NORM PULSE-PATTERN GENERATOR

GENERAL DESCRIPTION

The SAD1019 is part of a frame transfer image sensor camera system which uses the NXA series of frame transfer image sensors. The device provides the vertical transport pulses necessary, for the operation of the frame transfer image sensors and a start-stop signal for the horizontal clock generator. The drive pulses and clock signals for the SAD1019 are provided by the universal sync generator (SAA1043).

Features

- Vertical transport pulses for the image region and storage region of the image sensor during field blanking (ϕ_A and ϕ_B pulses)
- Colour separation and transport of one line of sensor information to the output register during line blanking (ϕ_B, TG and ϕ_C pulses)
- Other additional pulses required for the control and processing in the frame transfer image sensor camera

PACKAGE OUTLINES

SAD1019: 24-lead DIL; plastic (SOT101B).
SAD1019T: 24-lead mini-pack; plastic (SO24; SOT137A).

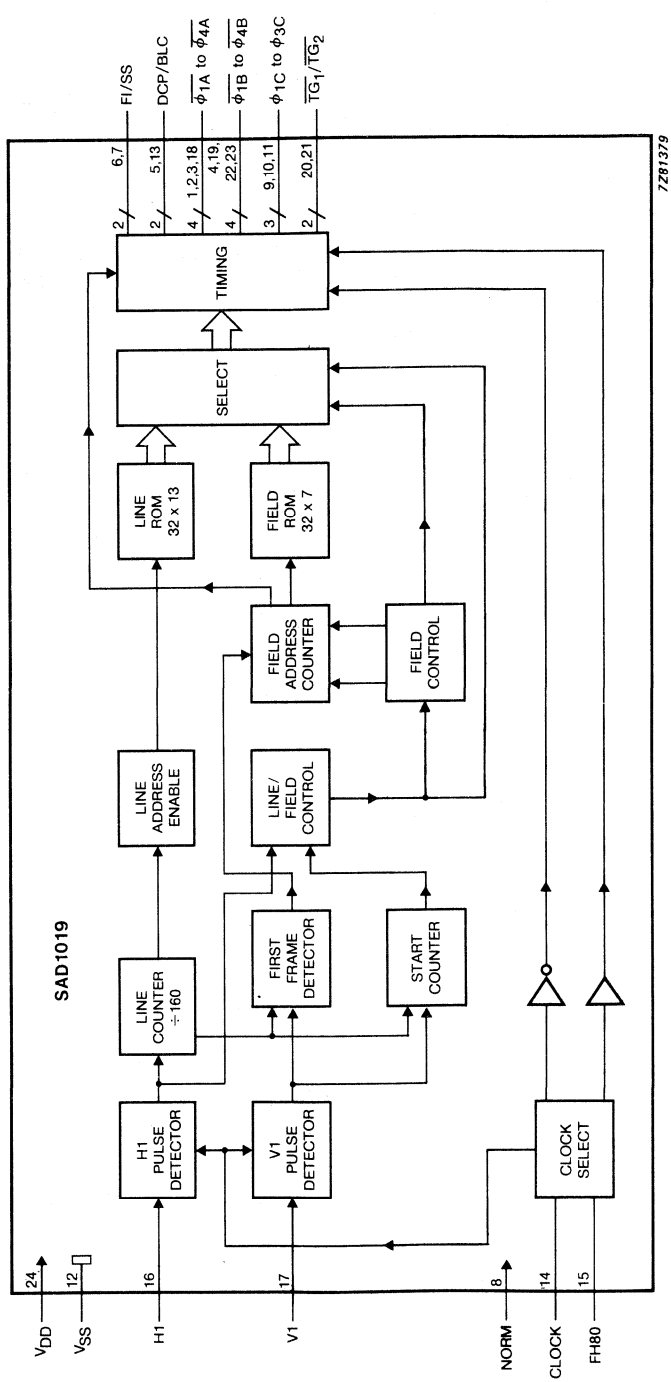


Fig.1 Block diagram.

PINNING

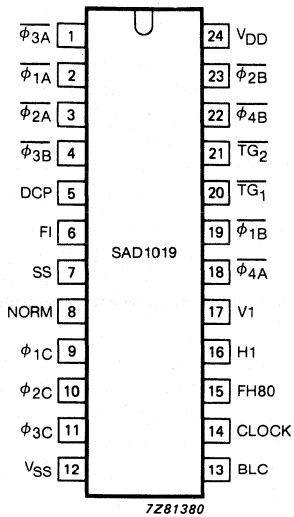


Fig.2 Pinning diagram.

Power supplies

V_{DD}	positive supply voltage (+ 5 V)
V_{SS}	ground (0 V)

Inputs (CMOS)

CLOCK	clock input from SAA1043, typ. 2.5 MHz (625 lines) or typ. 2.51748 MHz (525 lines). 5 MHz mode, typ. 5 MHz (625 lines) or 5.03496 MHz (525 lines)
FH80	clock input from SAA1043, typ. 1.25 MHz (625 lines) or 1.25874 MHz (525 lines)
H1	H1 input from SAA1043, typ. 15.625 kHz (625 lines) or typ. 15.734 kHz (525 lines)
V1	V1 input from SAA1043, typ. 50 Hz (625 lines) or 59.94 Hz (525 lines)
NORM	norm-selection input, 625 lines = LOW, 525 lines = HIGH

Outputs (CMOS push-pull)

$\overline{\phi 1A}$ to $\overline{\phi 4A}$	sensor image section control to drivers
$\overline{\phi 1B}$ to $\overline{\phi 4B}$	sensor storage section control to drivers
$\phi 1C$ to $\phi 3C$	low frequency outputs for transport pulses to pixel oscillator
DCP	DC clamp pulse
FI	frame identification
SS	start/stop for pixel generator
BLC	black-level clamping
$\overline{TG_1}$ and $\overline{TG_2}$	transfer gate control to drivers

FUNCTIONAL DESCRIPTION

625 line mode (NORM = LOW, see Figs 3 to 7)

One complete cycle of the multi-norm pulse-pattern generator (MNPPG) occurs after a command from the synchronization pulse generator (SYN). This cycle consists of 294 line cycles which are used to read out the sensor information followed by transport of the integrated information from the image area to the storage area of the sensor. Once this cycle has been completed the device enters into a 'wait' status period which lasts until the device receives a start command from the SYN.

The cycle is restarted with a V-pulse from the SYN. The falling edge of this pulse is detected in the MNPGG and results in a reset of the start counter as well as providing the field information (field 1/2). The start counter counts 11 lines and then the line cycle information is read from the line ROM. The start of the line cycle occurs at line 22 in frame 1 and line 335 in frame 2. The H1 pulse of the SYN controls the position of the line cycle with respect to the SYN pulses. The H1 pulse sets the correct value in the line counter of the MNPPG.

The control counter counts the number of line cycles and switches the line cycle to field cycle after 294 lines (in both fields), then the field cycle information is read from the field ROM. The control counter was reset before the switch over had taken place, it now counts the field cycles. The field cycle lasts for 294 cycles of the $\overline{\phi 4B}$ pulse and then the device enters the wait status period again.

The device will continue to operate in the manner described, until the overall system is switched off.

525 line mode (NORM = HIGH)

The basic operation is identical except for variations in the start points and number of transports (see Figs 8 to 12).

Operating modes

Synchronization generator (SAA1043)

The H1 pulse from the SAA1043, due to internal delays, is out of phase with the MNPPG clock signal. The following method is used to obtain the correct phase relationship between the H1 pulse and the MNPPG output. The H1 pulse and the FH80 are clocked into a flip-flop, at the output of the flip-flop the timing of the H1 and FH80 signals are in phase. The output of the flip-flop is sampled with that of the CLOCK, which is in phase with the FH80. In this way a reliable fixed phase relationship between SYN and MNPPG is obtained.

Other operating modes

- single 2.5 MHz operation:
  If another synchronization pulse generator is used, in which an H1 pulse is in phase with the CLOCK, a single 2.5 MHz clock signal can be used.

  Connect the 2.5 MHz to the CLOCK and with delay circuitry (RC elements, 50 ns approx.) to FH80.
- single 5 MHz operation:
  If another synchronization pulse generator is used, in which an H1 pulse is in phase with the CLOCK, a single 5 MHz clock signal can be used.

  Connect the 5 MHz to the CLOCK and connect FH80 to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 24)	V_{DD}	−0.5	+ 7.0	V
Supply current (pin 24)	I_{DD}	−	50	mA
Supply current (pin 12)	I_{SS}	−	50	mA
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	−	10	mA
Output current	$\pm I_O$	−	10	mA
Total power dissipation per package	P_{tot}	−	500	mW
Power dissipation per output	P_O	−	25	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0.5 V not to exceed 7.0 V.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 25 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Current						
Supply current	on all outputs; I_O = 0 mA	I_{DD}	–	–	10	μA
Inputs H1, V1, NORM, CLOCK and FH80						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
Input voltage LOW	CMOS compatible	V_{IL}	–	–	$0.3V_{DD}$	V
Outputs						
Output voltage HIGH	all outputs except BLC; $-I_O$ = 0.8 mA; V_{DD} = 5 V	V_{OH}	–	–	$V_{DD}-0.5$	V
Output voltage LOW	all outputs except BLC; I_O = 2.9 mA; V_{DD} = 5 V	V_{OL}	–	–	0.5	V
Black level clamping (BLC)						
Output voltage HIGH	$-I_O$ = 2.6 mA; V_{DD} = 5 V	V_{OH}	–	–	$V_{DD}-0.5$	V
Output voltage LOW	I_O = 2.9 mA; V_{DD} = 5 V	V_{OL}	–	–	0.5	V

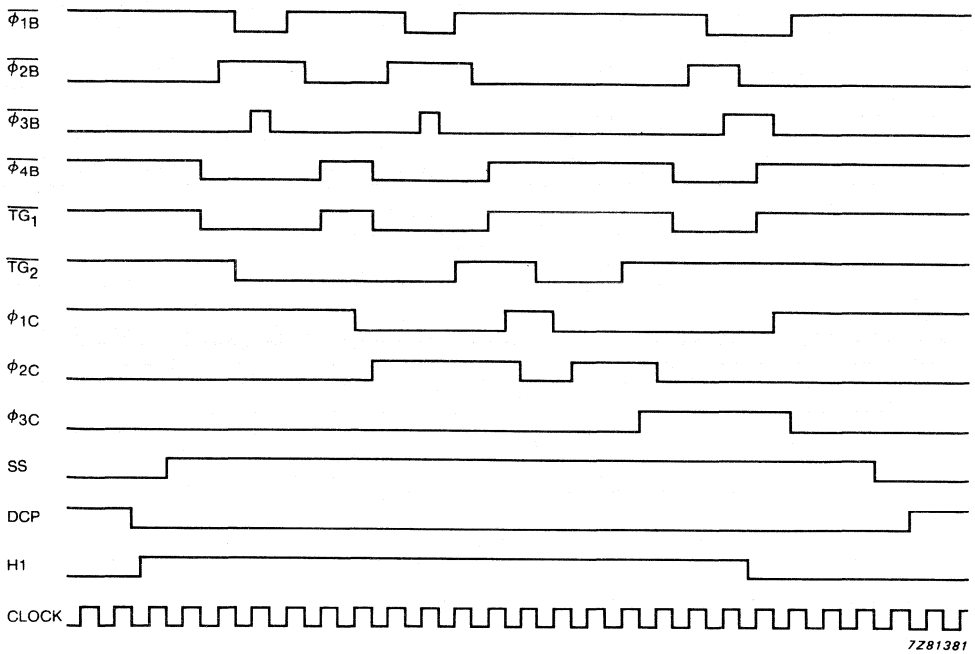
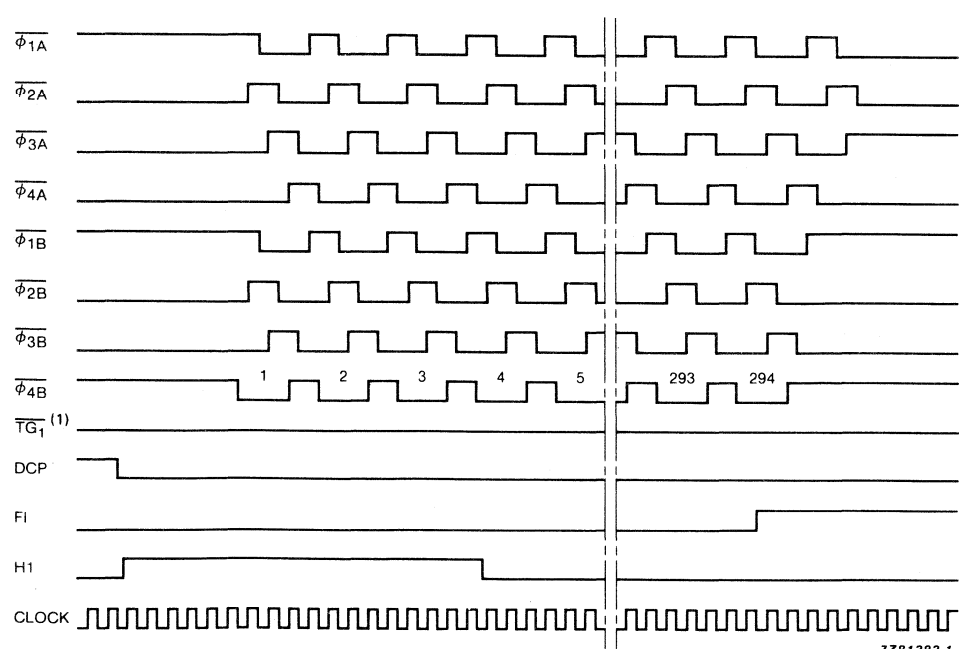
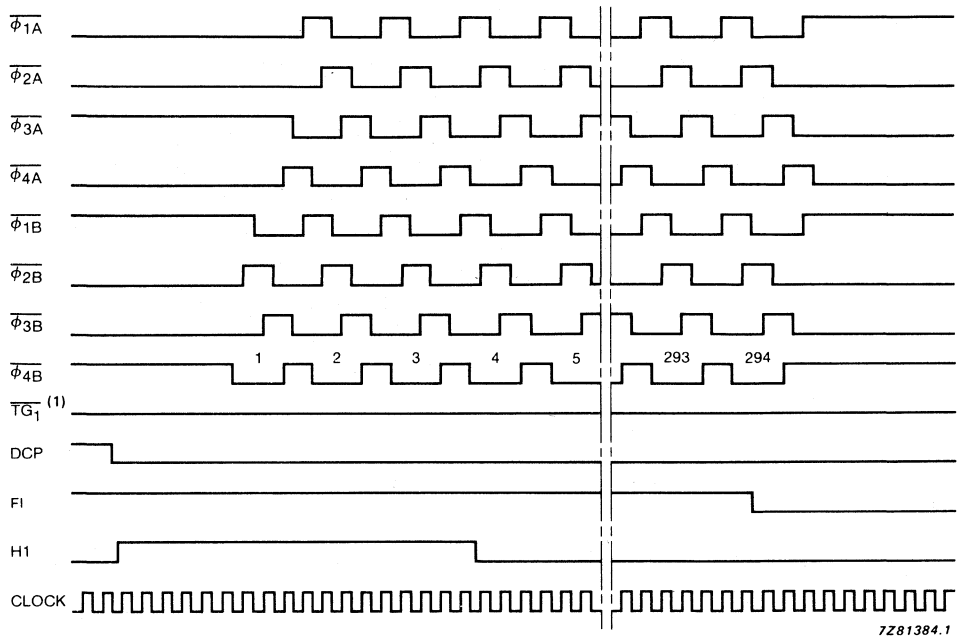


Fig.3 Line transport (625 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.4 Image sensor transport, field 2 (625 lines)



(1) $\overline{TG_1}$ = HIGH state.

Fig.5 Image sensor transport, field 1 (625 lines).

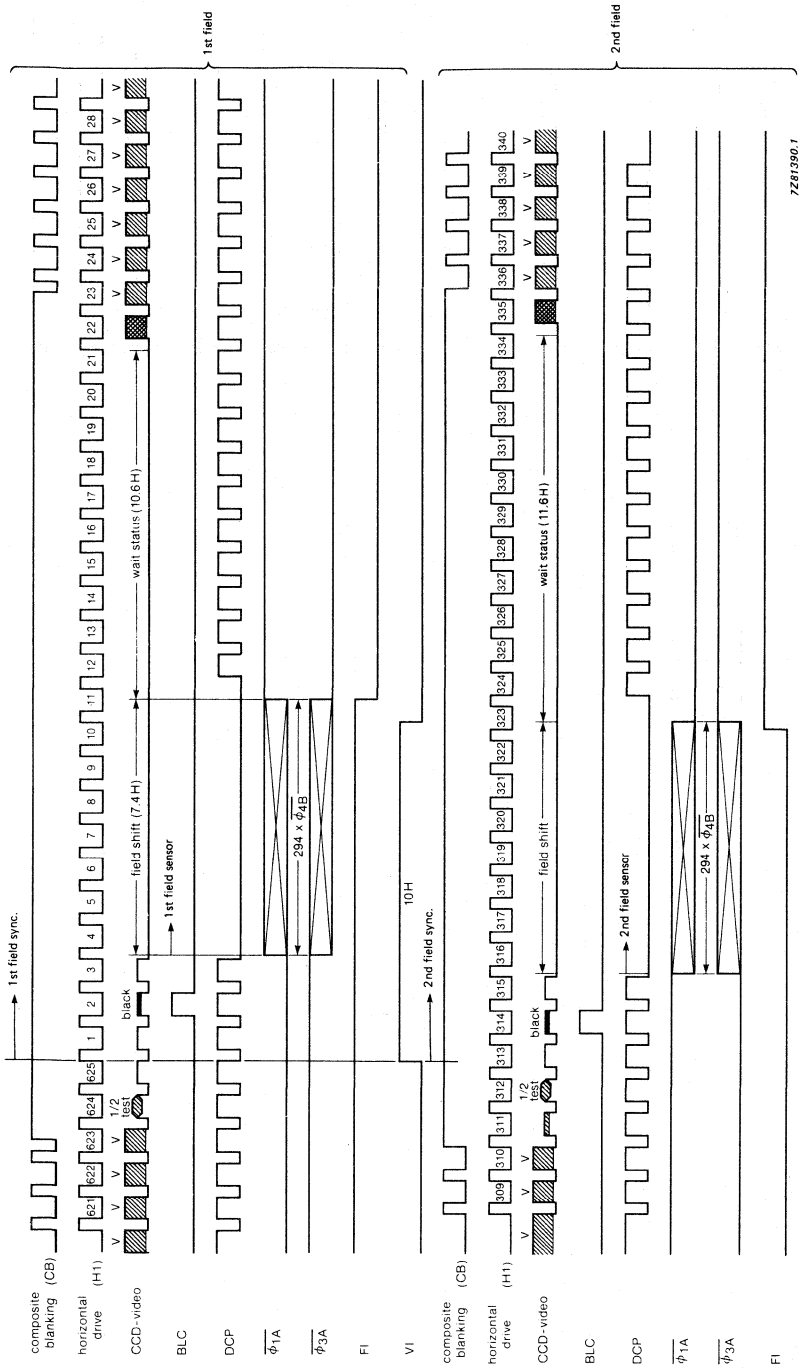


Fig.6 Pulse pattern during field blanking (625 lines).

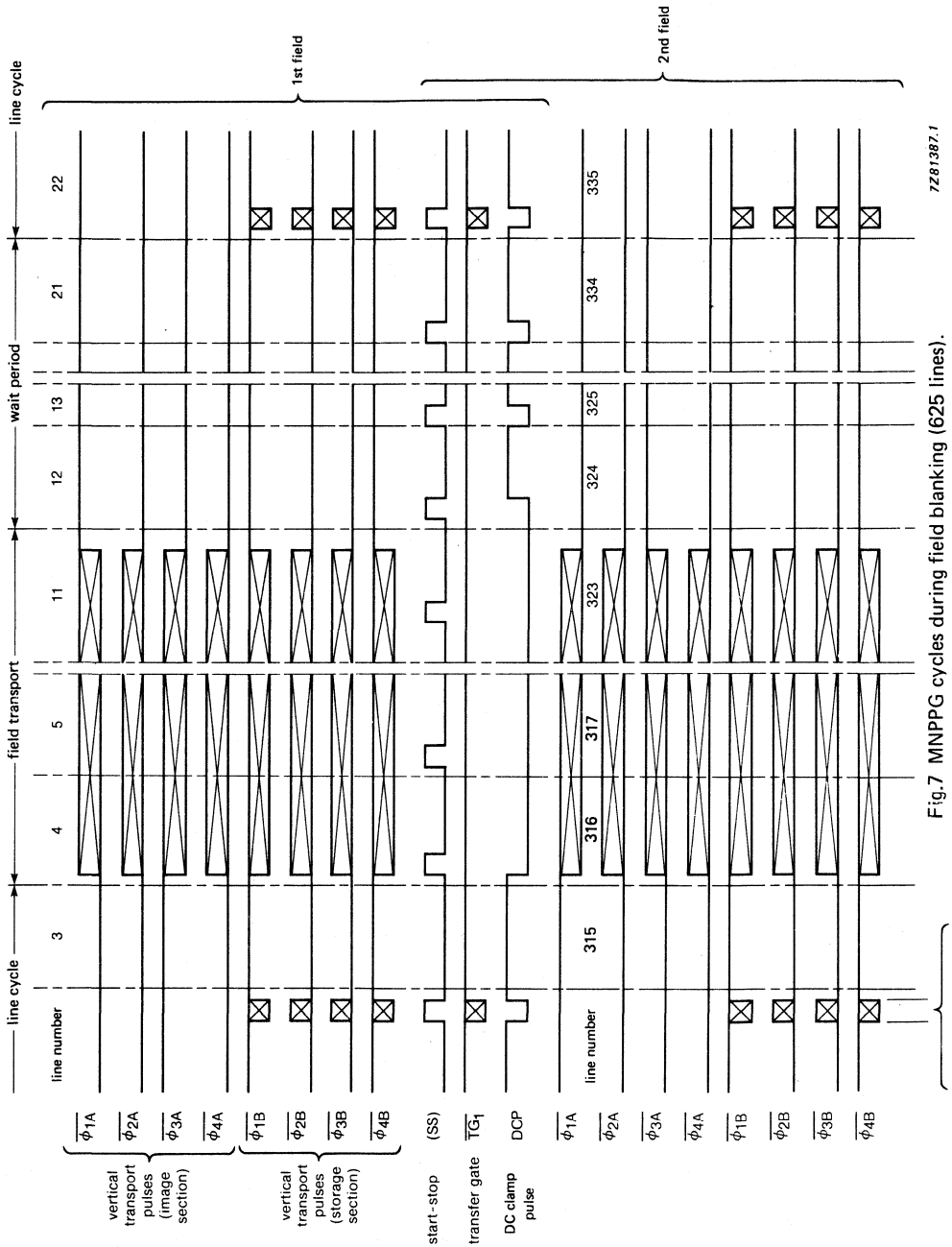


Fig.7 MNPPG cycles during field blanking (625 lines).

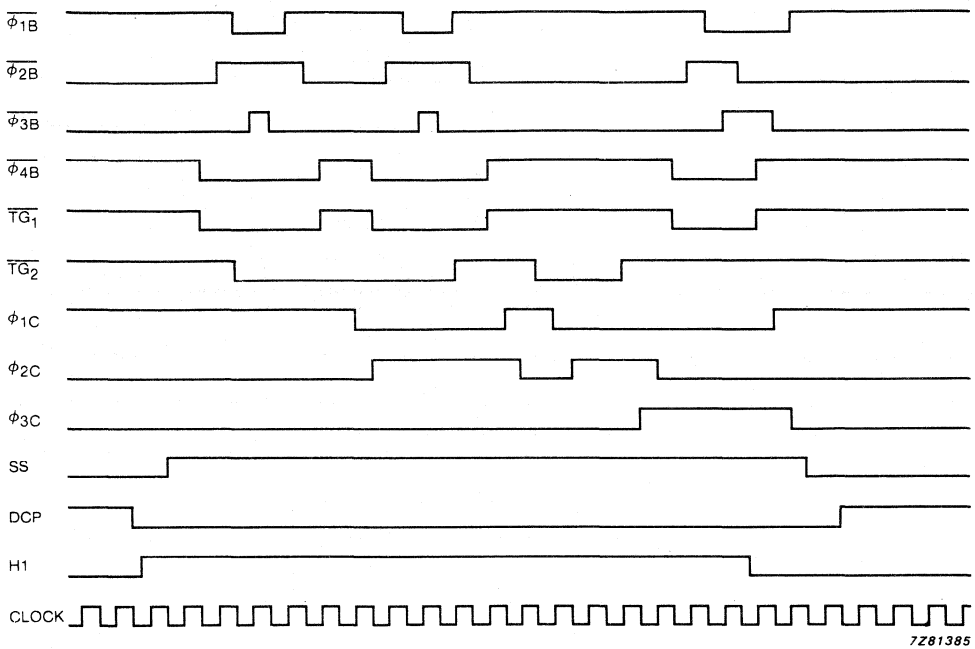
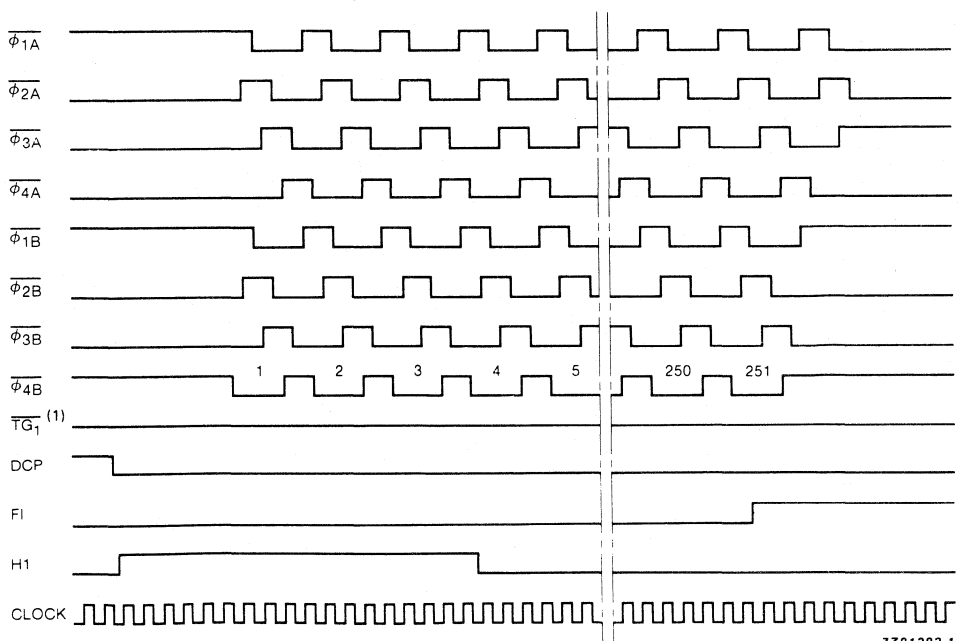
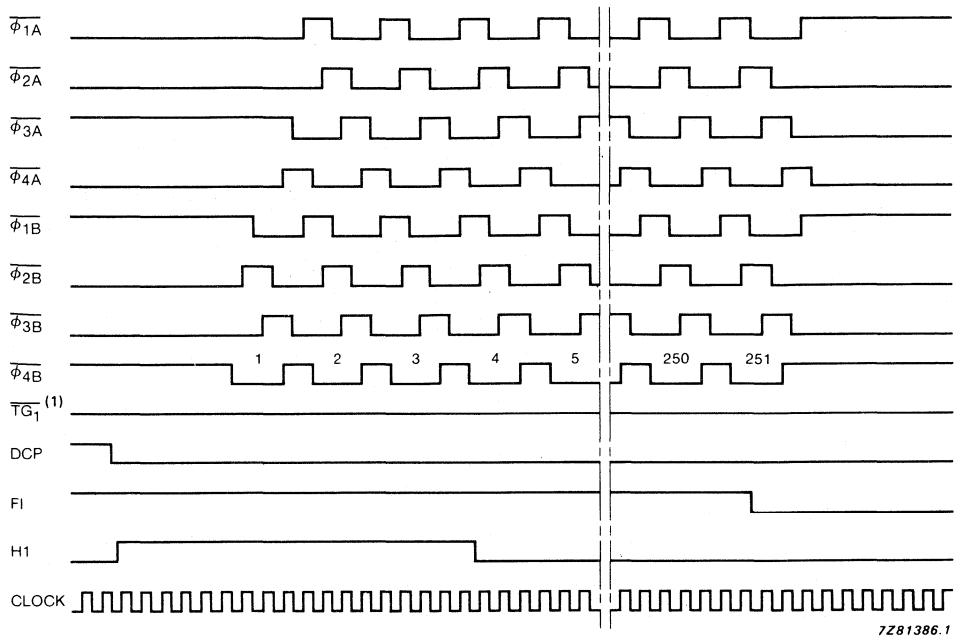


Fig.8 Line transport (525 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.9 Image sensor transport, field 2 (525 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.10 Image sensor transport, field 1 (525 lines).

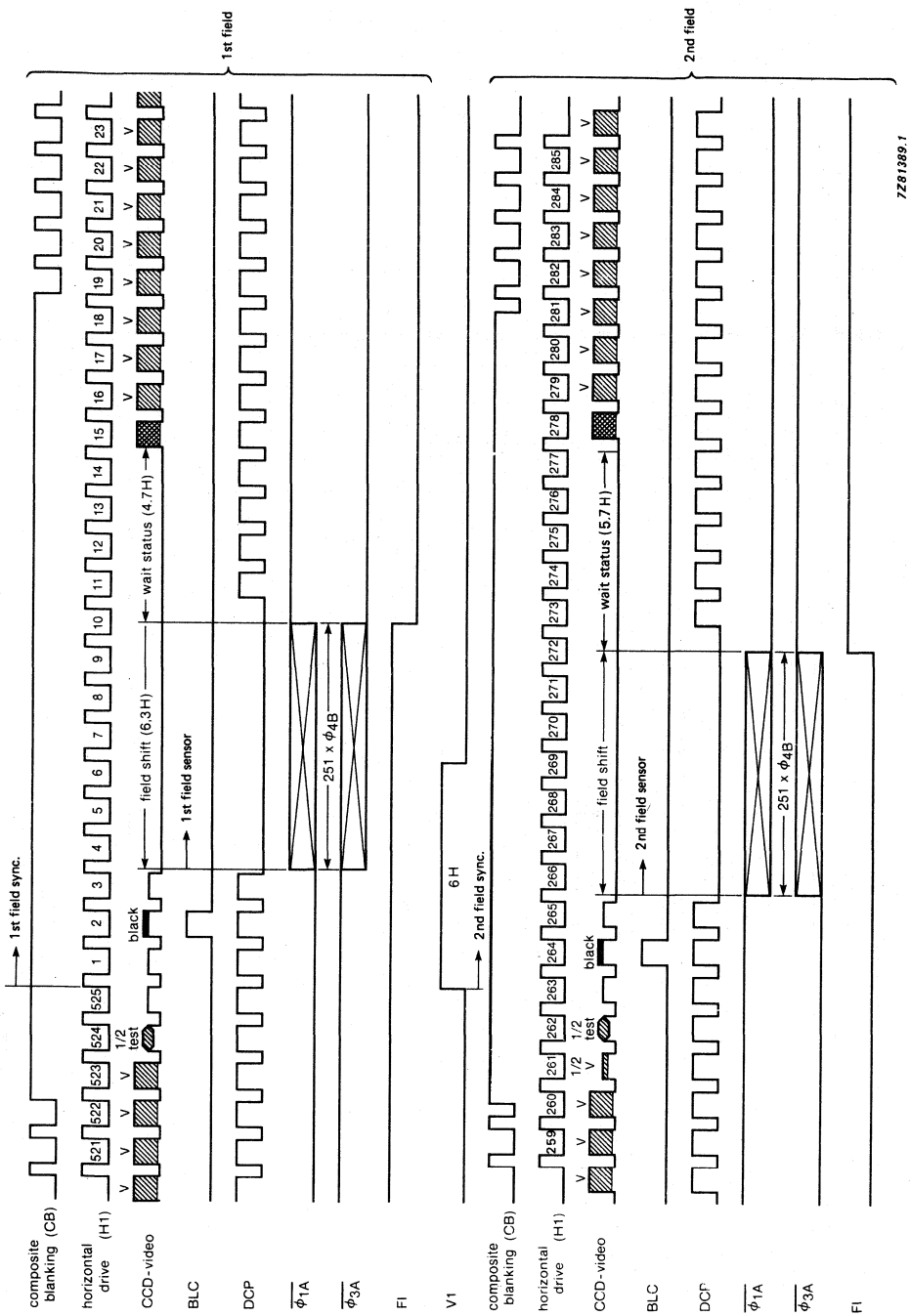


Fig.11 Pulse pattern during field blanking (525 lines

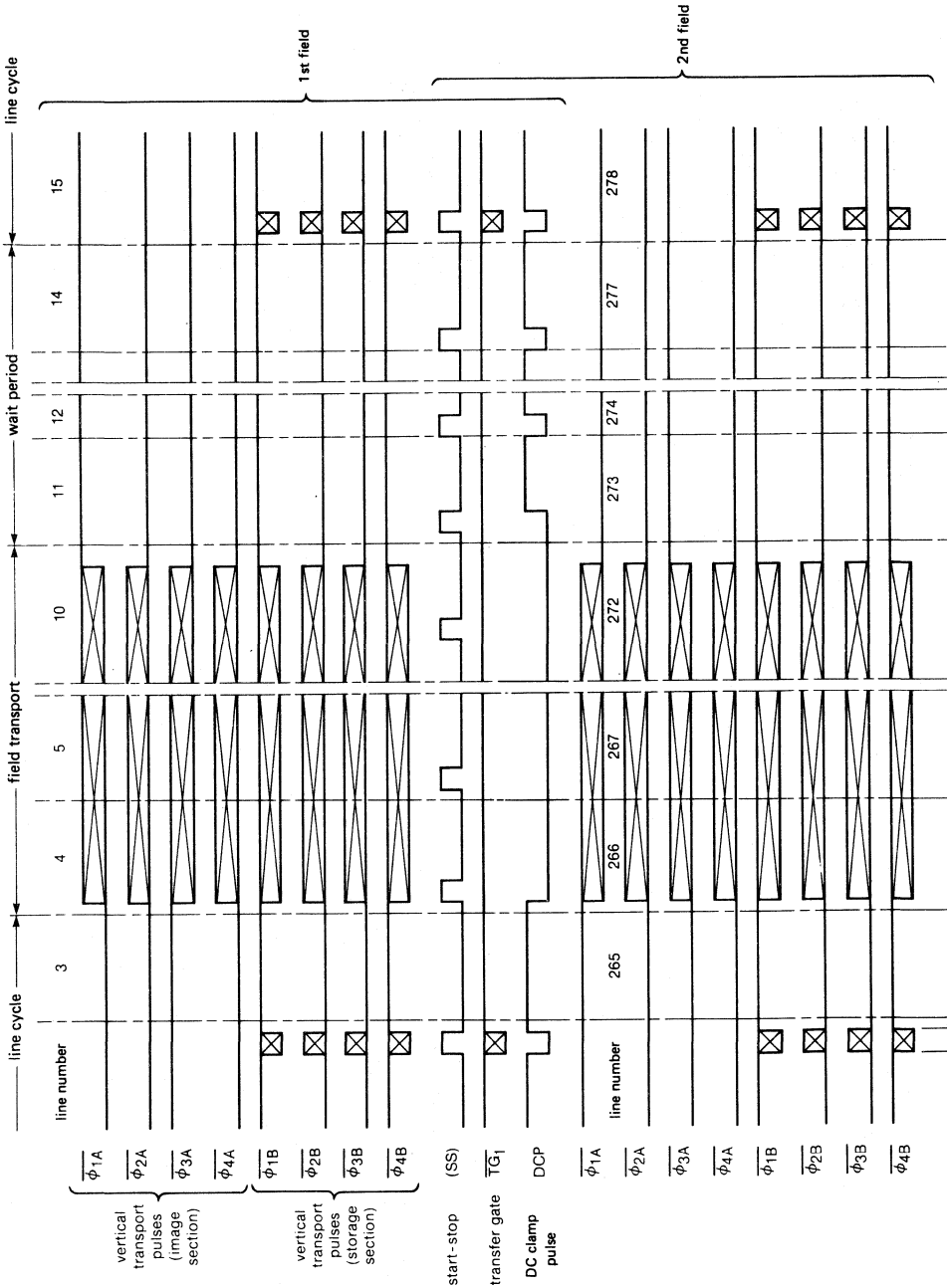


Fig.12 MNPPG cycles during field blanking (525 lines).

DATA LINE DECODER

GENERAL DESCRIPTION

The SAF1135 is a data line decoder, designed in CMOS technology, which operates in conjunction with the data line processor (SAA5235) to form a data line receiver system.

This system receives and decodes binary data that is transmitted in line 16 of every first field of a standard television signal. The decoded information is accessed via the built-in I²C bus interface. This information can be used to program a video tape recorder to start and stop the recording of a television program at the correct time, regardless of a delay or extension in the transmission time of the required television program.

Valid Video Programming System (VPS) data is transmitted in line 16 only. There is no VPS information in line 329.

The data transmission is biphase modulated and the bit transfer rate is 2,5 Mbit/s.

Features

- Field selection
- Line 16 decoding
- Start code check
- Biphase check
- Storage of data line information
- Generation of data reset pulse
- I²C bus transmitter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 14)	I_{DD}	–	1	–	mA
Bit transfer rate at input DLD (pin 8)	BR_{DLD}	–	2,5	–	Mbits/s
Clock frequency at input DLCL (pin 11)	f_{DLCL}	–	5	–	MHz
Storage temperature range	T_{stg}	−65	–	+150	°C
Operating ambient temperature range	T_{amb}	0	–	70	°C

PACKAGE OUTLINES

14-lead DIL; plastic (SOT27).

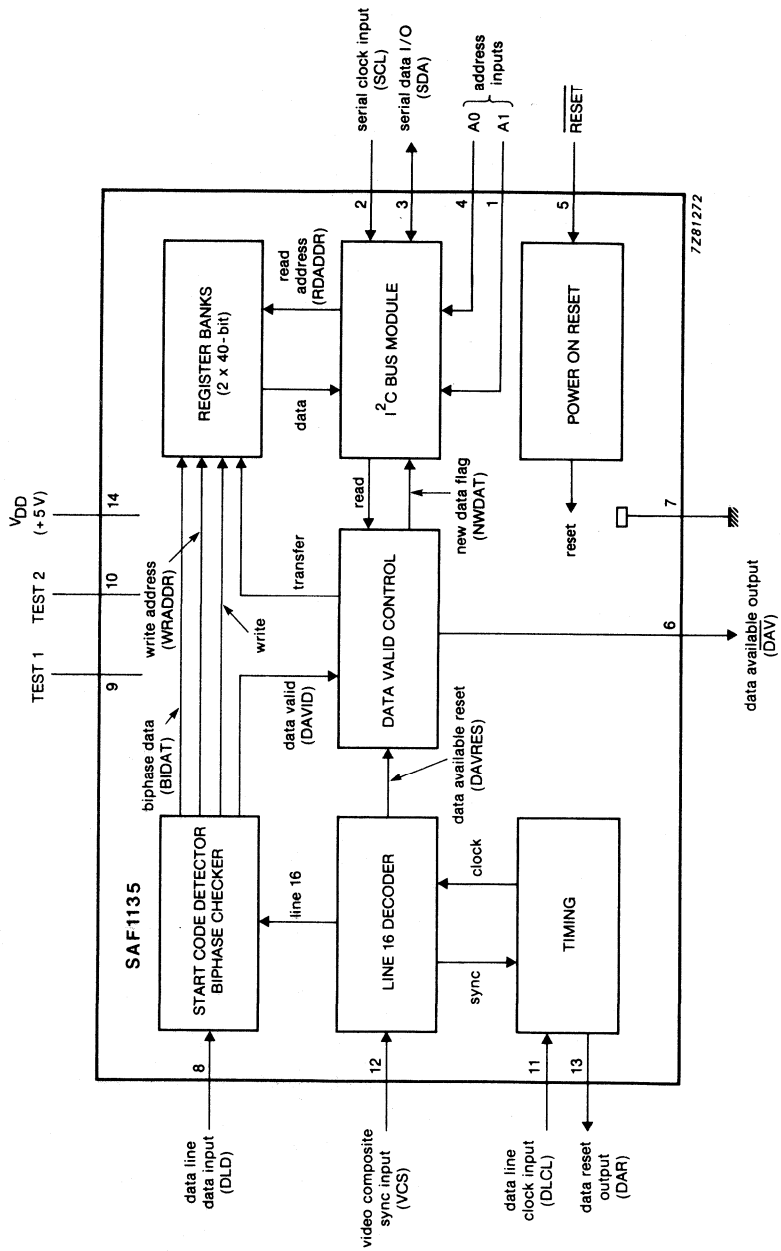


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The SAF1135 is designed to receive and decode Video Tape Recorder (VTR) control information which is transmitted in line 16 of every first field of a standard television signal. The following description refers to the block diagram Fig. 1 unless otherwise stated.

Data line 16

The total information of data line 16 consists of fifteen 8-bit words. The contents of the information is shown in Fig. 2, a timing diagram of the data line in Fig. 3 and a survey of VTR control labels in Fig. 4.

From the total fifteen 8-bit words, the SAF1135 extracts words 5, 11, 12, 13 and 14. The contents of these words can be requested via the built-in I^2C bus interface (see Fig. 9). The circuit is fully transparent, thus each bit is transferred without modification. Only the sequence of the words is changed; words 11 to 14 being transmitted first followed by word 5.

By evaluation of the Video Composite Sync (VCS) signal at pin 12 the SAF1135 identifies the beginning of line 16 in the first field. The line 16 decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection, see Fig. 5) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in register bank R (Receive). If no biphase error has occurred, the contents of register bank R are transferred to register bank T (Transmit) by the data valid control signal (DAVID). If the system has been addressed, this transfer is delayed until the next start or stop condition of the I^2C bus has been received.

The last correct data line information remains available until it is read via the I^2C bus. After it is read once the stored information is no longer considered to be valid, the internal new data flag (NWDAT) is reset and if the circuit is addressed, the only VPS data sent back is "FFF...F". The same conditions apply after power-up. Then no data can be read out.

New data is available after reception of another error-free line 16.

Power-on Reset

Reset pulses applied externally to pin 5 ($\overline{\text{RESET}}$; active LOW) are latched internally by the power-on reset circuit.

$\overline{\text{RESET}}$ = LOW influences:

- I^2C bus logic to no acknowledge
- NWDAT flag and internal timing to reset
- Data available output ($\overline{\text{DAV}}$; active LOW) at pin 6 forced to LOW
- Data reset output (DAR) at pin 13 forced to HIGH
- Serial data (SDA) input/output at pin 3 released

When $\overline{\text{RESET}}$ changes to HIGH the reset period is terminated with the next negative-going transition of the data line clock (DLCL) input at pin 11. Then, the data available ($\overline{\text{DAV}}$) output at pin 6 will go HIGH.

When an external reset is not used pin 5 is connected to V_{DD}. If an external reset is required, the rise time (t_r) of $\overline{\text{RESET}}$ voltage must be greater than 50 μs. An external 10 kΩ resistor connected between pin 5 and V_{DD} and an external 2,7 nF capacitor connected to V_{SS} will result in $t_r \geqslant 50$ μs.

FUNCTIONAL DESCRIPTION (continued)

Word	Content
1	Run in
2	Start code
3	Program source identification (binary coded)
4	Program source identification (ASCII sequential)
5	Sound and VTR control information
6	Program/Test picture identification
7	Internal information exchange
8	Address assignment of signal distribution
9	
10	Messages/Commands
11	VTR Control Information
12	
13	
14	
15	Reserve

Fig. 2 Total information of data line 16.

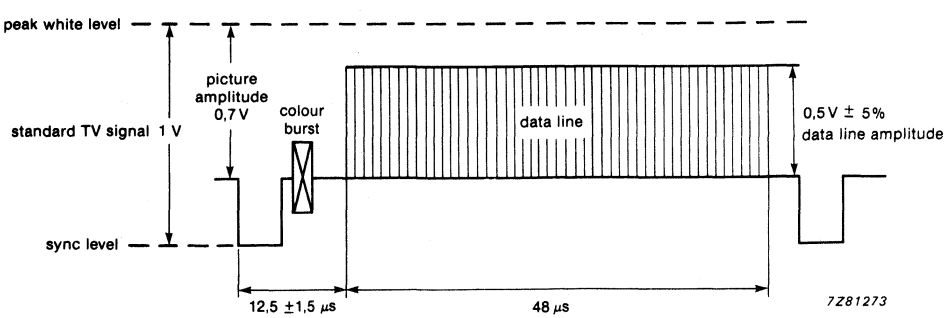


Fig. 3 Timing diagram of data line 16; modulation depth 71,4%.

	VTR Control Information																																						
Word-no.	5								11								12								13								14							
Bit-no.	1	2	3	4	5	6	7	8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Label binary	Bit 1	Bit 2	Status						Address range	Day							Month				Hour				Minute								Nation				Program Source			
	0	0	2-Channel							Special System Code																														
	0	1	Mono																																					
	1	0	Stereo																																					
	1	1	2-Channel																																					
System Status Code									1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	NC . . NC				PC . . . . PC			
	Bit 3	Bit 4																																						
Pause Code	1	0	not for children						1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	NC . . NC				PC . . . . PC			
Interrupt Code	0	1	free						1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	NC . . NC				PC . . . . PC			

Where:

X = 0 or 1 (bit)
NC is the Nation Code
PC is the Program Source Code

Fig. 4 VTR control information of data line 16.

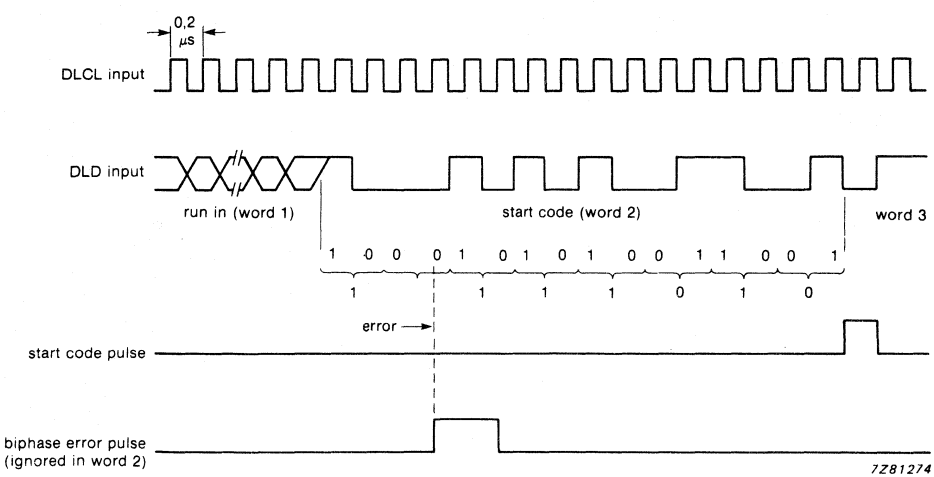


Fig. 5 Timing diagram of start code detection.

FUNCTIONAL DESCRIPTION (continued)

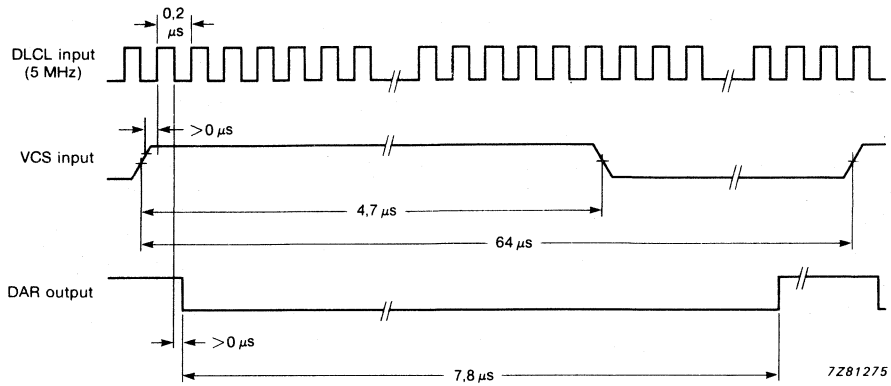


Fig. 6 Timing diagram of the data reset pulse generation.

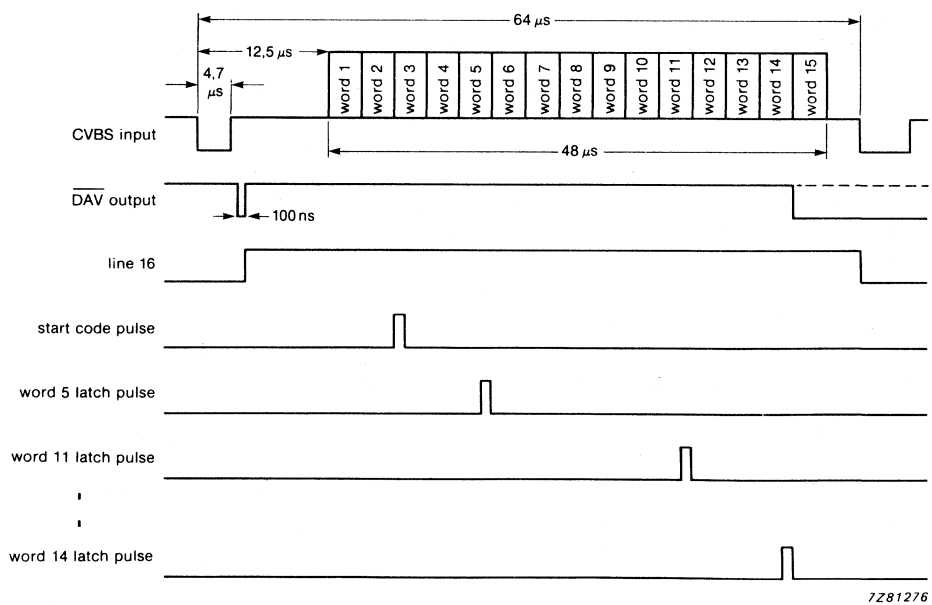


Fig. 7 Timing diagram of the data available output and word latch pulses.

Data line data and clock inputs (DLD; DLCL)

The data line data and clock signals from the SAA5235 are input at pins 8 and 11 respectively. The data transmission is biphase modulated, the bit transfer rate is 2,5 Mbit/s and the clock frequency is 5 MHz.

Input DLD incorporates an internal active clamping circuit. DLCL is internally a.c. coupled.

Video composite sync input (VCS)

The VCS input pulse at pin 12 is used for:

- Generation of the data reset pulse (DAR)
- Identification of the first field
- Selection of line 16

The timing of the data reset pulse generation is shown in Fig. 6.

I^2C bus address inputs (A0; A1)

The two I^2C address inputs at pins 4 and 1 respectively, provide the four different addresses 20H, 22H, 24H and 26H.

Data reset output (DAR)

The DAR output at pin 13 is a line frequency pulse with a 0,88 duty factor derived from the VCS pulse. The DAR pulse is fed to the SAA5235 to reset the data slicer circuit and the clock phase detector circuit.

Data available output ($\overline{DAV}$)

The $\overline{DAV}$ active LOW output at pin 6 is set to LOW after reception of one error-free data line 16. $\overline{DAV}$ returns to HIGH after at the beginning of the next first field.

If no valid data is available $\overline{DAV}$ remains HIGH. However, a short duration (100 ns) pulse inserted at the beginning of line 16 ensures that a HIGH-to-LOW transition occurs, which can be used for triggering.

The timing of $\overline{DAV}$ output and word latch pulses is shown in Fig. 7.

I^2C bus

The internally latched data from words 5 and 11 to 14 can be clocked out via the I^2C interface by a bus master. The lines are the serial clock input (SCL) at pin 2 and the serial data input/output (SDA) at pin 3.

The SAF1135 can operate only as a slave transmitter on the bus.
Data format is shown in Fig. 8.

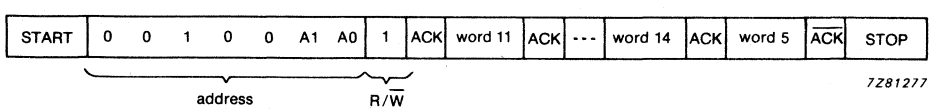


Fig. 8 I^2C bus data format.

- The MSB of each word is transmitted first.
- There is no restriction on the number of words to be transmitted, but if more than five words are requested, word 5 will be repeated.
- Noise pulses less than 200 ns duration are ignored on the bus lines.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 14)	V_{DD}		−0,5 to +7,0	V
Supply current (pin 14)	I_{DD}	max.	20	mA
Supply current (pin 7)	I_{SS}	max.	20	mA
Input voltage (pins 8 and 11)	V_I		−0,5 to +12	V
Input voltage on all other pins	V_I		−0,5 to V_{DD} +0,5*	V
Input current	$\pm I_I$	max.	10	mA
Output current	$\pm I_O$	max.	10	mA
Power dissipation per package**	P_{tot}	max.	400	mW
Power dissipation per output	P	max.	100	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* V_{DD} +0,5 not to exceed 7,0 V.

** Above +60 °C: derate linearly with 8 mW/K.

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 14)						
Supply voltage	–	V_{DD}	4,5	5	5,5	V
Supply current	Quiescent at 25 °C All inputs at V_{DD} or V_{SS} $\overline{RESET}$ at V_{SS} TEST 1 and TEST 2 at V_{DD} I_O = 0 mA	I_{DD}	–	–	10	μA
	During normal operation (without LED at $\overline{DAV}$, V_{DD} = 5 V)	I_{DD}	–	1	–	mA
Inputs						
A0, A1, TEST 1, TEST 2, SCL						
Input voltage LOW		V_{IL}	–	–	$0,2V_{DD}$	V
Input voltage HIGH		V_{IH}	$0,7V_{DD}$	–	–	V
Leakage current		I_{LI}	–	–	1	μA
DLCL						
Input voltage	Clock internally a.c. coupled	V_I	–	–	12	V
Leakage current	V_I = 0 to 10 V	I_{LI}	–	–	10	μA
$\overline{RESET}$	During normal operation pin 5 connected to V_{DD}					
Input voltage LOW		V_{IL}	–	–	$0,3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0,9V_{DD}$	–	–	V
Input current HIGH		I_{IH}	–	–	15	μA
Leakage current		I_{LI}	–	–	10	μA
VCS						
Input voltage LOW		V_{IL}	–	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	–	V
Leakage current		I_{LI}	–	–	1	μA

D.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs/Outputs						
DLD	Internal active clamping circuit, open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	2,0	–	12	V
Leakage current		I_{LI}	–	–	1	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
SDA	open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	3,15	–	–	V
Leakage current	V_{DD} = 6 V; V_I = 0 or V_{DD}	I_{LI}	–	–	6	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Outputs						
DAR						
Output voltage LOW	I_{OL} = 1 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V
$\overline{DAV}$						
Output voltage LOW	I_{OL} = 10 mA	V_{OL}	–	–	1,0	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs						
Input capacitance		C_I	–	–	10	pF
A0, A1, TEST 1, TEST 2, SCL						
Rise time	$V_{IL(max)}$ to $V_{IH(min)}$	t_r	50	–	–	µs
DLCL						
Clock frequency	sinusoidal input signal	f_{DLCL}	–	5	–	MHz
Input voltage	peak-to-peak value	$V_{I(p-p)}$	1	–	–	V
DLD						
Coupling capacitor		C_{EXT}	—	1	4,7	nF
Set-up time	relative to rising edge of DLCL	t_{SU}	40	–	–	ns
Hold-up time	relative to rising edge of DLCL	t_{HD}	40	–	–	ns
Outputs						
DAR, $\overline{DAV}$						
Rise and fall times	C_L = 50 pF	t_r, t_f	–	–	50	ns
DAR-time LOW		$t_{DAR,L}$	–	7,8	–	µs
SDA						
Fall time	C_L = 400 pF	t_f	–	–	300	ns
I²C bus - Input/Output						
Input current HIGH	For both SDA and SCL valid 0,9 V_{DD}, including I_{LI} of possible output stage	I_{IH}	–	–	10	µA
Input capacitance		C_I	–	–	10	pF
Rise time		t_r	–	–	1	µs
Fall time		t_f	–	–	0,3	µs
Clock frequency		f_{CL}	–	–	100	kHz
Pulse duration LOW		t_{LOW}	4,7	–	–	µs
Pulse duration HIGH		t_{HIGH}	4,0	–	–	µs

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

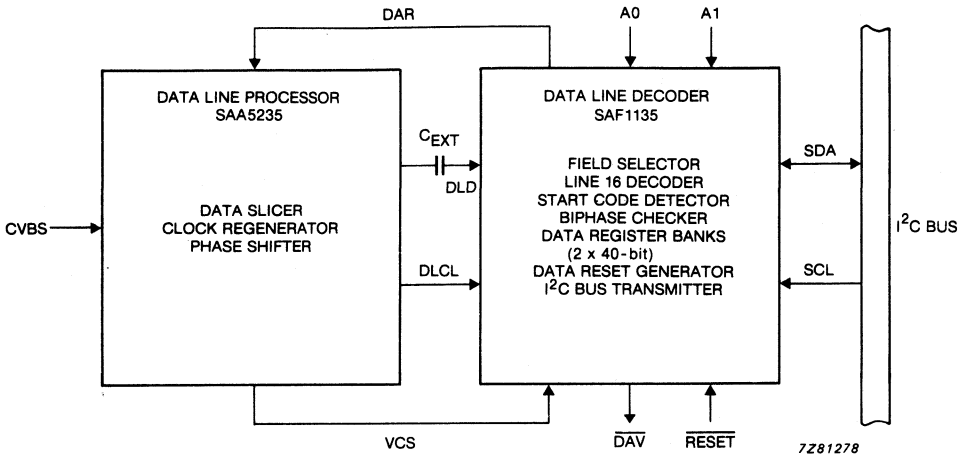


Fig. 9 Data line receiver.

SOUND I.F. AMPLIFIER/DEMODULATOR FOR TV

The TBA120U is an i.f. amplifier with a symmetrical FM demodulator and an a.f. amplifier with adjustable output voltage. The a.f. amplifier is also provided with an output for volume control and an input for VCR operation.

The input and output of the TBA120U are especially designed for LC-circuits, but the input can also be used with a ceramic filter.

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	12 V
Supply current	I_P	typ.	13,5 mA
I.F. voltage gain at f = 5,5 MHz	$G_{v\ if}$	typ.	68 dB
Input voltage starting limiting	V_i	typ.	30 μV
AM suppression at $\Delta f = \pm 50$ kHz	α	typ.	60 dB
A.F. output voltage adjustment range (pin 8)	$\Delta V_{o\ af}$	typ.	85 dB
A.F. output voltage at $\Delta f = \pm 50$ kHz (r.m.s. value)			
at pin 8	$V_{o\ af(rms)}$	typ.	1,2 V
at pin 12	$V_{o\ af(rms)}$	typ.	1,0 V

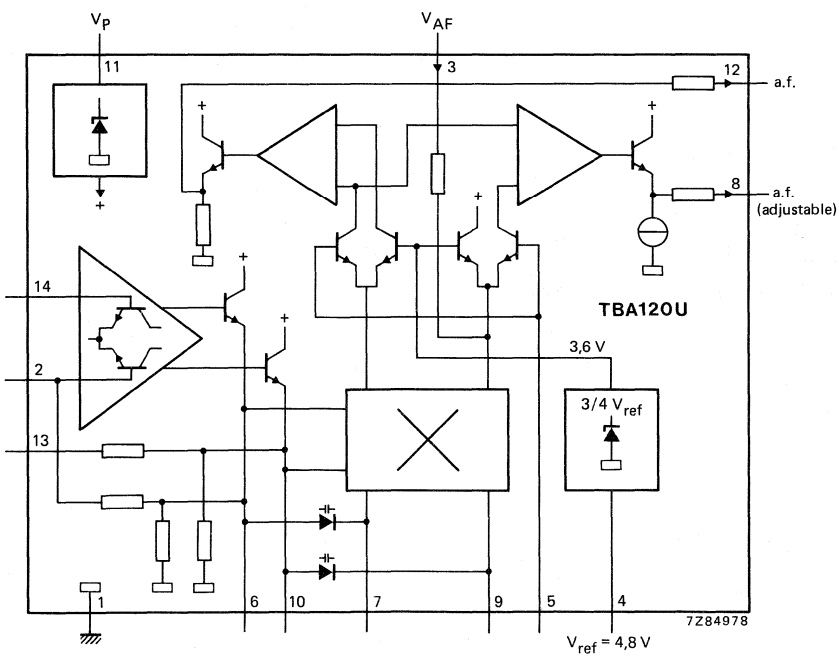


Fig. 1 Block diagram.

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-1}$	max.	18	V*
Adjustment voltage (pin 5)	V_{5-1}	max.	6	V
Total power dissipation	P_{tot}	max.	400	mW
By-pass resistance	R_{13-14}	max.	1	kΩ
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; f = 5,5 MHz

I.F. voltage gain	$G_{v\ if\ 6-14}$	typ.	68	dB
Input voltage starting limiting at Δf = ± 50 kHz; f_m = 1 kHz	V_i	typ. <	30 60	μV μV
I.F. output voltage at limiting (peak-to-peak value)	$V_{o\ if\ (p-p)}$	typ.	250	mV
AM suppression at Δf = ± 50 kHz; V_i = 500 μV; f_m = 1 kHz; m = 30%	α	> typ.	50 60	dB dB
I.F. residual voltage without de-emphasis at pin 12	$V_{if\ 12}$	typ.	30	mV
at pin 8	$V_{if\ 8}$	typ.	20	mV
A.F. voltage gain	$G_{v\ af\ 8-3}$	typ.	7,5	
A.F. adjustment at R_{4-5} = 5 kΩ; R_{5-1} = 13 kΩ	$\Delta V_{o\ af}$	 typ.	20 to 36 28	dB dB
A.F. output voltage control range	$\Delta V_{o\ af}$	> typ.	70 85	dB dB
Adjustment resistor**	R_{4-5}		1 to 10	kΩ
D.C. voltage portion at the a.f. outputs pin 12	V_{12-1}	typ.	5,6	V
pin 8	V_{8-1}	typ.	4,0	V
Output resistance of the a.f. outputs pin 12	$R_{o\ 12-1}$	typ.	1,1	kΩ
pin 8	$R_{o\ 8-1}$	typ.	1,1	kΩ
Input resistance of the a.f. input	$R_{i\ 3-1}$	typ.	2	kΩ
Stabilized reference voltage	$V_{4-1} = V_{ref}$	 typ.	4,2 to 5,3 4,8	V V
Source resistance of reference voltage source	R_{4-1}	typ.	12	Ω

* Supply voltage operating range is 10 to 18 V.

** Pin 5 must be connected to pin 4, when volume control adjustment is not applicable.

Hum suppression			
at pin 12	V_{12}/V_{11}	typ.	30 dB
at pin 8	V_8/V_{11}	typ.	35 dB
Supply current (pin 11)	$I_P = I_{11}$		9,5 to 17,5 mA
		typ.	13,5 mA
I.F. input impedance	$\|Z_i\|$	typ.	40 kΩ/4,5 pF
		>	15 kΩ/< 6 pF
A.F. output voltage at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 45$; r.m.s. value			
at pin 12	$V_{o\ af\ (rms)}$	typ.	1,0 V
at pin 8	$V_{o\ af\ (rms)}$	typ.	1,2 V
Distortion at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 20$	d_{tot}	typ.	1 %

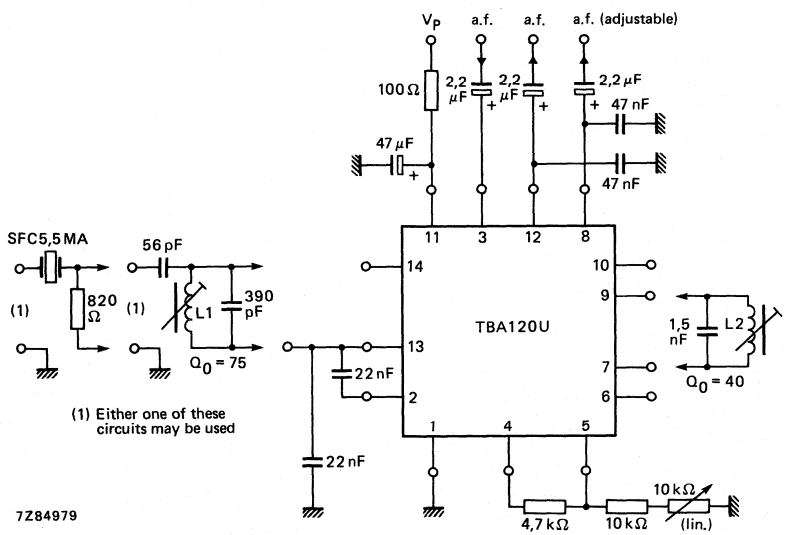


Fig. 2 Application example using TBA120U.

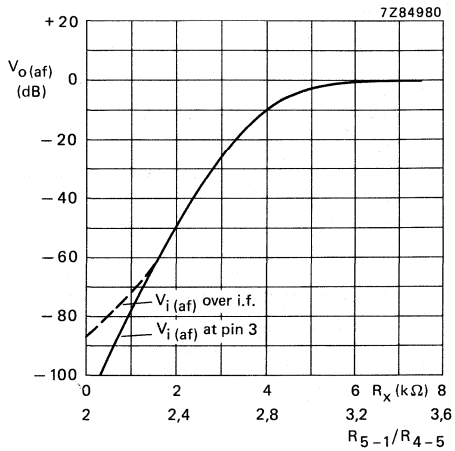


Fig. 3 The a.f. output voltage at pin 8 as a function of the resistance values as shown in Fig. 4.

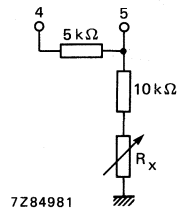
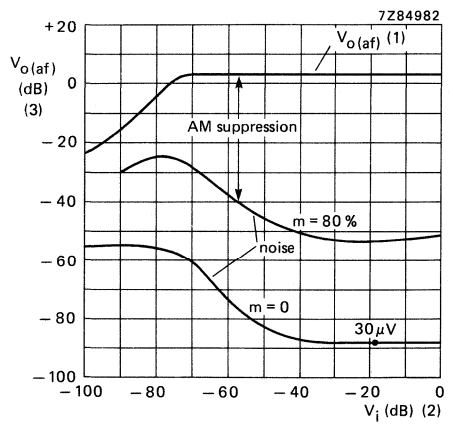


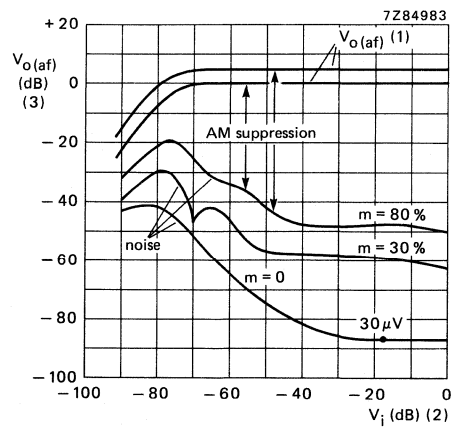
Fig. 4 Resistor conditions for curves in Fig. 3.



(1) $V_{o\,af}$ with de-emphasis at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $d_{tot} = 1{,}5\%$; 0 dB ≙ 770 mV.

(2) V_i: 0 dB ≙ 200 mV at 60 Ω.

Fig. 5 The a.f. output voltage at pin 8 as a function of the input voltage with SFC 5,5 MA at the input (see Fig. 2).



(1) $V_{o\,af}$ with de-emphasis at $f_m = 1$ kHz; 0 dB ≙ 770 mV;
curve a: $\Delta f = \pm 50$ kHz; $d_{tot} = 3\%$;
curve b: $\Delta f = \pm 25$ kHz; $d_{tot} = 1\%$.

(2) V_i: 0 dB ≙ 200 mV at pin 14.

Fig. 6 The a.f. output voltage at pin 8 as a function of the input voltage with broadband input (60 Ω).

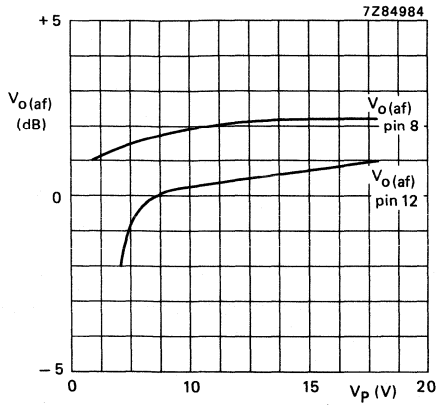


Fig. 7 The a.f. output voltages at pins 8 and 1 as a function of the supply voltage; 0 dB ≙ 770 mV.

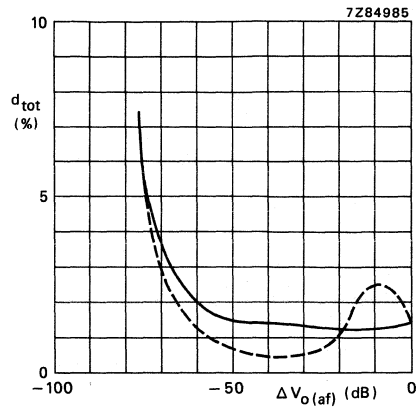


Fig. 8 Total distortion as a function of the a.f. output voltage change.
——— 0 dB ≙ 900 mV over i.f. (pin 8)
– – – – 0 dB ≙ 1,15 V (pin 8)

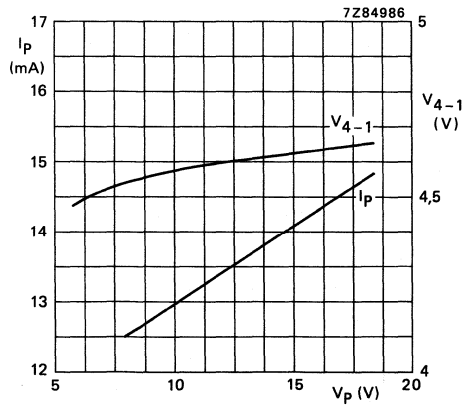


Fig. 9 Supply current and the reference voltage at pin 4 as a function of supply voltage.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

4 W AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

GENERAL DESCRIPTION

The TDA1013B is an integrated audio amplifier circuit with DC volume control, encapsulated in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit ideal for applications in mains and battery-fed apparatus such as television receivers and record players.

The DC volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control is by means of a DC voltage variable between 2 and 6.5 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop. This device requires only a few external components and offers stability and performance.

Features

- Few external components
- Wide supply voltage range
- Wide control range
- Pin compatible with TDA1013A
- Fixed gain
- High signal-to-noise ratio
- Thermal protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10	18	40	V
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	0.1	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
DC volume control unit						
Gain control range		$\lvert\Delta G_V\rvert$	80	–	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	45	55	mV
Input impedance (pin 8)		$\lvert Z_i\rvert$	23	29	35	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

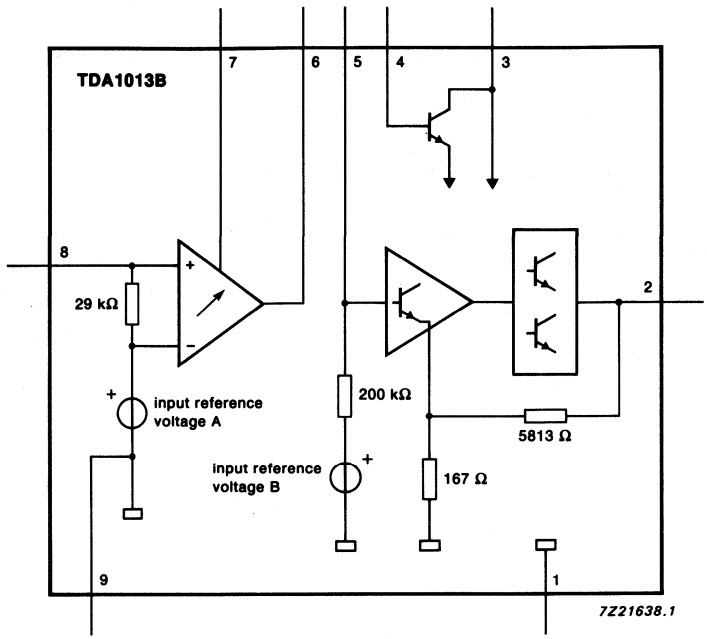


Fig.1 Block diagram.

PINNING

1 signal ground
2 amplifier output
3 supply voltage
4 electronic filter
5 amplifier input
6 control unit output
7 control voltage
8 control unit input
9 power ground

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 18	V
Peak output current	I_{OM}	max. 2,5	A
Output power at d_{tot} = 10%			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,3	%
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	> 100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

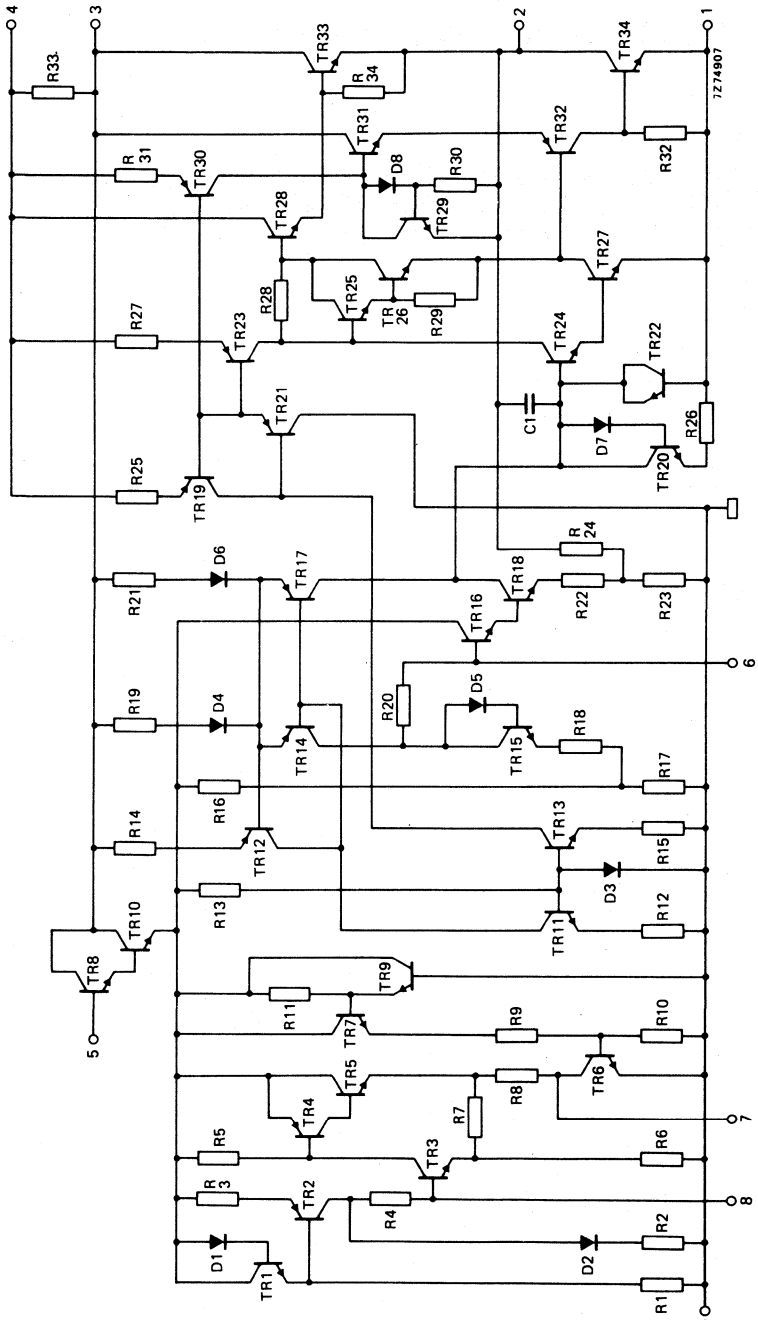


Fig. 1 Circuit diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	°C
Storage temperature range	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

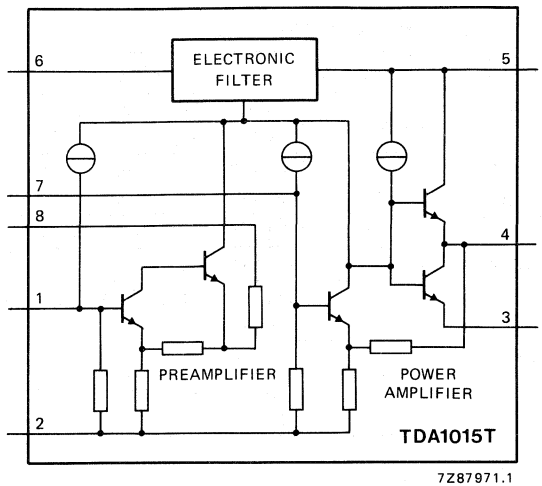


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12 V
Peak output current	I_{OM}	max.	1 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range			−55 to +150 °C
A.C. short-circuit duration of load during sine-wave drive at Vp = 9 V	t_{sc}	max.	1 hour

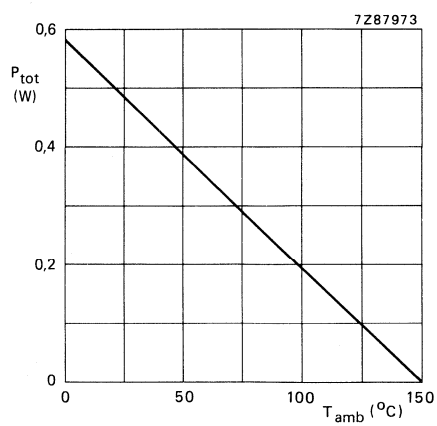


Fig. 2 Power derating curve.

Proportional-control triac triggering circuit

TDA1023/T

FEATURES

- Adjustable width of proportional range
- Adjustable hysteresis
- Adjustable width of trigger pulse
- Adjustable repetition timing of firing burst
- Control range translation facility
- Fail safe operation
- Supplied from the mains
- Provides supply for external temperature bridge

APPLICATIONS

- Panel heaters
- Temperature control

GENERAL DESCRIPTION

The TDA1023 is a bipolar integrated circuit for controlling triacs in a proportional time or burst firing mode. Permitting precise temperature control of heating equipment it is especially suited to the control of panel heaters. It generates positive-going trigger pulses but complies with regulations regarding mains waveform distortion and RF interference.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage (derived from mains voltage)	-	13.7	-	V
V_Z	stabilized supply voltage for temperature bridge	-	8	-	V
$I_{16(AV)}$	supply current (average value)	-	10	-	mA
t_w	trigger pulse width	-	200	-	µs
T_b	firing burst repetition time at C_T = 68 µF	-	41	-	s
$-I_{OH}$*	output current	-	-	150	mA
T_{amb}	operating ambient temperature range	−20	-	+75	°C

Note

*Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1023	16	DIL	plastic	SOT38
TDA1023T	16	mini-pack	plastic	SO16; SOT109A

Proportional-control triac triggering circuit

TDA1023/T

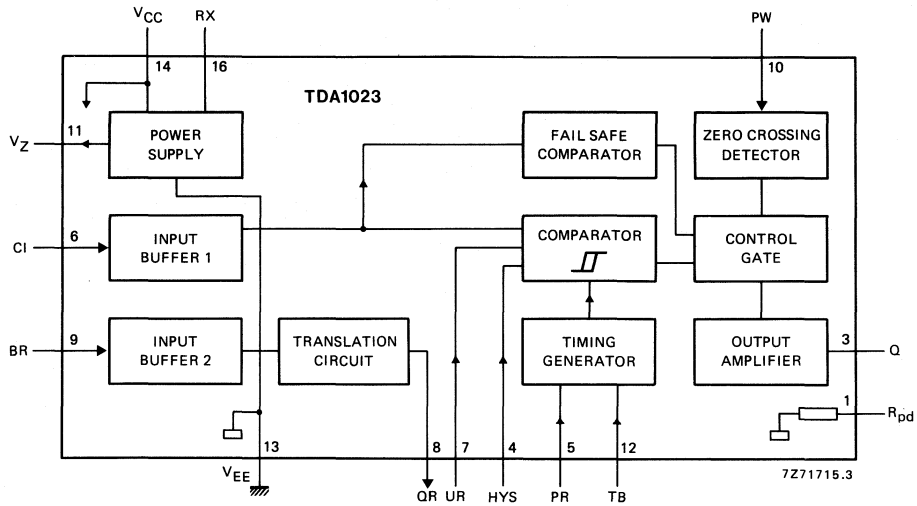


Fig.1 Block diagram.

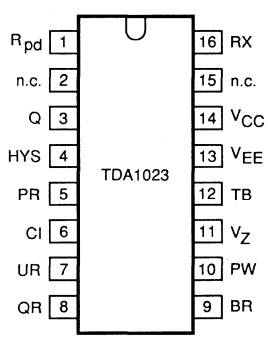


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
R_{pd}	1	internal pull-down resistor
n.c.	2	not connected
Q	3	output
HYS	4	hysteresis control input
PR	5	proportional range control input
CI	6	control input
UR	7	unbuffered reference input
QR	8	output of reference buffer
BR	9	buffered reference input
PW	10	pulse width control input
V_Z	11	reference supply output
TB	12	firing burst repetition time control input
V_{EE}	13	ground
V_{CC}	14	positive supply
n.c.	15	not connected
RX	16	external resistor connection

FUNCTIONAL DESCRIPTION

The TDA1023 generates pulses to trigger a triac. These pulses coincide with the zero excursions of the mains voltage, thus minimizing RF interference and mains supply transients. In order to gate the load on and off, the trigger pulses occur in bursts thus further reducing mains supply pollution. The average power in the load is varied by modifying the duration of the trigger pulse burst in accordance with the voltage difference between the control input CI and the reference input, either UR or BR.

Power supply: V_{CC}, RX and V_z (pins 14, 16 and 11)

The TDA1023 is supplied from the AC mains via a resistor R_D to the RX connection (pin 16); the V_{EE} connection (pin 13) is linked to the neutral line (see Fig.4a). A smoothing capacitor C_S should be coupled between the V_{CC} and V_{EE} connections.

A rectifier diode is included between the RX and V_{CC} connections whilst the DC supply voltage is limited by a chain of stabilizer diodes between the RX and V_{EE} connections (see Fig.3).

A stabilized reference voltage (V_Z) is available at pin 11 to power an external temperature sensing bridge.

Supply operation

During the positive mains half-cycles the current through the external voltage dropping resistor R_D charges the external smoothing capacitor C_S until RX attains the stabilizing potential of the internal stabilizing diodes. R_D should be selected to be capable of supplying the current I_{CC} for the TDA1023, the average output current $I_{3(AV)}$, recharge the smoothing capacitor C_S and provide the supply for an external temperature bridge. (see Figs 9 to 12). Any excess current is by-passed by the internal stabilizer diodes. The maximum rated supply current, however, must not be exceeded.

During the negative mains half-cycles external smoothing capacitor C_S supplies the sum of the current demand described above. Its capacitance must be sufficiently high to maintain the supply voltage above the specified minimum.

Dissipation in resistor R_D is halved by connecting a diode in series (see Fig.4b and 9 to 12). A further reduction in dissipation is possible by using a high quality dropping capacitor C_D in series with a resistor R_{SD} (see Figs 4c and 14). Protection of the TDA1023 and the triac against mains-borne transients can be provided by connecting a suitable VDR across the mains input.

Control and reference inputs CI, BR and UR (pins 6, 9 and 7)

For the control of room temperature (5 °C to 30 °C) optimum performance is obtained by using the translation circuit. The buffered reference input BR (pin 9) is used as a reference input whilst the output reference buffer QR (pin 8) is connected to the unbuffered reference input UR (pin 7). This ensures that the range of room temperature is encompassed in most of the rotation of the potentiometer to give a linear temperature scale with accurate setting.

Should the translation circuit not be required, the unbuffered reference input UR (pin 7) is used as a reference input. The buffered reference input BR (pin 9) must then be connected to the reference supply output V_Z (pin 11).

For proportional power control the unbuffered reference input UR (pin 7) must be connected to the firing burst repetition time control input TB (pin 12).The buffered reference input BR (pin 9), which is in this instance inactive, must then be connected to the reference supply output V_Z (pin 11).

Proportional range control input PR (pin 5)

The output duty factor changes from 0% to 100% by a variation of 80 mV at the control input CI (pin 6) with the proportional range control input PR open. For temperature control this corresponds to a temperature difference of 1 K.

By connecting the proportional range control input PR (pin 5) to ground the range may be increased to 400 mV, i.e. 5 K. Intermediate values may be obtained by connecting the PR input to ground via a resistor R5 (see Table 1).

Hysteresis control input HYS (pin 4)

With the hysteresis control input HYS (pin 4) open, the device has a built-in hysteresis of 20 mV. For temperature control this corresponds with 0.25 K.

Hysteresis is increased to 320 mV, corresponding to 4 K, by grounding HYS (pin 4). Intermediate values are obtained by connecting pin 4 via resistor R4 to ground. Table 1 provides a set of values for R4 and R5 giving a fixed ratio between hysteresis and proportional range.

Trigger pulse width control input PW (pin 10)

The width of the trigger pulse may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor

R_S between the trigger pulse width control input PW (pin 10) and the AC mains. The pulse width is inversely proportional to the input current (see Fig.13).

Output Q (pin 3)

Since the circuit has an open-emitter output it is capable of sourcing current. It is thus suited for generating positive-going trigger pulses. The output is current-limited and short-circuit protected. The maximum output current is 150 mA and the output pulses are stabilized at 10 V for output currents up to that value.

To minimize the total supply current and power dissipation, a gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figs 5 to 8).

Pull-down resistor R_{pd} (pin 1)

The TDA1023 includes a 1.75 kΩ pull-down resistor R_{pd} between pins 1 and 13 (V_{EE}, ground connection) intended for use with sensitive triacs.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	-	16	V
Supply current				
$I_{16(AV)}$	average	-	30	mA
$I_{16(RM)}$	repetitive peak	-	100	mA
$I_{16(SM)}$	non-repetitive peak (tp < 50 µs)	-	2	A
V_I	input voltage, all inputs	-	16	V
$I_{6,\ 7,\ 9,\ 10}$	input current	-	10	mA
V_1	voltage on R_{pd} connection	-	16	V
$V_{3,\ 8,\ 11}$	output voltage, Q, QR, V_Z	-	16	V
Output current				
$-I_{OH(AV)}$	average	-	30	mA
$-I_{OH(M)}$	peak max. 300 µs	-	700	mA
P_{tot}	total power dissipation	-	500	mW
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−20	+75	°C

CHARACTERISTICS

V_{CC} = 11 to 16 V; T_{amb} = −20 to +75 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	internally stabilized supply voltage at I_{16} = 10mA		12	13.7	15	V
$\Delta V_{CC}/\Delta I_{16}$	variation with I_{16}		-	30	-	mV/mA
I_{16}	supply current at V_{16-13} = 11 to 16 V I_{10} = 1mA; f = 50 Hz; pin 11 open; $V_{6-13} > V_{7-13}$	pins 4 and 5 open	-	-	6	mA
		pins 4 and 5 grounded	-	-	7.1	mA
Reference supply output V_Z (pin 11) for external temperature bridge						
V_{11-13}	output voltage		-	8	-	V
$-I_{11}$	output current		-	-	1	mA
Control and reference inputs CI, BR and UR (pins 6, 9 and 7)						
V_{6-13}	input voltage to inhibit the output		-	7.6	-	V
$I_{6, 7, 9}$	input current	V_1 = 4 V	-	-	2	µA
Hysteresis control input HYS (pin 4)						
ΔV_6	hysteresis	pin 4 open	9	20	40	mV
ΔV_6	hysteresis	pin 4 grounded	-	320	-	mV
Propcrtional control range input PR (pin 5)						
ΔV_6	proportional range	pin 5 open	50	80	130	mV
ΔV_6	proportional range	pin 5 grounded	-	400	-	mV
Pulse width control input PW (pin 10)						
t_w	pulse width	$I_{10(RMS)}$ = 1mA; f = 50 Hz	100	200	300	µs
Firing burst repetition time control input TB (pin 12)						
T_bC_T	firing burst repetition time, ratio to capacitor C_T		320	600	960	ms/µF
Output of reference buffer QR (pin 8)						
	output voltage at input voltage:					
V_{8-13}		V_{9-13} = 1.6 V	-	3.2	-	V
V_{8-13}		V_{9-13} = 4.8 V	-	4.8	-	V
V_{8-13}		V_{9-13} = 8 V	-	6.4	-	V
Output Q (pin 3)						
V_{OH}	output voltage HIGH	$-I_{OH}$ = 150 mA	10	-	-	V
$-I_{OH}$	output current HIGH		-	-	150	mA
Internal pull-down resistor R_{pd} (pin 1)						
R_{pd}	resistance to V_{EE}		1	1.75	3	kΩ

Table 1 Adjustment of proportional range and hysteresis. Combinations of resistor values giving hysteresis > $^1/_4$ proportional range.

Proportional range	Proportional range resistor	Minimum hysteresis	Maximum hysteresis resistor
	R5		R4
mV	kΩ	mV	kΩ
80	open	20	open
160	3.3	40	9.1
240	1.1	60	4.3
320	0.43	80	2.7
400	0	100	1.8

Table 2 Timing capacitor values C_T

Effective DC value	Marked AC specification		Catalogue number*
µF	µF	V	
68	47	25	2222 016 90129
47	33	40	- - 90131
33	22	25	- 015 90102
22	15	40	- - 90101
15	10	25	- - 90099
10	6.8	40	- - 90098

Note

*Special electrolytic capacitors recommended for use with the TDA1023.

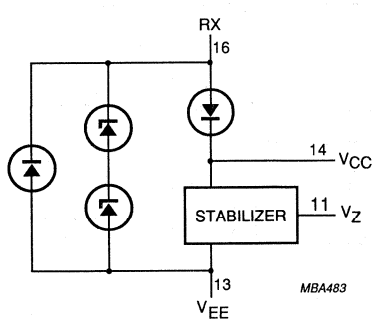


Fig.3 Internal supply connections.

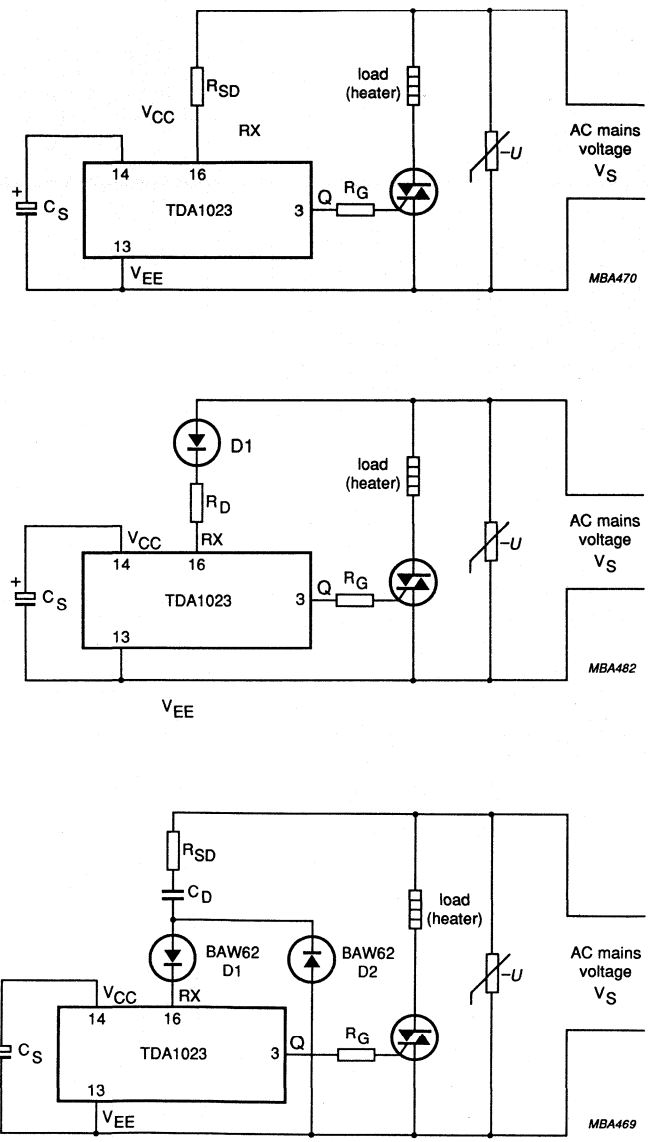


Fig.4 Alternative supply arrangements.

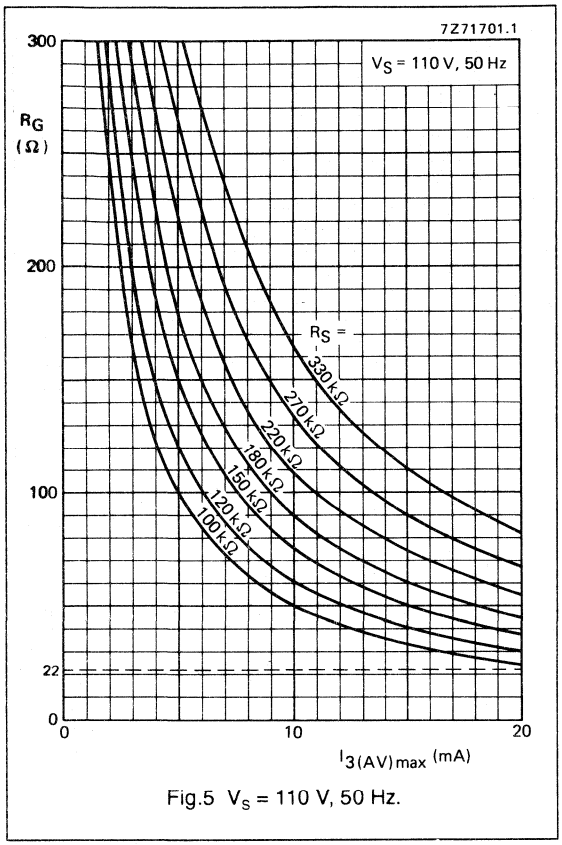


Fig.5 V_S = 110 V, 50 Hz.

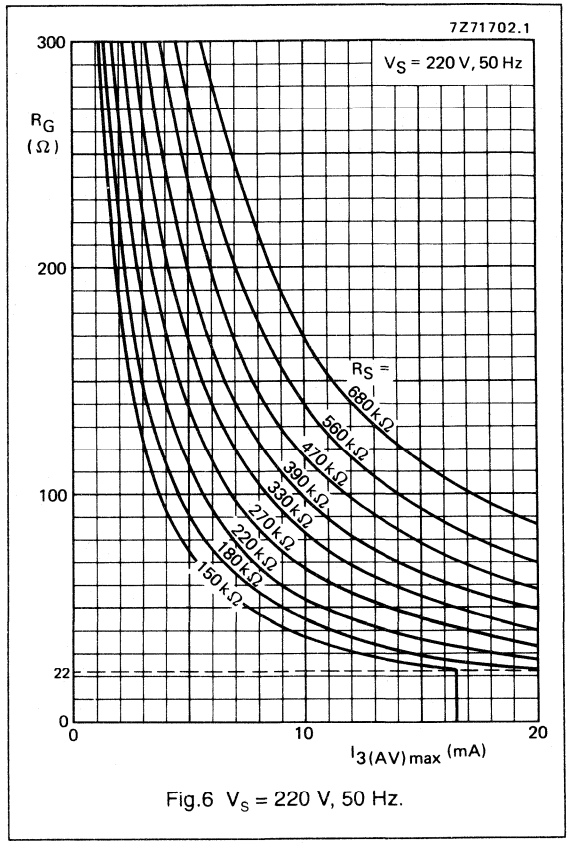


Fig.6 V_S = 220 V, 50 Hz.

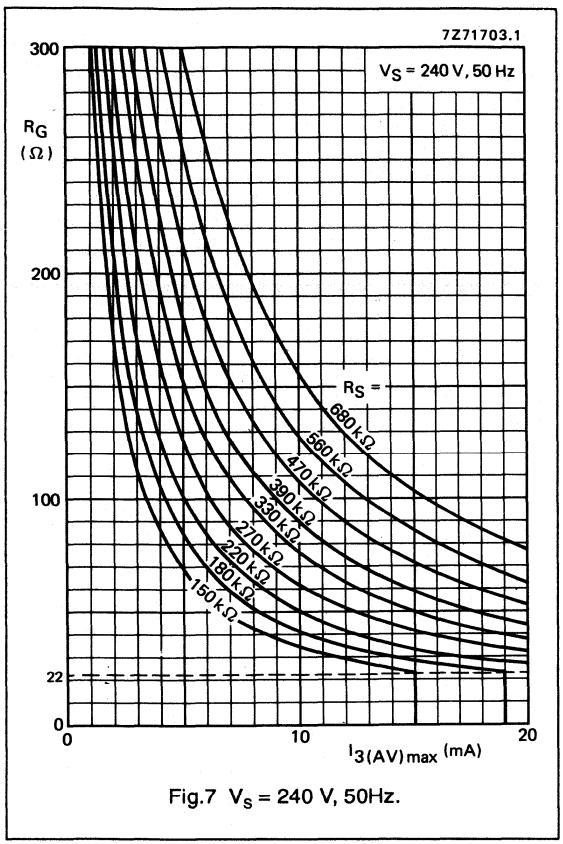


Fig.7 V_S = 240 V, 50Hz.

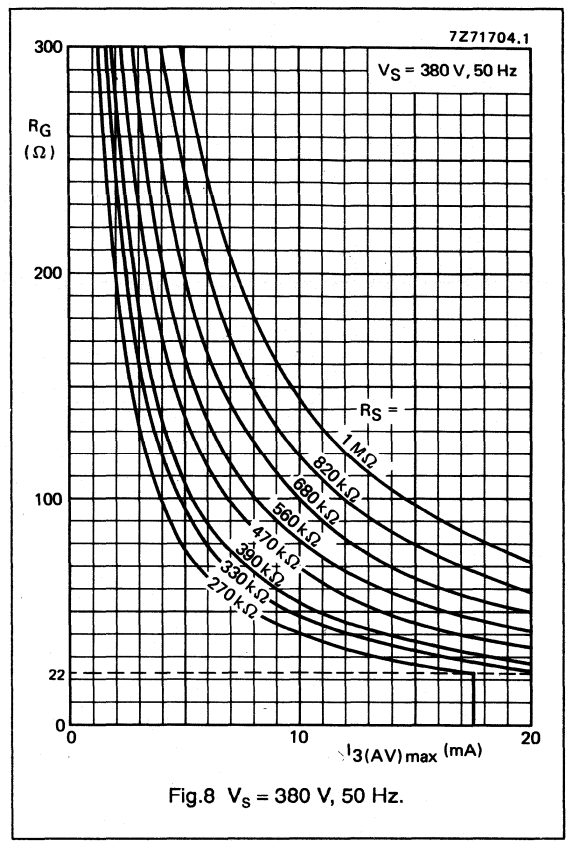


Fig.8 V_S = 380 V, 50 Hz.

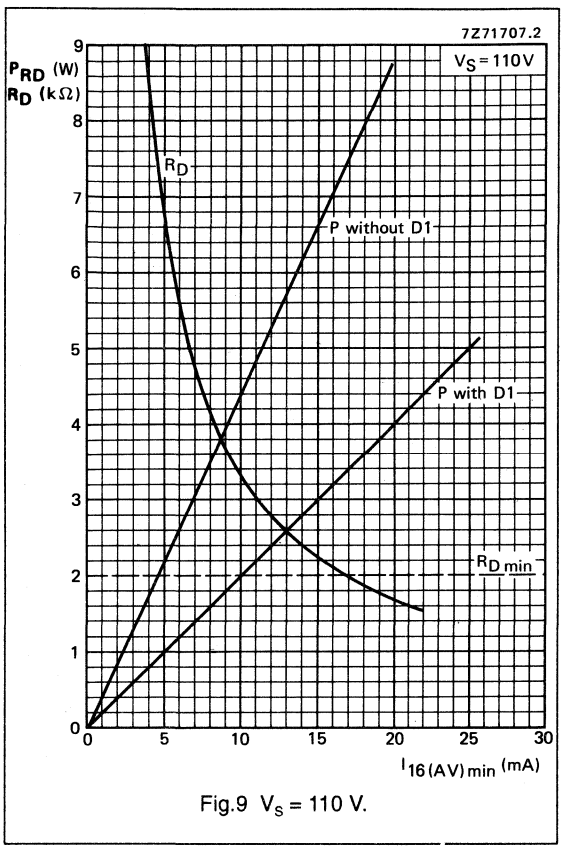


Fig.9 V_S = 110 V.

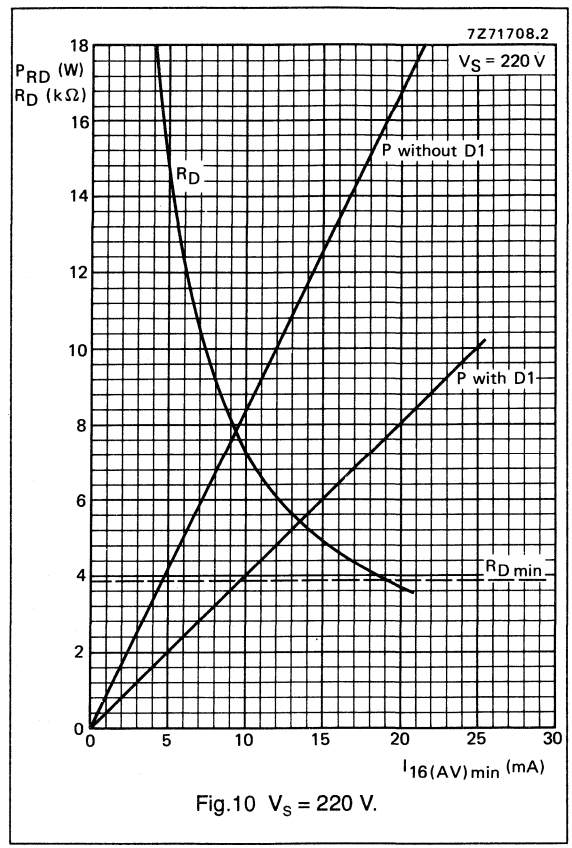


Fig.10 V_S = 220 V.

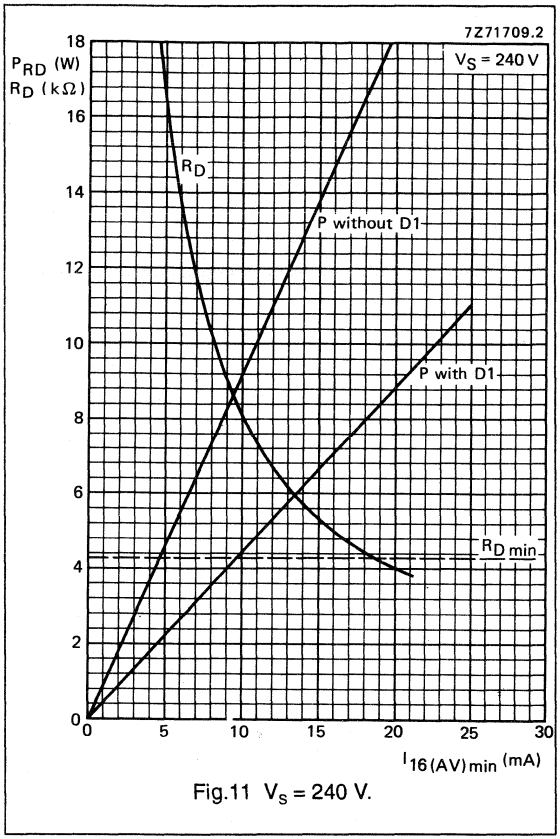


Fig.11 V_S = 240 V.

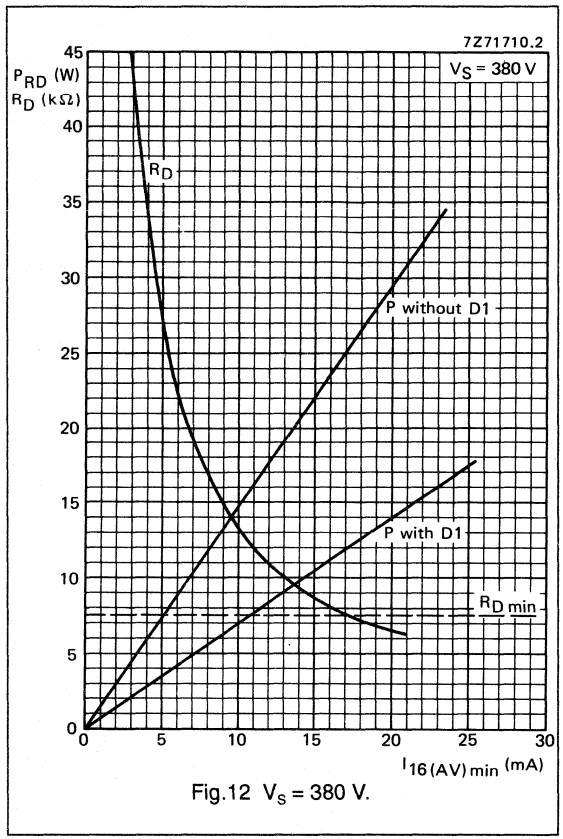
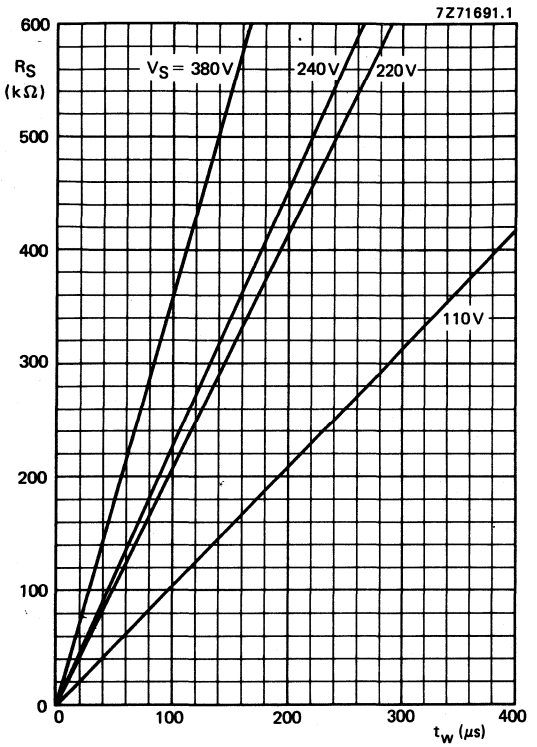


Fig.12 V_S = 380 V.



of required trigger pulse width t_w with a mains voltage V_S as a parameter.

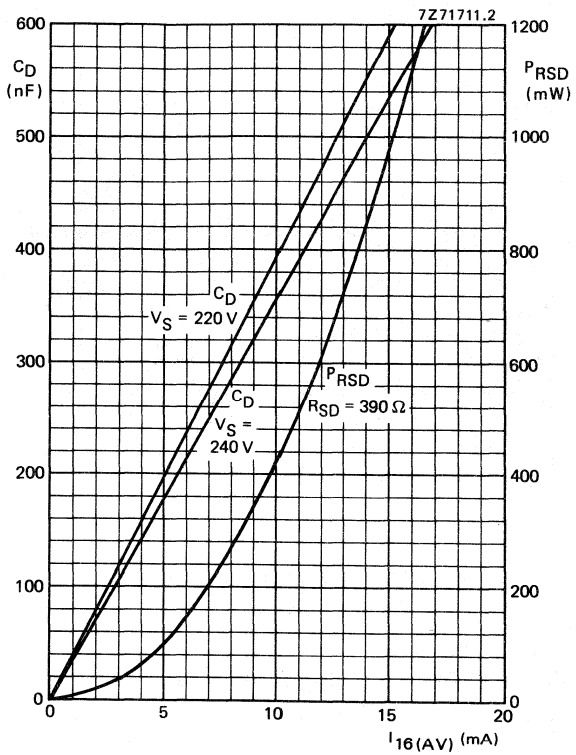
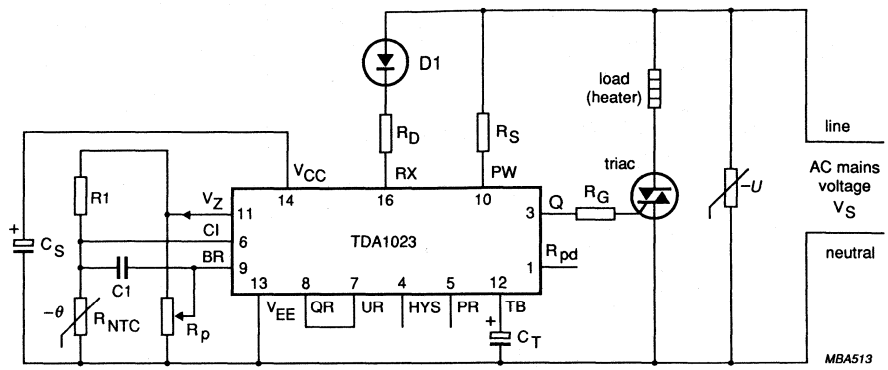


Fig.14 Nominal value of voltage dropping capacitor C_D and power P_{RSD} dissipated in a voltage dropping resistor R_{SD} as a function of average supply current $I_{16\ (AV)}$ with the mains supply voltage V_S as a parameter.



Conditions:- Mains supply; V_S = 220 V; Temperature range = 5 to 30 °C.
BT139 data at T_j = 25 °C; V_{gt} < 1.5 V; I_{gt} > 70 mA; I_L < 60 mA

Fig.15 The TDA1023/T used in a 1200 to 2000 W heater with triac BT139. For component values see Table 3.

Table 3 Temperature controller component values (see Fig. 15).

SYMBOL	PARAMETER	REMARKS	VALUE
t_w	trigger pulse width	see BT139 data sheet	75 µs
R_S	synchronization resistor	see Fig. 13	180 kΩ
R_G	gate resistor	see Fig. 6	110 Ω
$I_{3(AV)}$	max. average gate current	see Fig.8	4.1 mA
R4	hysteresis resistor	see Table 1	n.c.
R5	proportional band resistor	see Table 1	n.c.
$I_{16(AV)}$	min. required supply current		11.1 mA
R_D	mains dropping resistor	see Fig. 10	6.2 kΩ
P_{RD}	power dissipated in R_D	see Fig.10	4.6 W
C_T	timing capacitor (eff. value)	see Table 2	68 µF
VDR	voltage dependent resistor	cat. no. 2322 593 62512	250 V AC
D1	rectifier diode		BYW56
R1	resistor to pin 11	1% tolerance	18.7 kΩ
R_{NTC}	NTC thermistor (at 25 °C)	B = 4200 K cat no. 2322 642 12223	22 kΩ
R_p	potentiometer		22 kΩ
C1	capacitor between pins 6 and 9		47 nF
C_S	smoothing capacitor		220 µF; 16 V
If R_D and D1 are replaced by C_D and R_{SD}			
C_D	mains dropping capacitor		470 nF
R_{SD}	series dropping resistor		390 Ω
P_{RSD}	power dissipated in R_{SD}	see Fig.14	0.6 W
VDR	voltage dependent resistor	cat. no. 2322 594 62512	250 V AC

Notes

1. ON/OFF control: pin 12 connected to pin 13.
2. If translation circuit is not required: slider of R_p to pin 7; pin 8 open; pin 9 connected to pin 11.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23 V
Operating ambient temperature	T_{amb}		−30 to + 80 °C
Supply voltage (pin 14)	V_P	typ.	20 V
Current consumption	I_{14}	typ.	3,5 mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6 V
Voltage gain	G_v	typ.	1
Total harmonic distortion	d_{tot}	typ.	0,01 %
Crosstalk	α	typ.	70 dB
Signal-to-noise ratio	S/N	typ.	120 dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

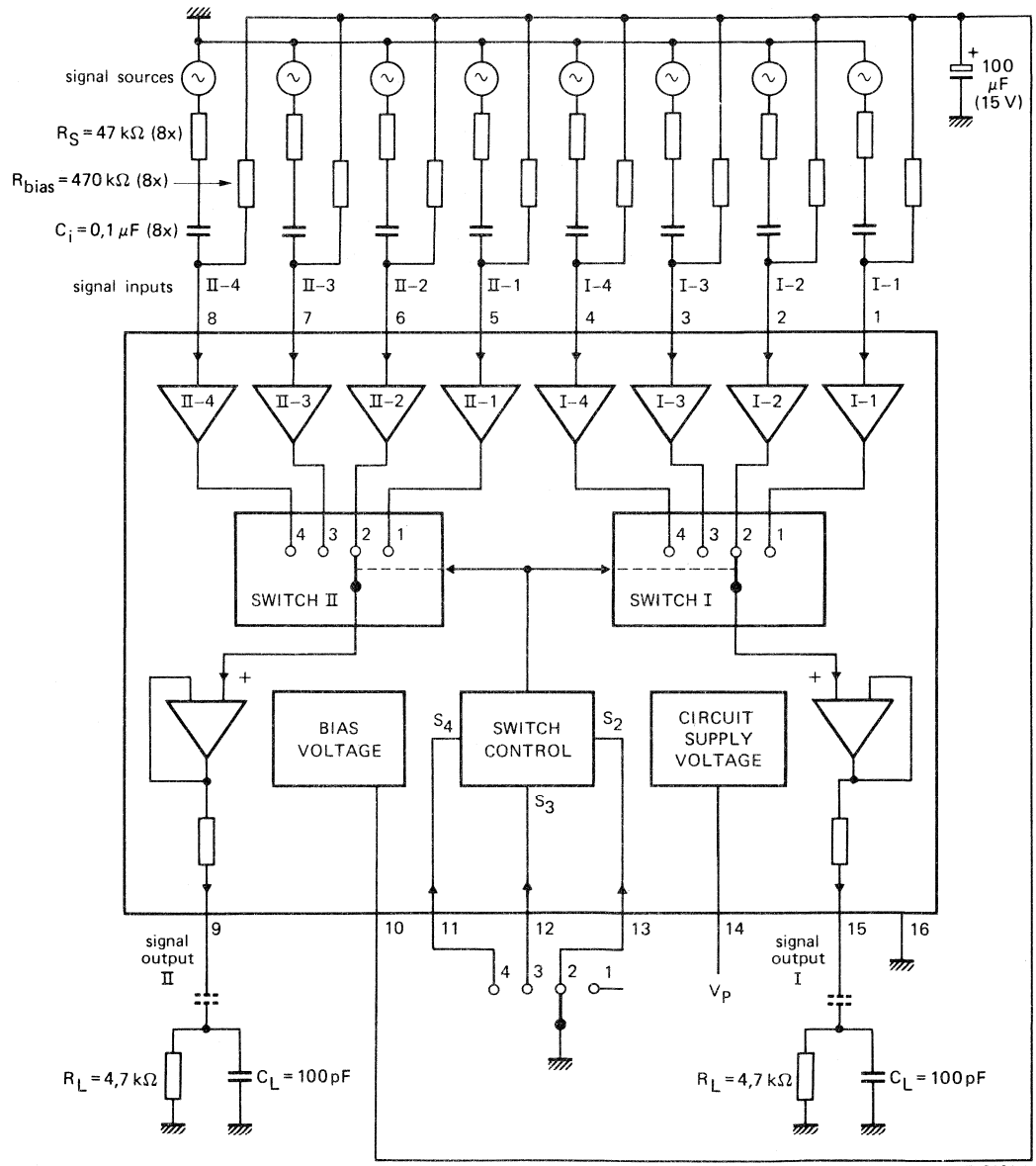


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption				
without load; $I_9 = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V
Signal inputs				
Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage R_S = 0; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at R_S = 1 kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_g = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1	
Current gain of a switched-on amplifier	G_i	typ.	10^5	

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400	Ω
Output current capability at V_P = 6 to 23 V	$\pm I_g$; $\pm I_{15}$	typ.	5	mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3	MHz
Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2	V/μs

Bias voltage

D.C. output voltage	$V_{10\text{-}16}$	typ. 10,2 to 11,8	11	V * V
Output resistance	$R_{10\text{-}16}$	typ.	8,2	kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage				
HIGH	V_{SH}	>	3,3	V **
LOW	V_{SL}	<	2,1	V
Input current				
HIGH (leakage current)	I_{SH}	<	1	μA
LOW (control current)	$-I_{SL}$	<	250	μA

* $V_{10\text{-}16}$ is typically $0{,}5 \cdot V_{14\text{-}16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5	dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 100	mV mV
Total harmonic distortion				
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01	%
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02	%
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03	%
Output signal handling				
d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 5,3	V V
Noise output voltage (unweighted)				
f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5	μV
Noise output voltage (weighted)				
f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12	μV
Amplitude response				
V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1	dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75	dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90	dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

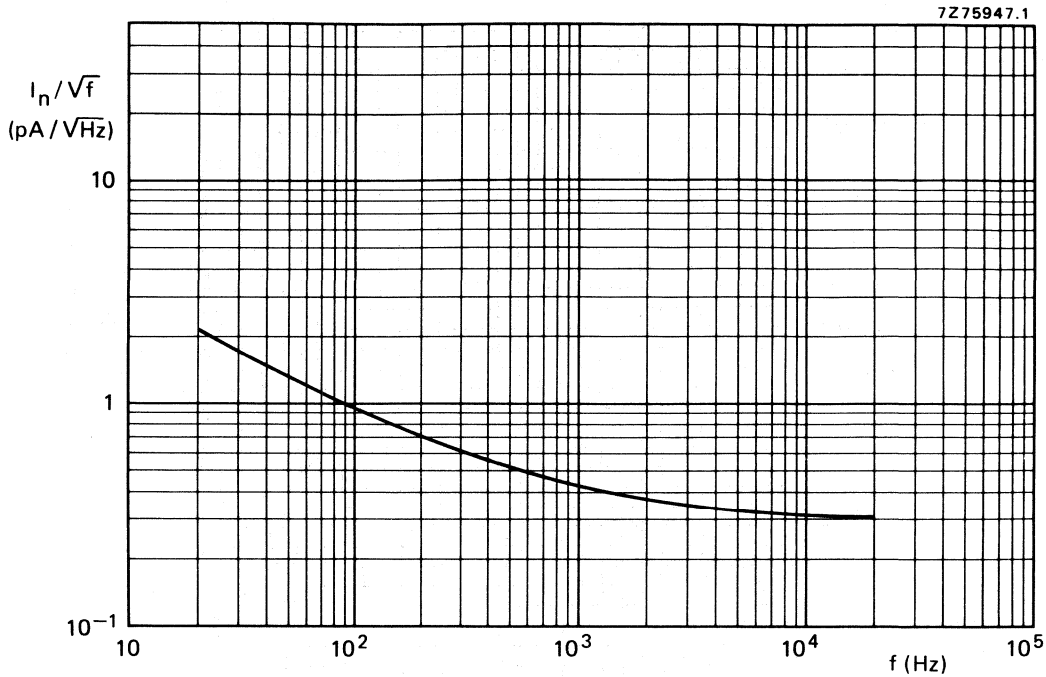


Fig. 2 Equivalent input noise current.

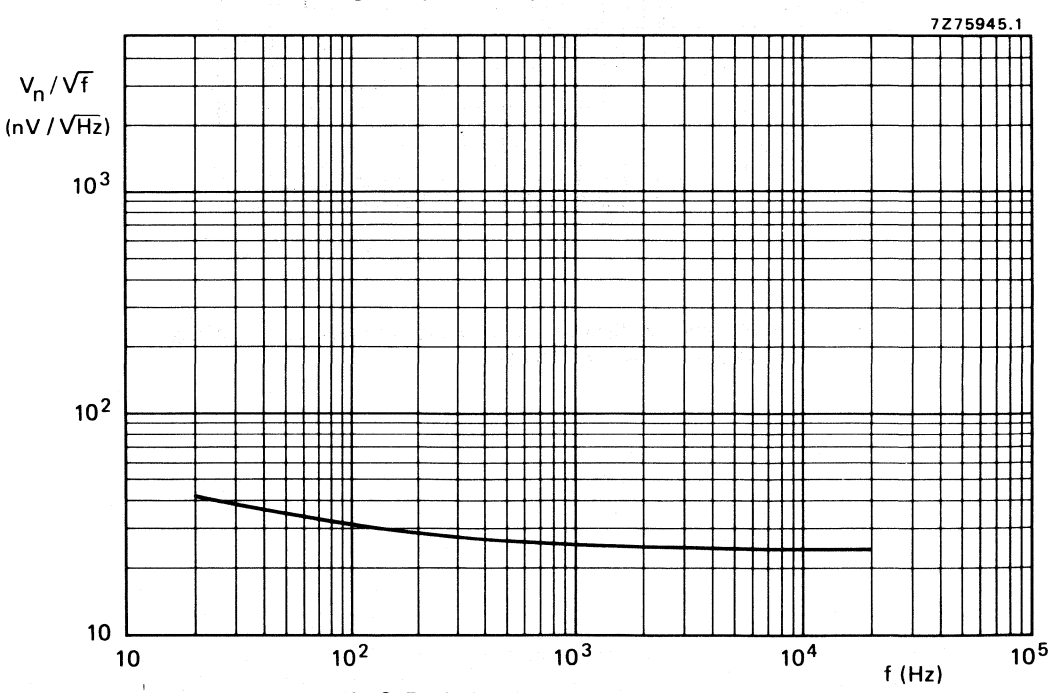


Fig. 3 Equivalent input noise voltage.

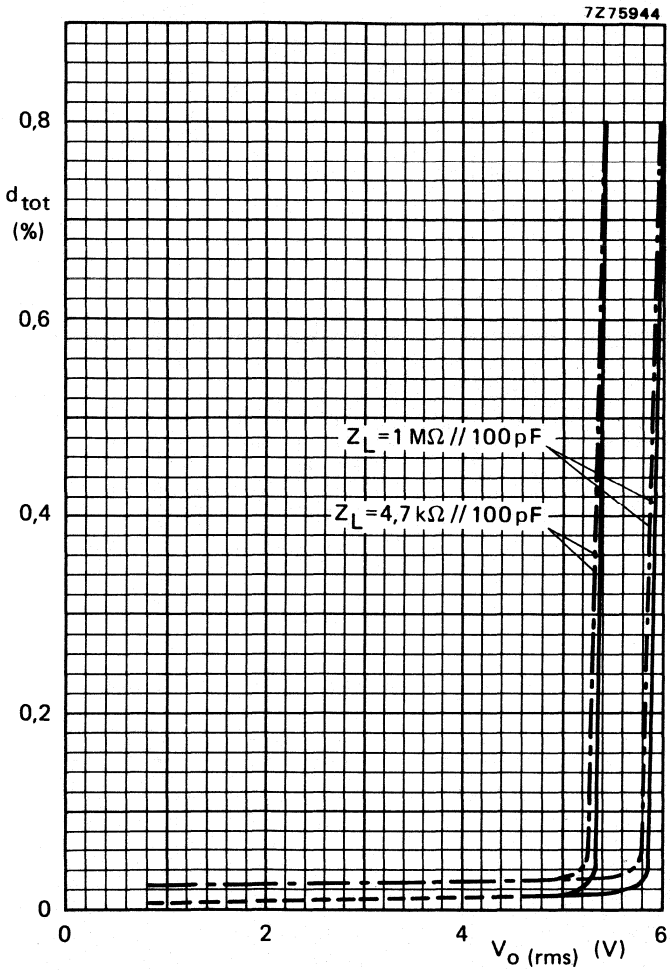


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — · — · f = 20 kHz.

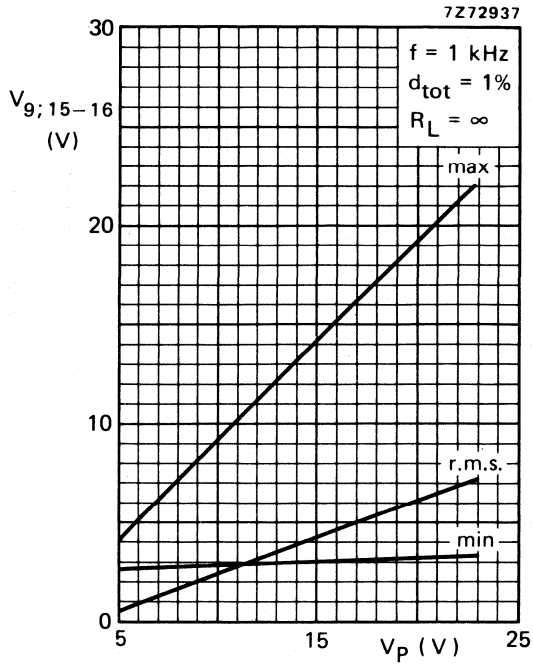


Fig. 5 Output voltage as a function of supply voltage.

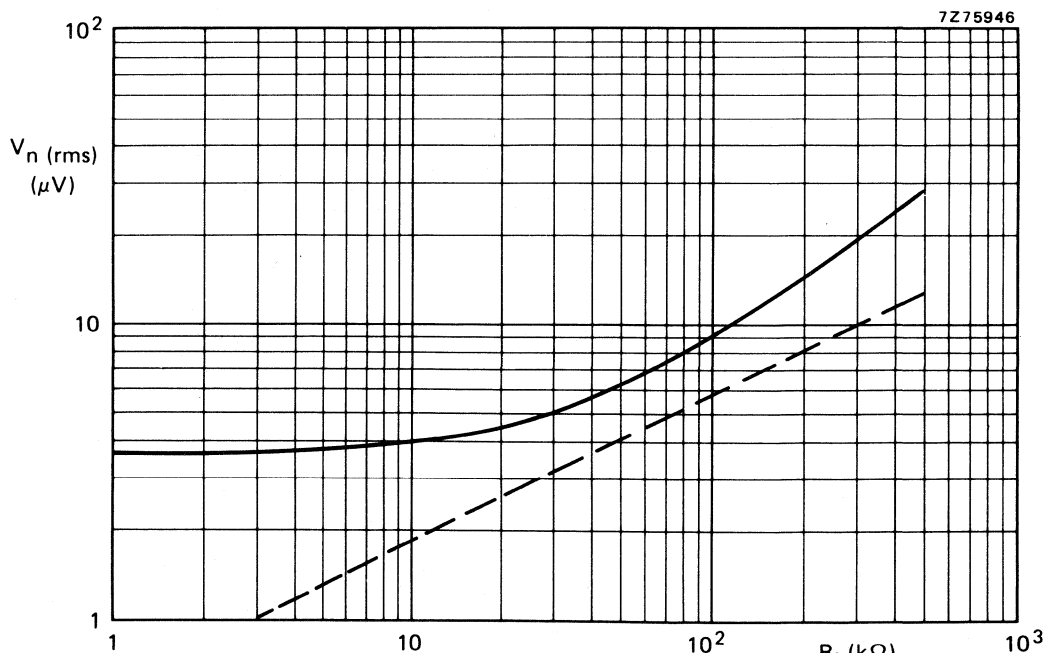


Fig. 6 Noise output voltage as a function of input resistance; G_V = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

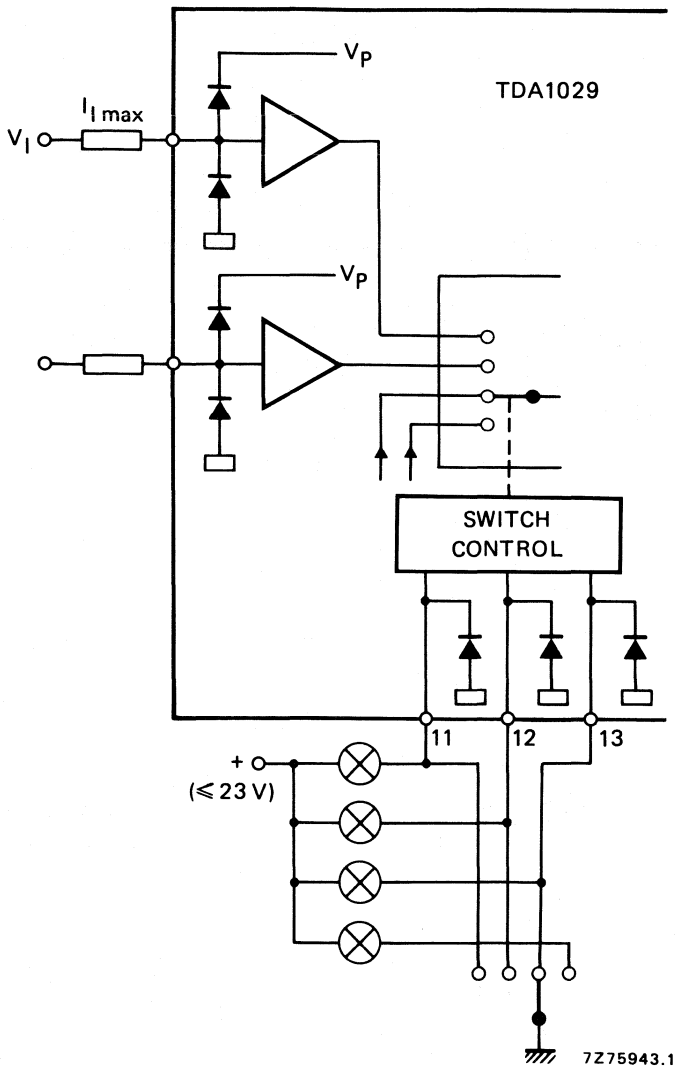


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

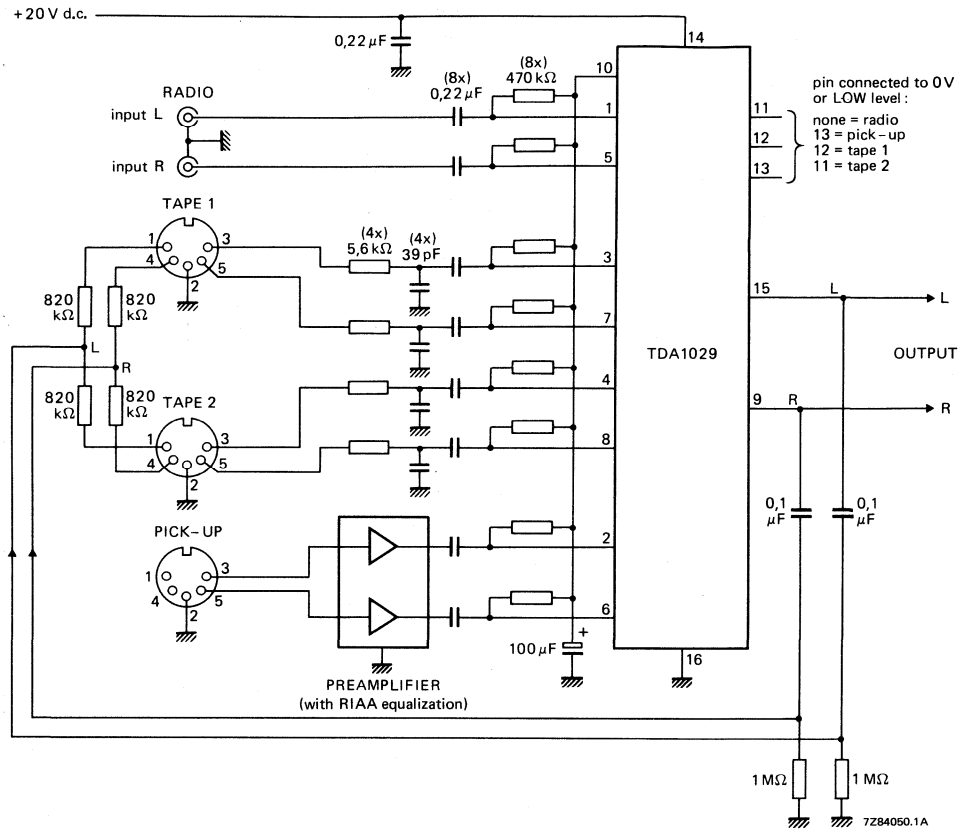


Fig. 8 TDA1029 connected as a four input stereo source selector.

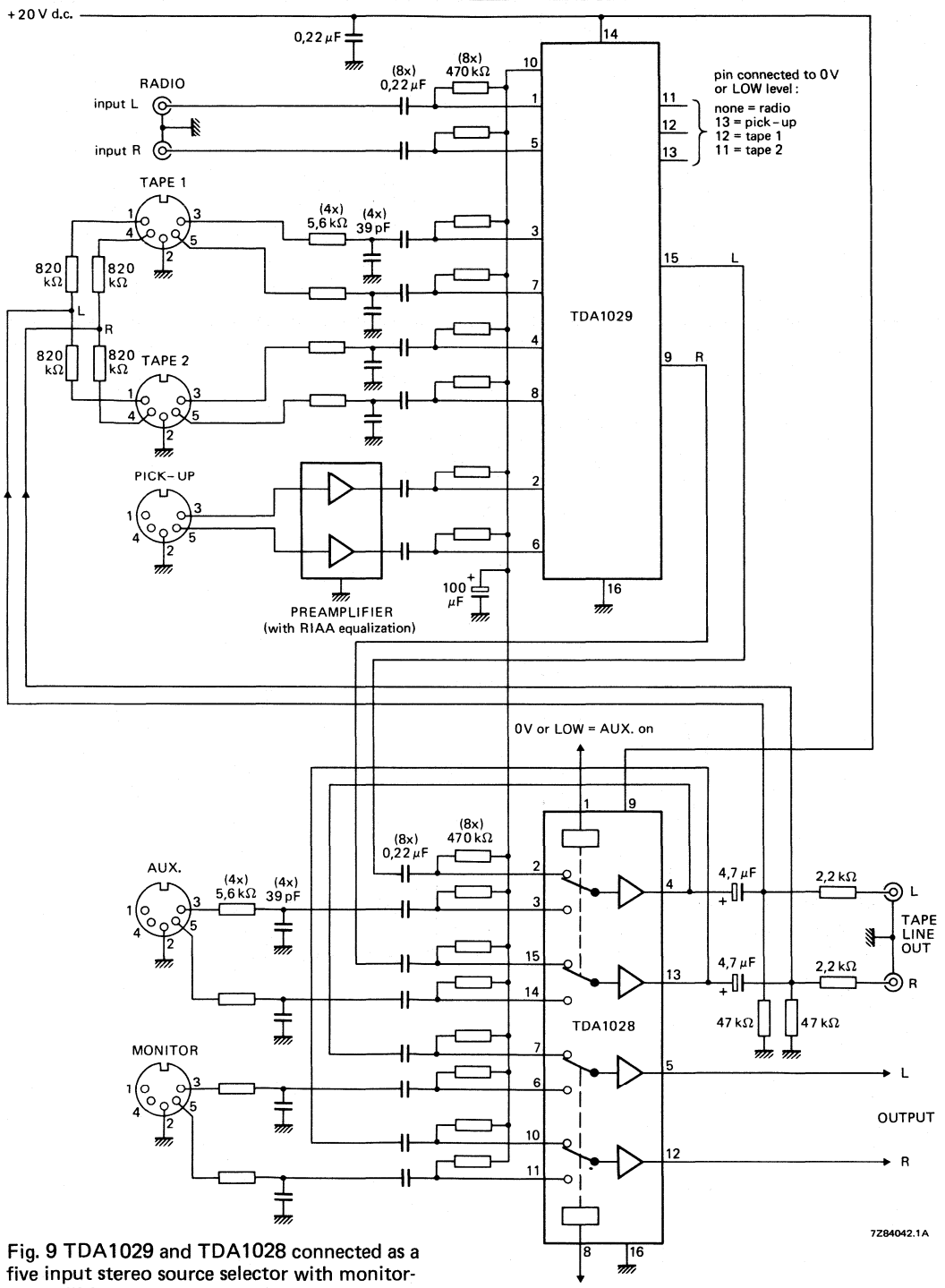


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

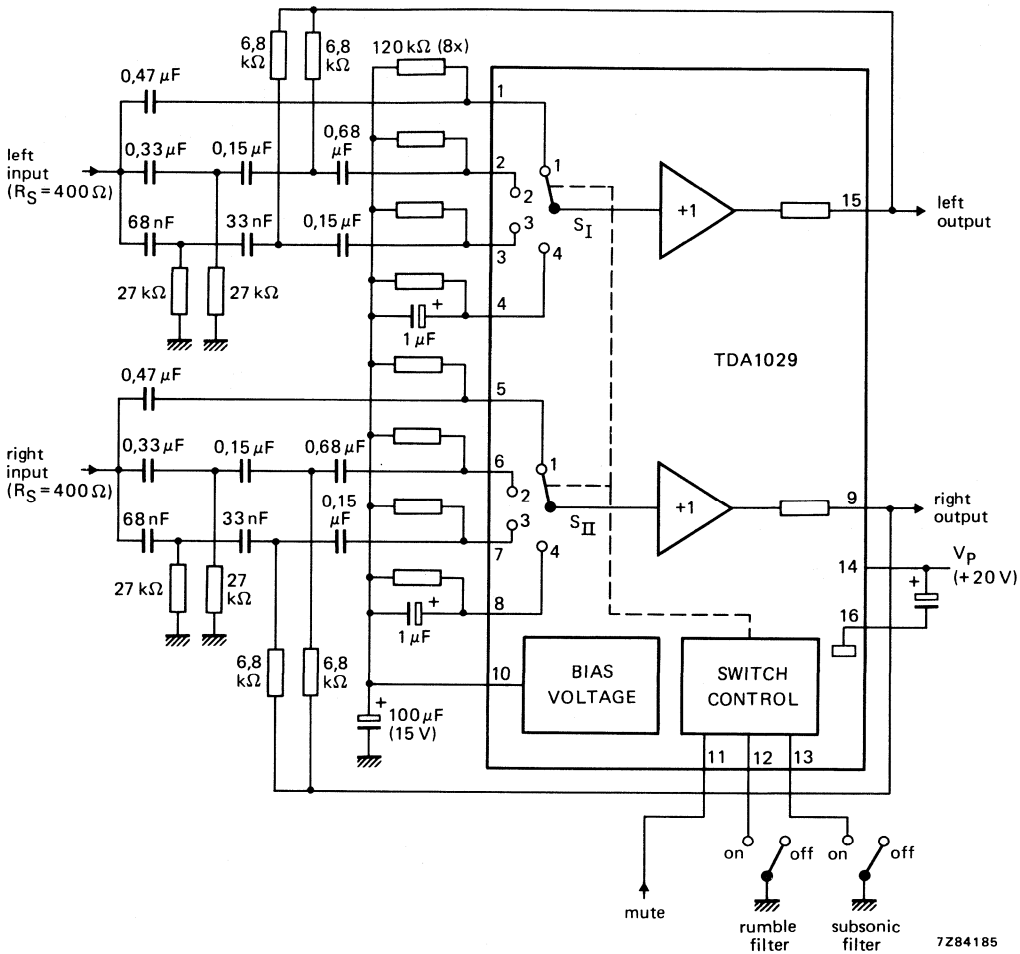


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

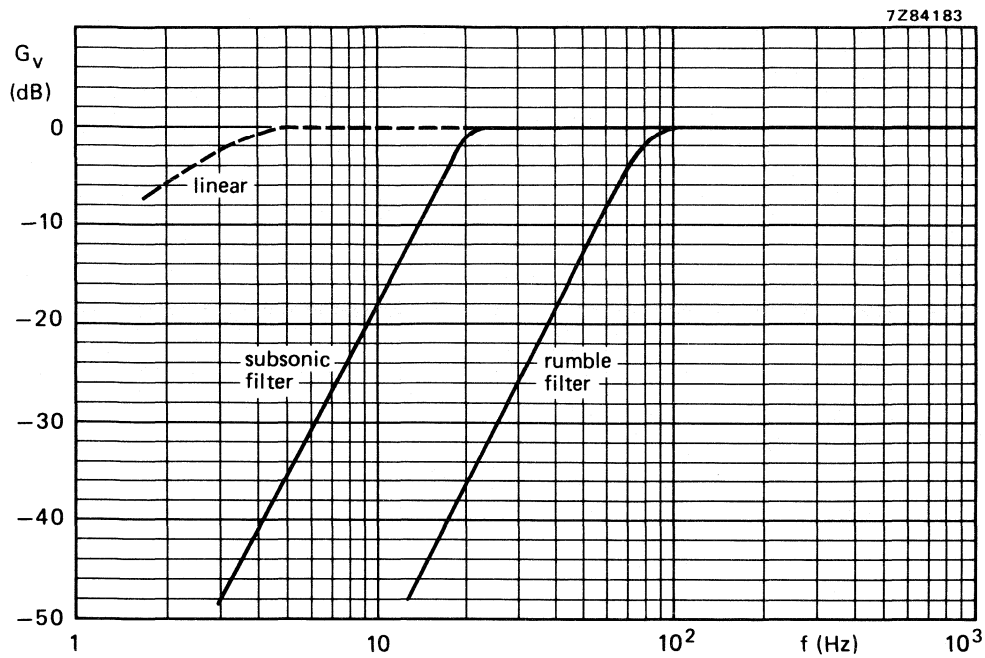


Fig. 11 Frequency response curves for the circuit of Fig. 10.

EAST-WEST CORRECTION DRIVER CIRCUIT

The TDA1082 is a monolithic integrated circuit driving east-west correction of colour tubes in television receivers. The circuit can be used for class-A and class-D operation and incorporates the following functions:

- differential input amplifier
- squaring stage
- differential output amplifier with driver stage
- protection stage with threshold
- switching off the correction during flyback
- voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 1)	V_P	typ.	12 V
Current consumption	I_P	typ.	17 mA
Total power dissipation	P_{tot}	max.	600 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C
Collector voltage drift external transistor	ΔV_C	typ.	0,7 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

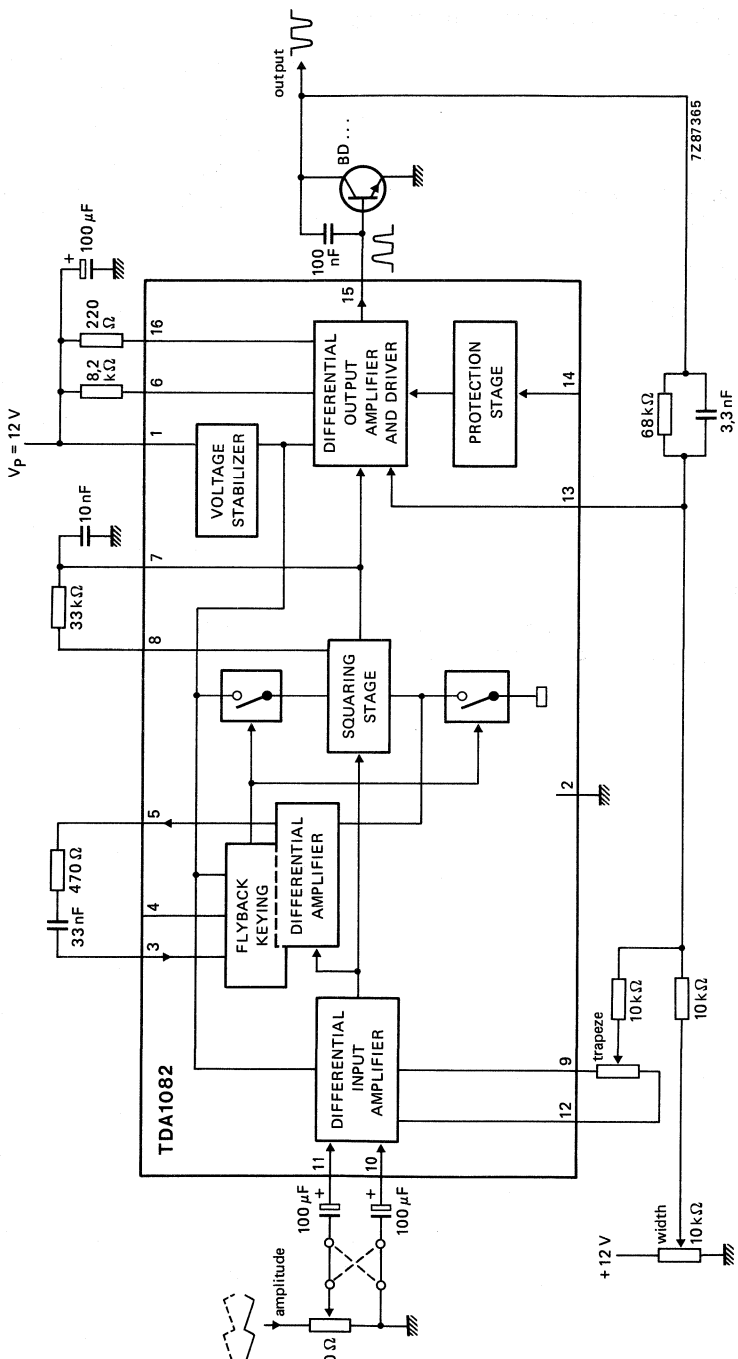


Fig. 1 Block diagram with external components (class-A operation). Also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	V_P	max.	16	V
Output current (pin 15)	$-I_O$	max.	50	mA
Total power dissipation	P_{tot}	max.	600	mW
Storage temperature range	T_{stg}	−25 to +150		°C
Operating ambient temperature range	T_{amb}	0 to +70		°C

Voltages

with respect to ground (pin 2)	min.	max.	
Pins 1, 5, 7, 8, 9, 12, 13 and 16	0	16	V
Pins 3 and 4	0	−	V
Pins 10, 11 and 15	0	5	V

Currents

Pins 3, 4 and 6	−	5	mA
Pin 14	0	1,5	mA
Pins 15 and 16 ($-I_{15}$ and $+I_{16}$)	0	50	mA

CHARACTERISTICS

V_P = 12 V (range 10,5 to 14 V); T_{amb} = 25; measured in circuit Fig. 1 with colour tube A66-500X; unless otherwise specified

Supply

Voltage range	V_P	10,5	to	14	V
Voltage peak value	V_{PM}	max.		15	V
Current range	I_P	11	to	30	mA
Current typical value	I_P	typ.		17	mA

Sawtooth signal (pin 10 or 11)

Input voltage d.c. value	V_i	typ.	2,5	V
Input resistance	R_i	typ.	5,6	kΩ
		<	7,0	kΩ

Correcting signals (pin 13)

Input voltage d.c. value	V_{13}	typ.	0,6	V
Input current	I_{13}	typ.	0,5	mA

Flyback keying (pin 3)

Input current range	I_3	0,05	to	5	mA
Peak value, d = 5%	I_3	typ.		20	mA

Threshold (pin 14)

Input voltage at I_{14} = 200 μA for switching off the driver stage	V_i	typ.		8	V
		7,2	to	8,8	V

Output stage (pin 6)			
Generator current	I_6	typ.	1 mA
Flyback differential amplifier (pin 5)			
D.C. value output voltage	V_5	typ.	6 V
Output resistance	R_5	typ.	5,6 kΩ
Squaring stage (pin 7)			
D.C. value output voltage	V_7	typ.	6 V
Peak to peak value output voltage	$V_{7(p-p)}$	typ.	1,5 V
Output resistance	R_7	5,6 to typ.	9,4 kΩ 7,5 kΩ
Correction trapezoidal deformation (pins 9 and 12)			
D.C. voltage	$V_{9,12}$	typ.	5 V
Output resistance	$R_{9,12}$	typ.	7,5 kΩ
Driver output (pin 15)			
Output current	$-I_{15}$	<	50 mA
Drift of d.c. collector voltage			
Of external transistor in closed loop T_{amb} = 15 to 70 °C; V_{CO} = 8 V	ΔV_C	typ.	0,7 V

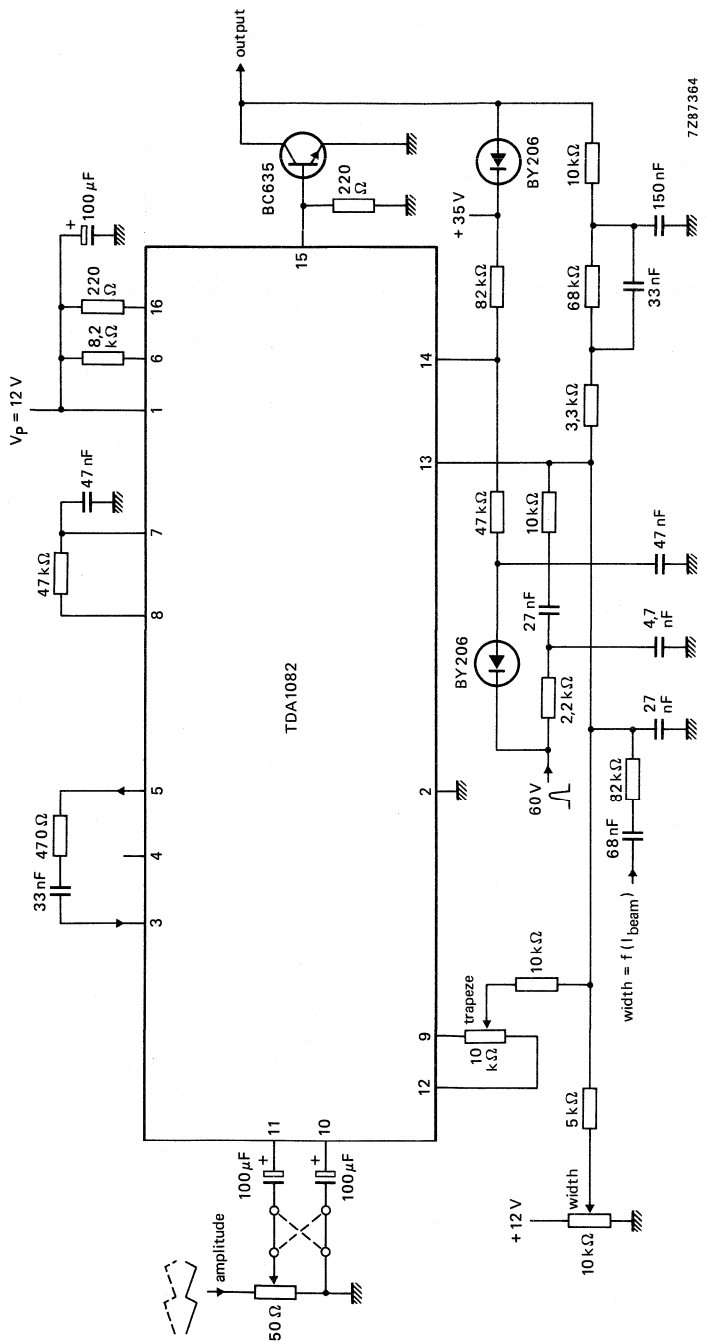


Fig. 2 Application circuit E-W-correction (class-D operation).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

12 to 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512A is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA
Output power at d_{tot} = 0,7%			
sine-wave power			
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13 W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7 W
music power			
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21 W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12 W
Closed-loop voltage gain (externally determined)	G_c	typ.	30 dB
Input resistance (externally determined)	R_i	typ.	20 kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72 dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50 dB

PACKAGE OUTLINES

TDA1512A: 9-lead SIL; plastic power (SOT131).
TDA1512AQ: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

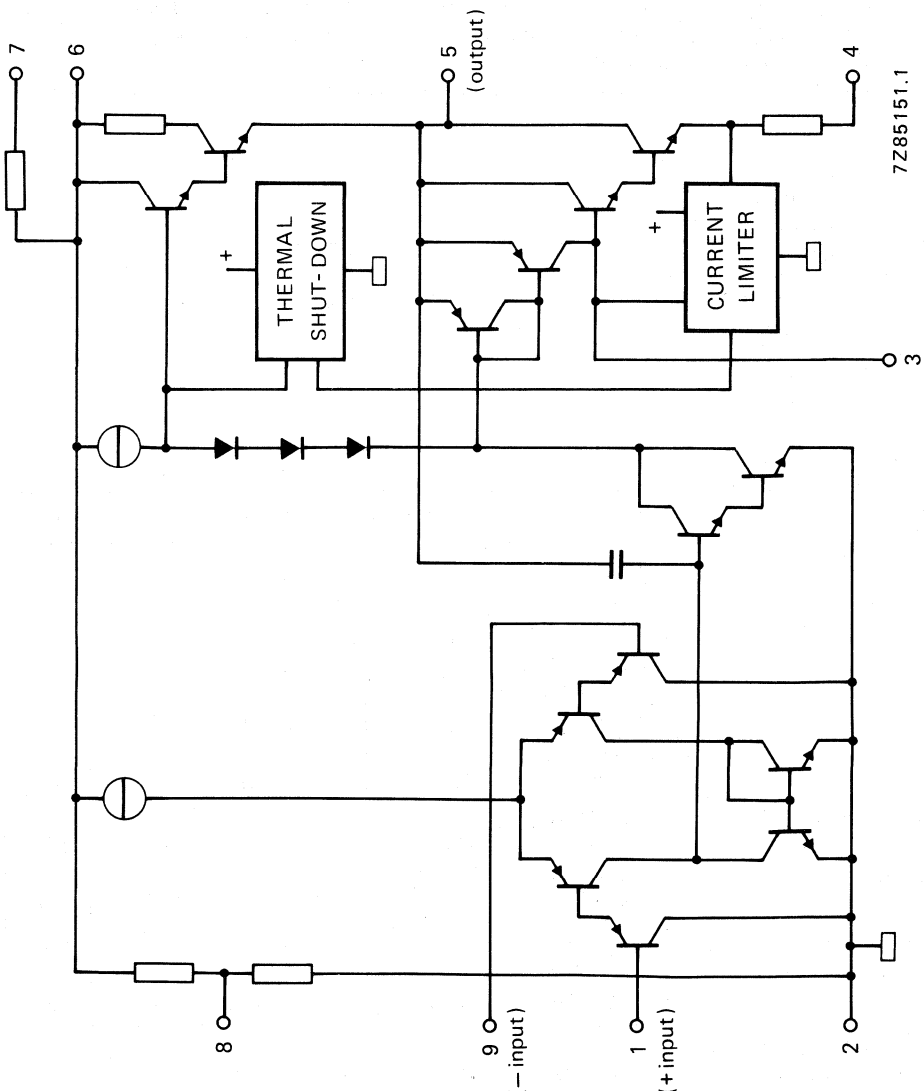


Fig. 1 Simplified internal circuit diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

50 W HIGH- PERFORMANCE HI-FI AMPLIFIER

GENERAL DESCRIPTION

The TDA1514A integrated circuit is a hi-fi power amplifier for use as a building block in radio, tv and other audio applications. The high performance of the IC meets the requirements of digital sources (e.g. Compact Disc equipment).
The circuit is totally protected, the two output transistors both having thermal and SOAR protection (see Fig.3). The circuit also has a mute function that can be arranged for a period after power-on with a delay time fixed by external components.
The device is intended for symmetrical power supplies but an asymmetrical supply may also be used.

Features

- High output power
- Low harmonic distortion
- Low intermodulation distortion
- Low offset voltage
- Good ripple rejection
- Mute/stand-by facilities
- Thermal protection
- Protected against electrostatic discharge
- No switch-on or switch-off clicks
- Very low thermal resistance
- Safe Operating Area (SOAR) protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 10	–	± 30	V
Total quiescent current	V_P = ± 27.5 V	I_{tot}	–	56	–	mA
Output power	THD = –60 dB; V_P = ± 27.5 V; R_L = 8 Ω	P_o	–	40	–	W
	V_P = ± 23 V; R_L = 4 Ω	P_o	–	50	–	W
Closed loop voltage gain	determined externally	G_c	–	30	–	dB
Input resistance	determined externally	R_i	–	20	–	kΩ
Signal plus noise-to-noise ratio	P_o = 50 mW	(S+N)/N	–	82	–	dB
Supply voltage ripple rejection	f = 100 Hz	SVRR	–	64	–	dB

PACKAGE OUTLINE

9-lead SIL, plastic power (SOT131A).

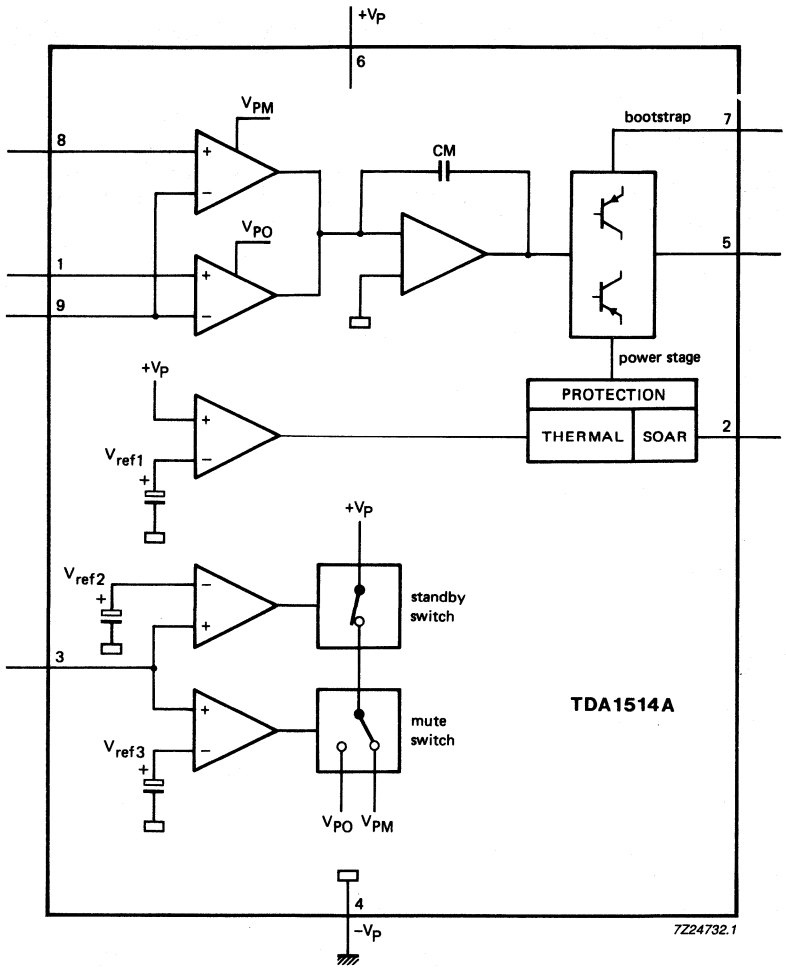


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

20 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1520B is an integrated hi-fi audio power amplifier designed for use with non-stabilized symmetrical or stabilized asymmetrical power supplies in mains-fed applications (e.g. stereo radio, stereo TV sound and cassette recorder).

Features

- Low offset voltage at output (suitable for BTL application)
- Low cross-over and secondary cross-over distortion
- Low intermodulation and transient intermodulation distortion
- Low harmonic distortion
- Good hum suppression
- High slew rate
- No switch-on/switch-off plop
- Thermal protection

QUICK REFERENCE DATA (note 1)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	15	–	50	V
Total quiescent current		I_{tot}	22	60	105	mA
Output power at THD = 0,5%		P_o	20	22	–	W
Input impedance		Z_I	1000	–	–	kΩ
Signal plus noise to noise ratio at P_O = 50 mW	note 2	(S+N)/N	70	75	–	dB
Supply voltage ripple rejection at R_S = 0 Ω	f = 100 Hz	SVRR	45	60	–	dB
	f = 10 kHz	SVRR	45	80	–	dB

Notes to the Quick Reference Data

1. All values measured from test circuit Fig.6; V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.
2. Bandwidth is 20 Hz to 20 kHz; R_S = 2 kΩ (RMS value).

PACKAGE OUTLINES

TDA1520B: 9-lead SIL; plastic power (SOT131).
TDA1520BQ: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

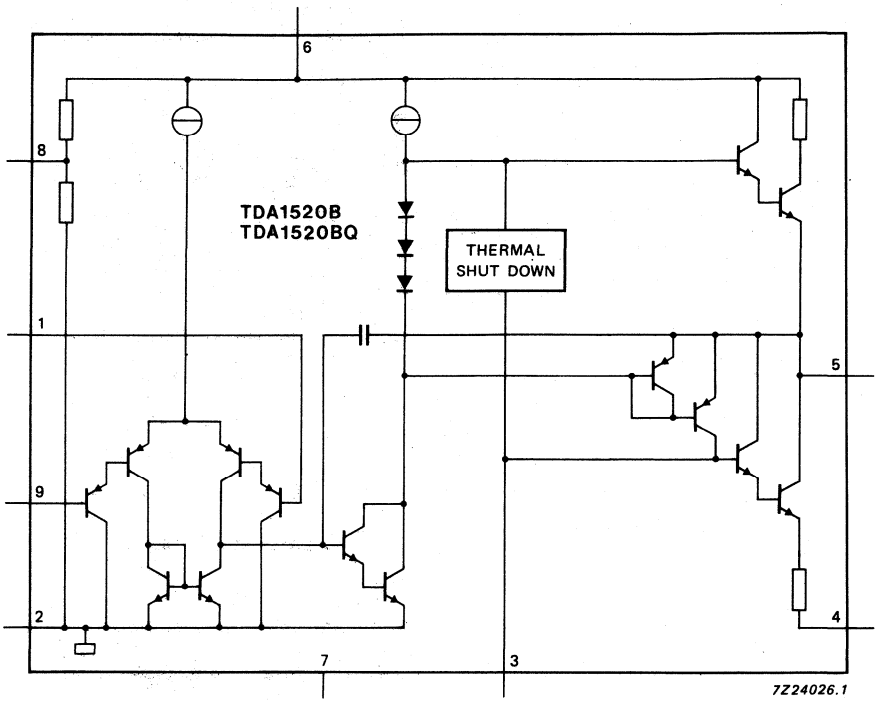


Fig. 1 Block diagram.

PINNING

1 Non-inverting input
2 Input ground (substrate)
3 Compensation
4 Negative supply (ground)
5 Output
6 Positive supply (V_P)
7 Not connected
8 Supply voltage ripple rejection
9 Inverting input (feedback)

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

2 x 12 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521/TDA1521Q is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 16 V	P_O	typ. 12	W
Voltage gain	G_V	typ. 30	dB
Gain balance between channels	ΔG_V	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINES

TDA1521: 9-lead single in-line; plastic power (SOT131).
TDA1521Q: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

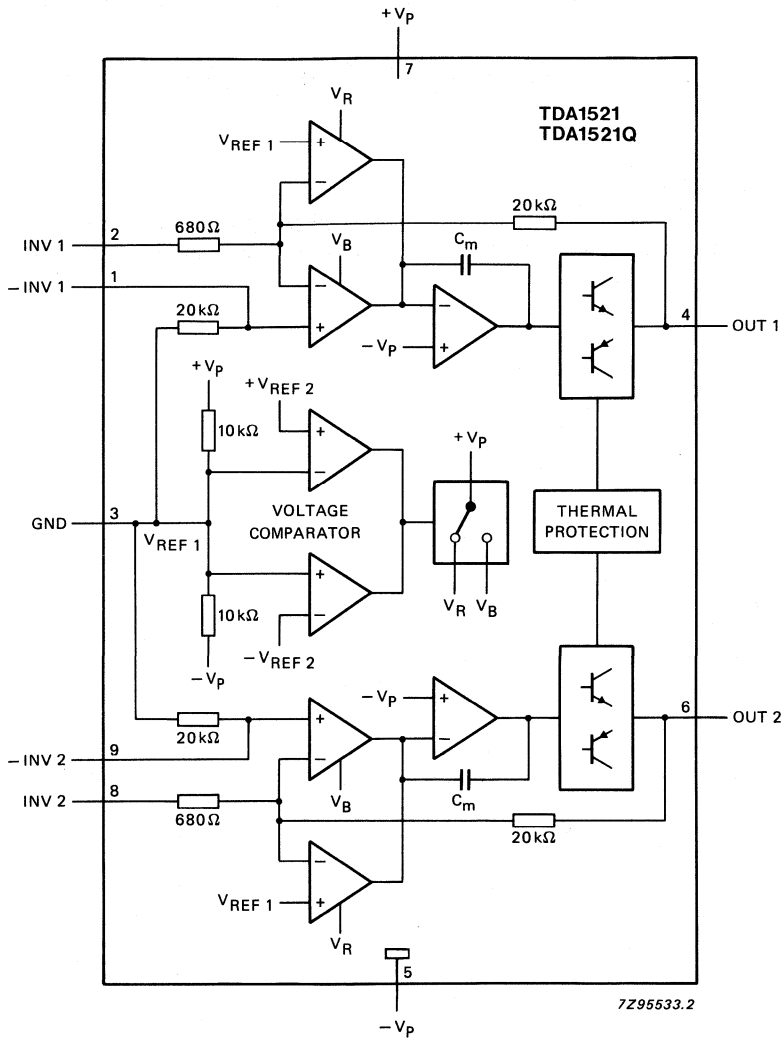


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ Vp (asymmetrical)
4	OUT1	output 1
5	–Vp	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	+ Vp	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

2 x 6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521A is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 12 V	P_O	typ. 6	W
Voltage gain	G_V	typ. 30	dB
Gain balance between channels	ΔG_V	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINE

TDA1521A: 9-lead single in-line; plastic power (SOT 110B).

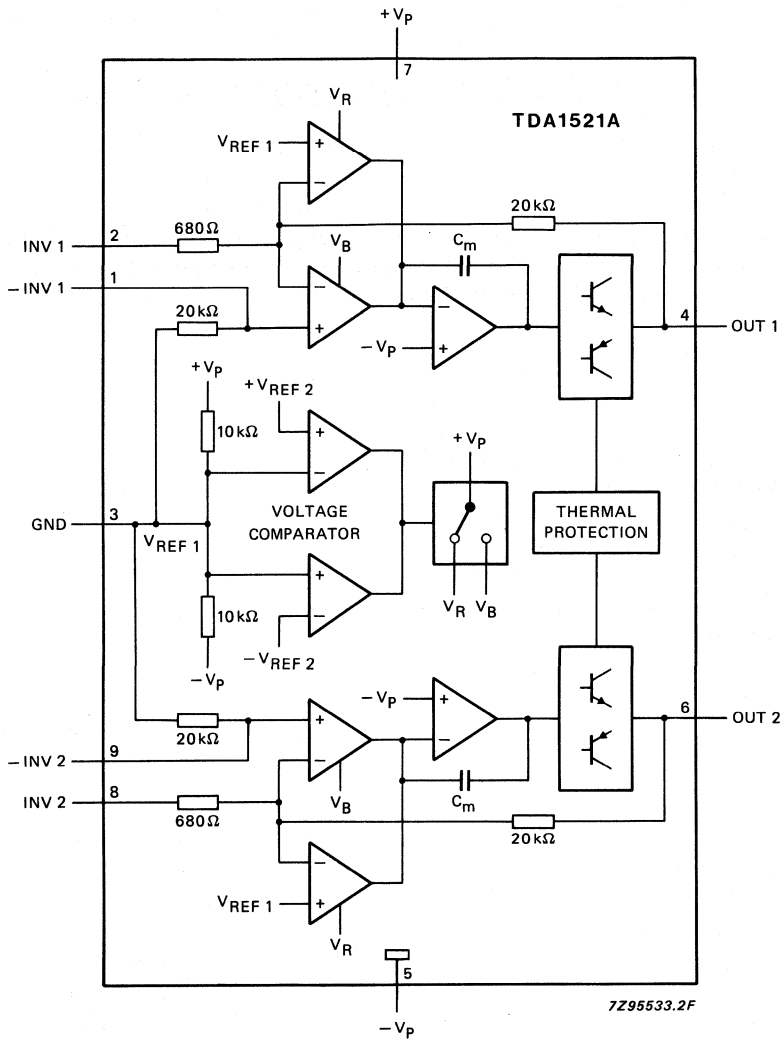


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) ½ V_P (asymmetrical)
4	OUT1	output 1
5	$-V_P$	negative supply (symmetrical) ground (asymmetrical)
6	OUT2	output 2
7	$+V_P$	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

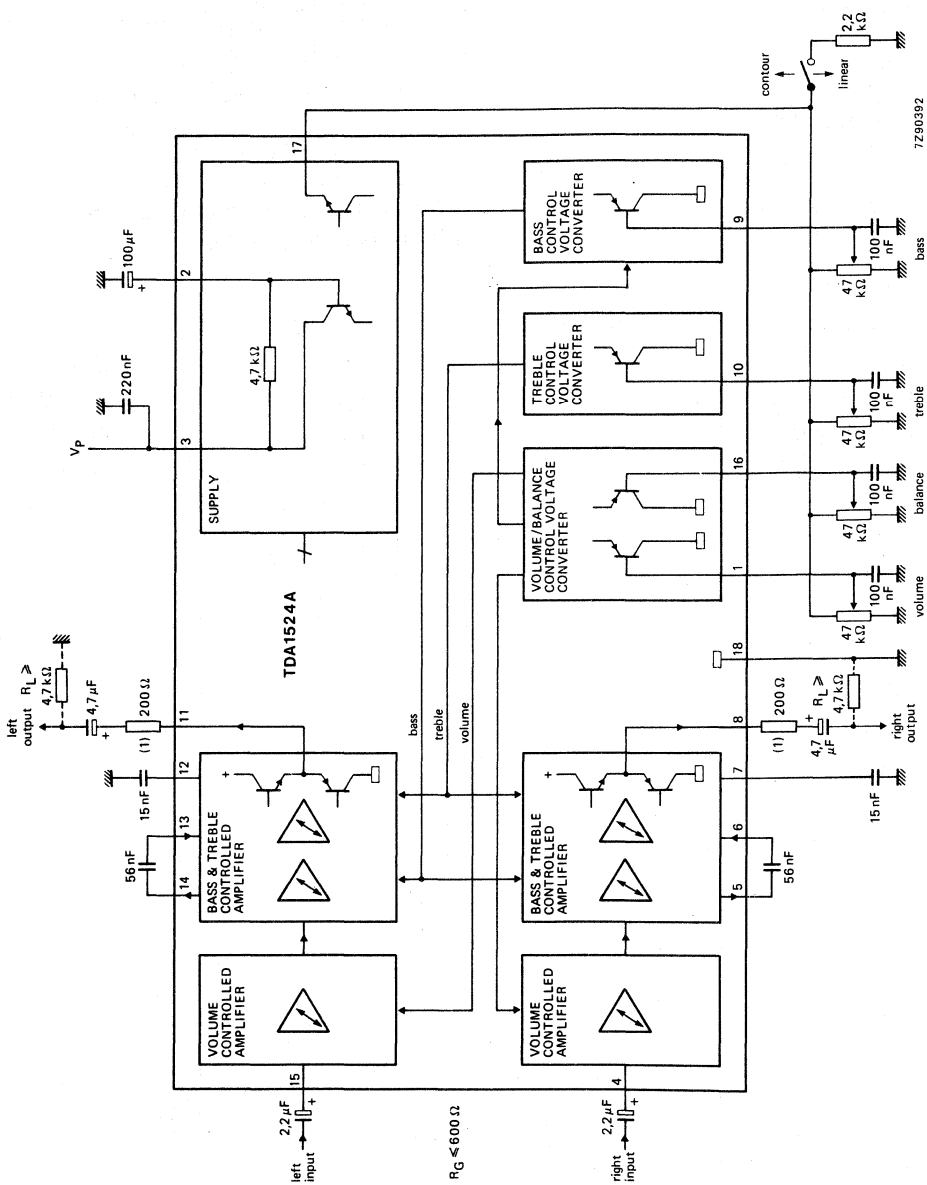
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	G_v		−80 to + 21,5 dB
Bass control range at 40 Hz	ΔG_v		−19 to + 17 dB
Treble control range at 16 kHz	ΔG_v	typ.	± 15 dB
Total harmonic distortion	THD	typ.	0,3 %
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; V_P = 12 V;			
for max. voltage gain	$V_{no(rms)}$	typ.	310 μV
for voltage gain G_v = −40 dB	$V_{no(rms)}$	typ.	100 μV
Channel separation at G_v = −20 to + 21,5 dB	α_{cs}	typ.	60 dB
Tracking between channels at G_v = −20 to + 26 dB	ΔG_v	max.	2,5 dB
Ripple rejection at 100 Hz	RR	typ.	50 dB
Supply voltage range (pin 3)	$V_P = V_{3\text{-}18}$		7,5 to 16,5 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

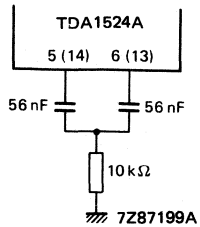


Fig. 2 Double-pole low-pass filter for improved bass-boost.

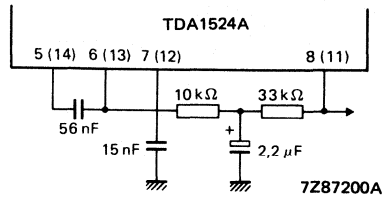


Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	max.	20 V
Total power dissipation	P_{tot}	max.	1200 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

D.C. CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7,5	–	16,5	V
Supply current					
at V_P = 8,5 V	$I_P = I_3$	19	27	35	mA
at V_P = 12 V	$I_P = I_3$	25	35	45	mA
at V_P = 15 V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at V_P = 8,5 V	$V_{4,15-18}$	3,8	4,25	4,7	V
at V_P = 12 V	$V_{4,15-18}$	5,3	5,9	6,6	V
at V_P = 15 V	$V_{4,15-18}$	6,5	7,3	8,2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at V_P = 8,5 V	$V_{8,11-18}$	3,3	4,25	5,2	V
at V_P = 12 V	$V_{8,11-18}$	4,6	6,0	7,4	V
at V_P = 15 V	$V_{8,11-18}$	5,7	7,5	9,3	V
Pin 17					
Internal potentiometer supply voltage at V_P = 8,5 V	V_{17-18}	3,5	3,75	4,0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4,5	–	$V_P/2-V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at V_{17-18} = 5 V	$V_{1,9,10,16}$	1,0	–	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	–	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

A.C. CHARACTERISTICS

$V_P = V_{3-18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{V\,max}$	20,5	21,5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; G_V = 0 dB (Fig. 6)	ΔG_V	–	−40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_V	–	−19 to + 17 ± 3		dB
Treble control range at 16 kHz (Fig. 8)	ΔG_V	–	± 15 ± 3	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: G_V = 20 dB	$R_{i4,15}$	10	–	–	kΩ
G_V = −40 dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at G_V = −20 to + 21,5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0{,}5\ V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0{,}5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1,5	dB
Tracking between channels					
for G_V = 21,5 to −26 dB					
f = 250 Hz to 6,3 kHz; balance adjusted at					
G_V = 10 dB	ΔG_V	–	–	2,5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1,8	2,0	–	V
at V_P = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2,2	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2,5	3,0	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3,5	–	V
Noise performance (V_P = 8,5 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_v = −3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_v = −16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	400	–	μV

parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_V = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405					
of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble					
(contour off; G_V = −40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_V}\ ;\ G_{V\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

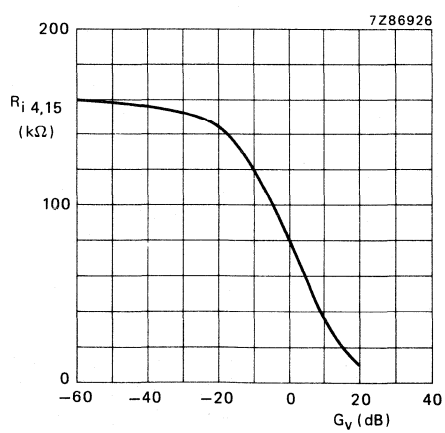


Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

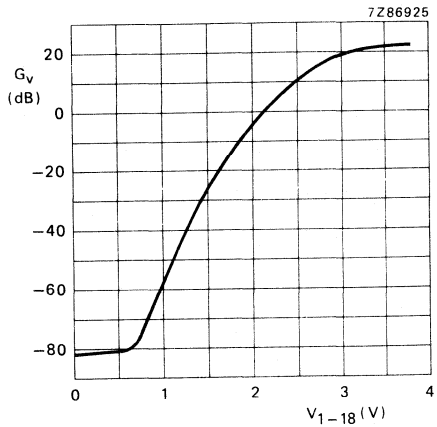


Fig. 5 Volume control curve; voltage gain (G_v) as a function of control voltage (V_{1-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 1 kHz.

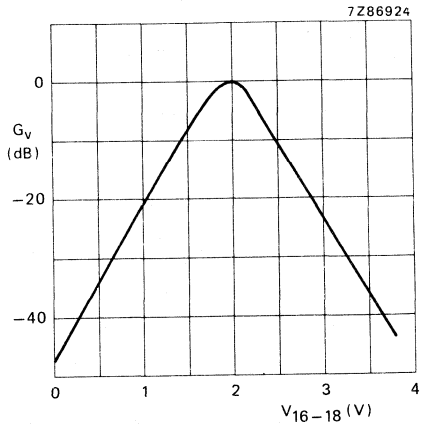


Fig. 6 Balance control curve; voltage gain (G_v) as a function of control voltage (V_{16-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V.

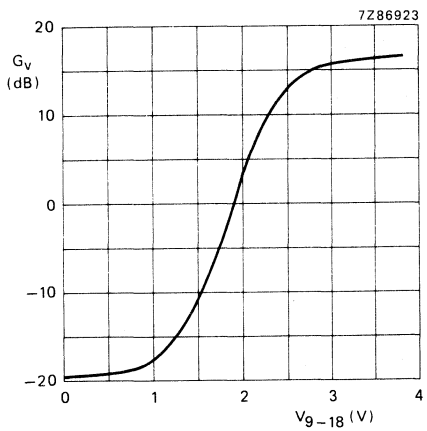


Fig. 7 Bass control curve; voltage gain (G_v) as a function of control voltage (V_{9-18}). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 40 Hz.

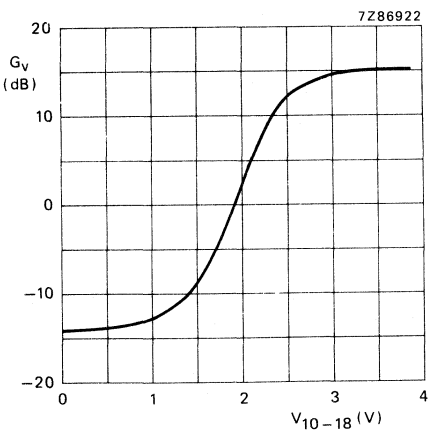


Fig. 8 Treble control curve; voltage gain (G_v) as a function of control voltage (V_{10-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 16 kHz.

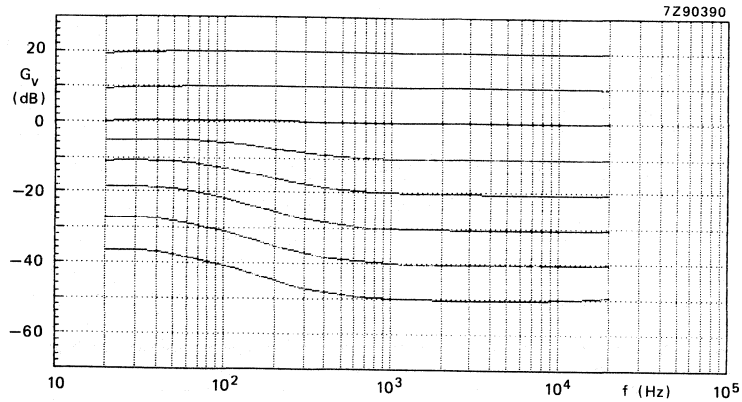


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

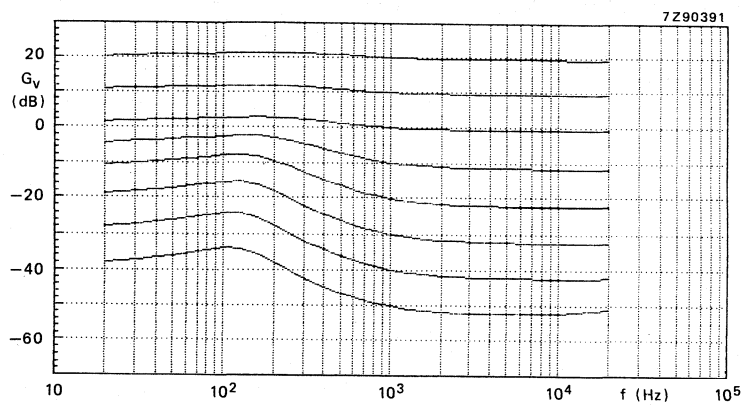


Fig. 10 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

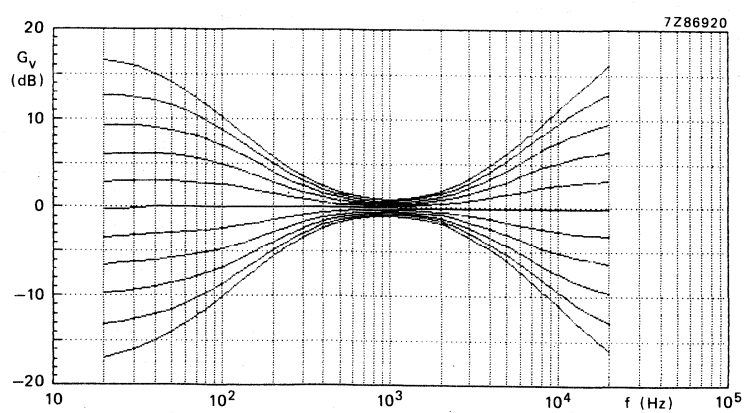


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

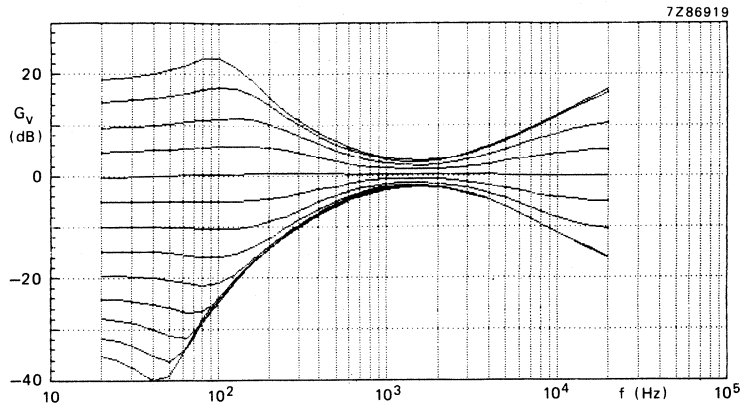


Fig. 12 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

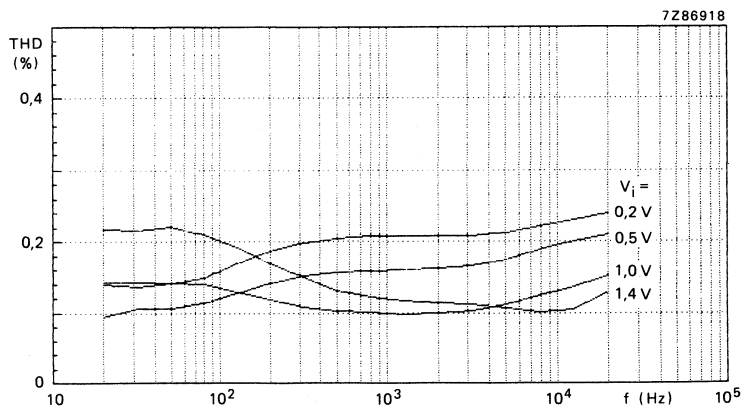


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8,5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

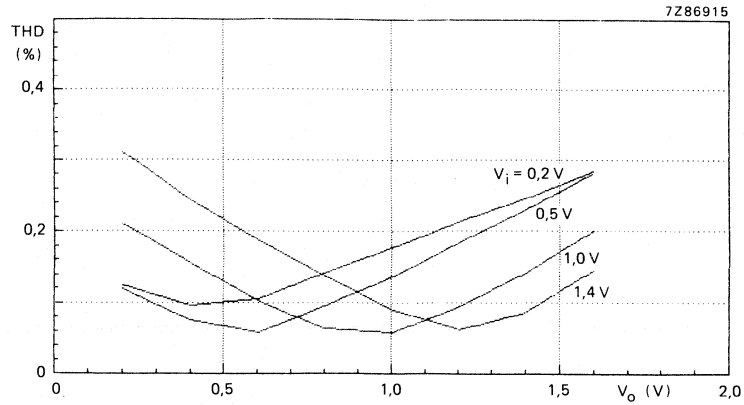
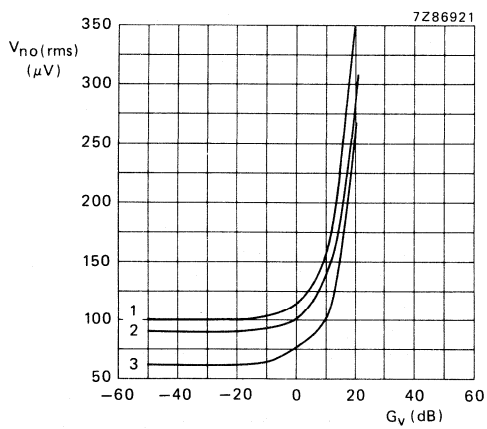


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig. 1; V_P = 8,5 V; f_i = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by DC voltages or by single linear potentiometers.

Features

- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

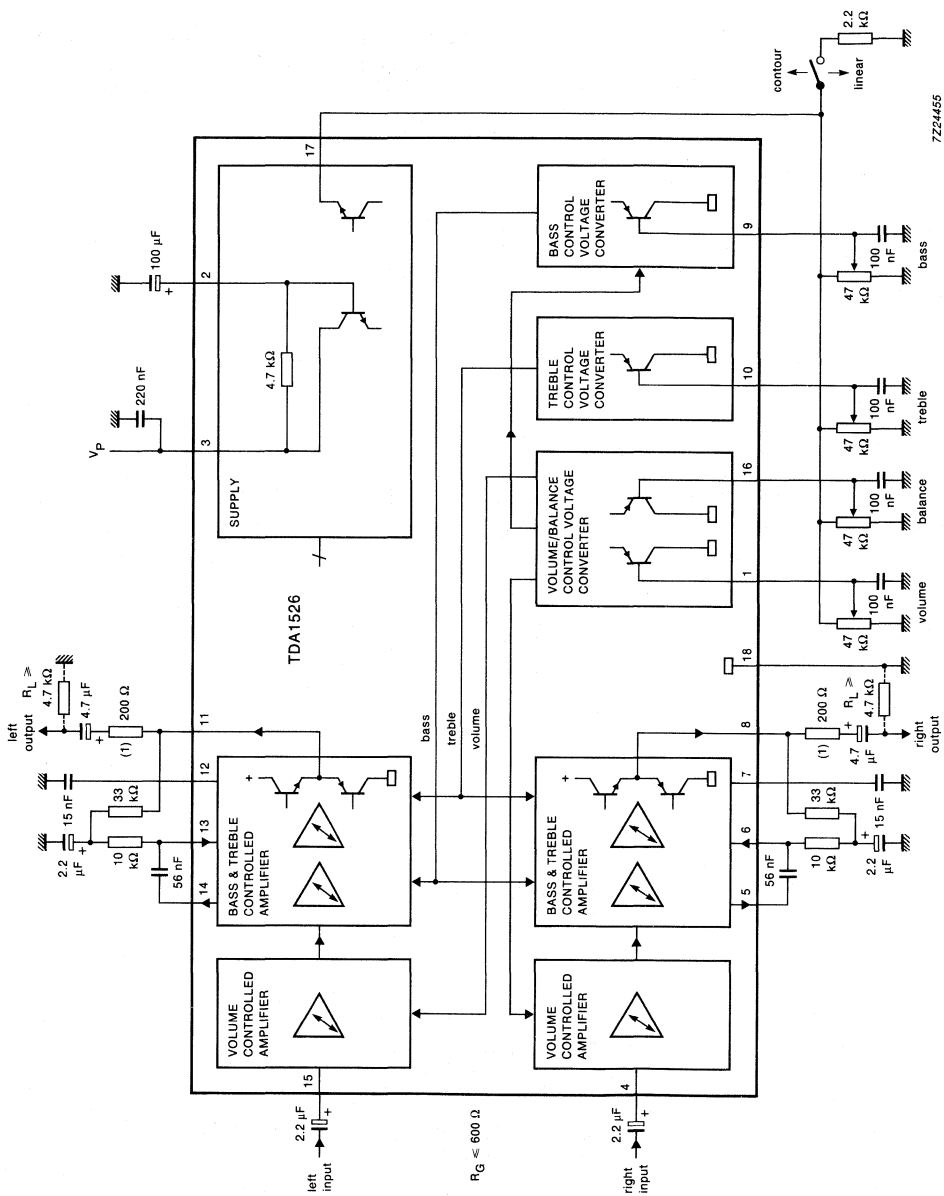
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_P	7.5	12	16.5	V
Supply current (pin 3)	V_P = 12 V	I_P	25	35	45	mA
Signal handling with DC feedback	V_P = 8.5 to 15 V; THD = 0.7%; f = 1 kHz					
Input signal handling (RMS value)		$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (RMS value)	notes 2 and 3	$V_{o(rms)}$	1.8	2.0	–	V
Control range						
Maximum gain of volume	see Fig. 4	$G_{V\,max}$	20.5	21.5	23	dB
Volume control range	$G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range	G_V = 0 dB; see Fig. 5	ΔG_V	–	–40	–	dB
Bass control range	at 40 Hz; see Fig. 6	ΔG_V	–	–19 to +17 ±3	–	dB
Treble control range	at 16 kHz; see Fig. 7	ΔG_V	–	±15 ±3	–	dB
Total harmonic distortion		THD	–	–	0.5	%
Noise performance	V_P = 12 V					
Output noise voltage (unweighted) at f = 20 Hz to 20 kHz for G_V = –16 dB	RMS value; note 4 note 5	$V_{no(rms)}$	–	100	200	μV
Signal processing						
Channel separation at G_V = –20 to 21.5 dB	f = 250 Hz to 10 kHz	α_{cs}	46	60	–	dB
Tracking between channels for G_V = 21.5 to –26 dB	f = 250 Hz to 6.3 kHz; balance at G_V = 10 dB	ΔG_V	–	–	2.5	dB
Ripple rejection	$V_{P(rms)} = \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Operating ambient temperature range		T_{amb}	–30	–	+85	°C

For explanation of notes see **Notes to the characteristics.**

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig.1 Block diagram and application circuit with single-pole filter.

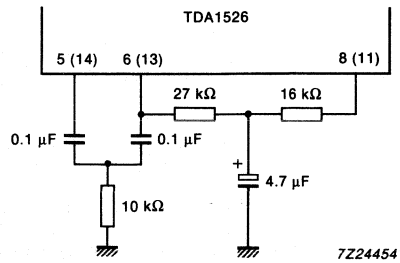


Fig.2 Double-pole low-pass filter for improved bass-boost.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	20	V
Total power dissipation	P_{tot}	–	1200	mW
Storage temperature range	T_{stg}	–55	+ 150	°C
Operating ambient temperature range	T_{amb}	–30	+ 80	°C

DC CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7.5	–	16.5	V
Supply current					
at $V_P = 8.5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
DC input levels (pins 4 and 15)					
at $V_P = 8.5$ V	$V_{4,15-18}$	3.8	4.25	4.7	V
at $V_P = 12$ V	$V_{4,15-18}$	5.3	5.9	6.6	V
at $V_P = 15$ V	$V_{4,15-18}$	6.5	7.3	8.2	V
DC output levels (pins 8 and 11) under all control voltage conditions with DC feedback					
at $V_P = 8.5$ V	$V_{8,11-18}$	3.3	4.25	5.2	V
at $V_P = 12$ V	$V_{8,11-18}$	4.6	6.0	7.4	V
at $V_P = 15$ V	$V_{8,11-18}$	5.7	7.5	9.3	V
Pin 17					
Internal potentiometer supply voltage at $V_P = 8.5$ V	V_{17-18}	3.5	3.75	4.0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0.5	mA
linear (switch closed)	$-I_{17}$	1.5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10.8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4.5	–	$V_P/2 - V_{BE}$	V
DC control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1.0	–	4.25	V
using internal supply	$V_{1,9,10,16}$	0.25	–	3.8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

AC CHARACTERISTICS

$V_P = V_{3-18} = 8.5$ V; $T_{amb} = 25$ °C; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Maximum gain of volume (Fig. 4)	$G_{V\,max}$	20.5	21.5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; G_V = 0 dB (Fig. 5)	ΔG_V	–	–40	–	dB
Bass control range at 40 Hz (Fig. 6)	ΔG_V	–	–19 to +17 ±3		dB
Treble control range at 16 kHz (Fig. 7)	ΔG_V	–	±15 ±3	–	dB
Contour characteristics			see Figs 9 and 10		
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: G_V = 20 dB	$R_{i4,15}$	10	–	–	kΩ
G_V = –40 dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at G_V = –20 to +21.5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0.5\ V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0.5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1.5	dB
Tracking between channels					
for G_V = 21.5 to –26 dB					
f = 250 Hz to 6.3 kHz; balance adjusted at					
G_V = 10 dB	ΔG_V	–	–	2.5	dB

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with DC feedback					
Input signal handling at V_P = 8.5 V – 15 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (note 2 and note 3) at V_P = 8.5 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{o(rms)}$	1.8	2.0	–	V
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 14) at f = 20 Hz to 20 kHz (RMS value; note 4) for G_V = –16 dB (note 5)	$V_{no(rms)}$	–	100	200	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 3)

$$R_i = \frac{160\,k\Omega}{1 + G_V}; G_{V\,max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. For peak values add 4.5 dB to RMS values.
5. Linear frequency response.

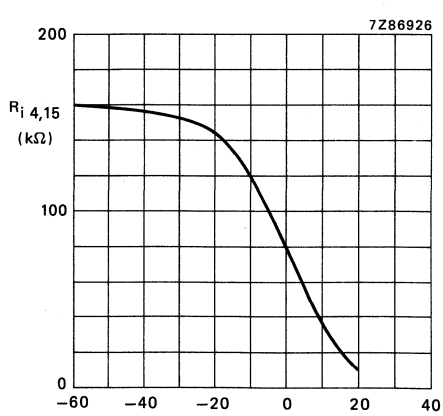


Fig.3 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig.1.

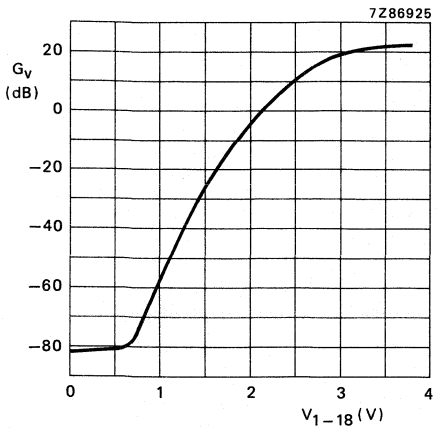


Fig.4 Volume control curve; voltage gain (G_v) as a function of control voltage (V_{1-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 1 kHz.

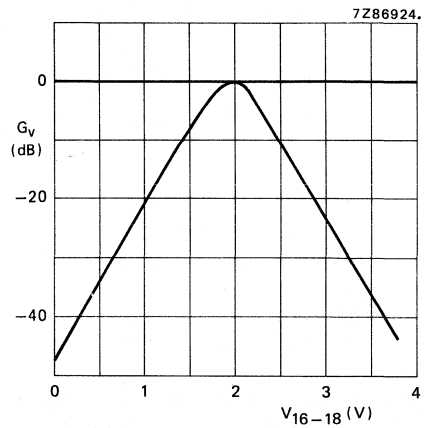


Fig.5 Balance control curve; voltage gain (G_v) as a function of control voltage (V_{16-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V.

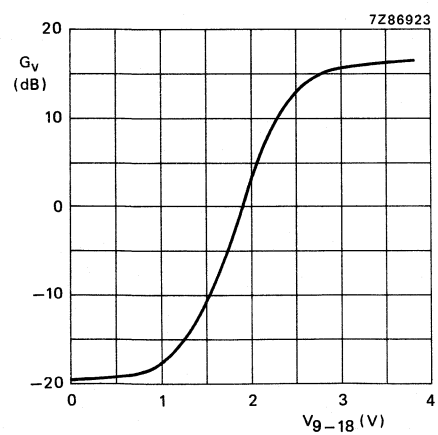


Fig.6 Bass control curve; voltage gain (G_v) as a function of control voltage (V_{9-18}). Measured in Fig.1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 40 Hz.

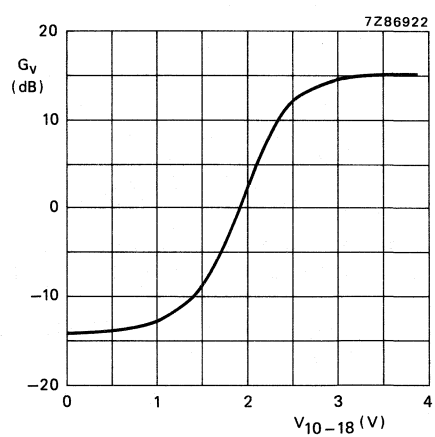


Fig.7 Treble control curve; voltage gain (G_v) as a function of control voltage (V_{10-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 16 kHz.

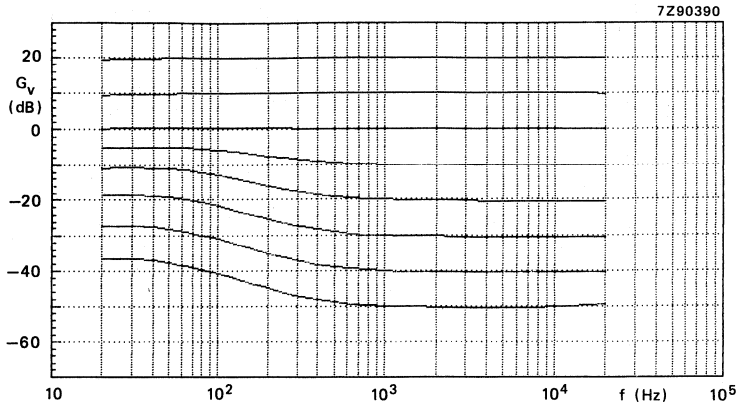


Fig.8 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

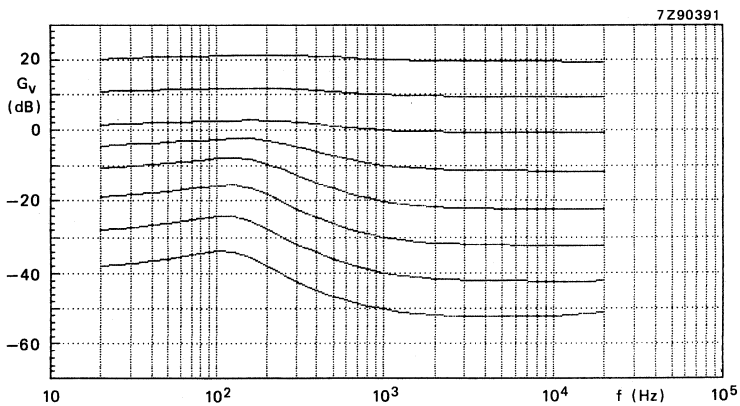


Fig.9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

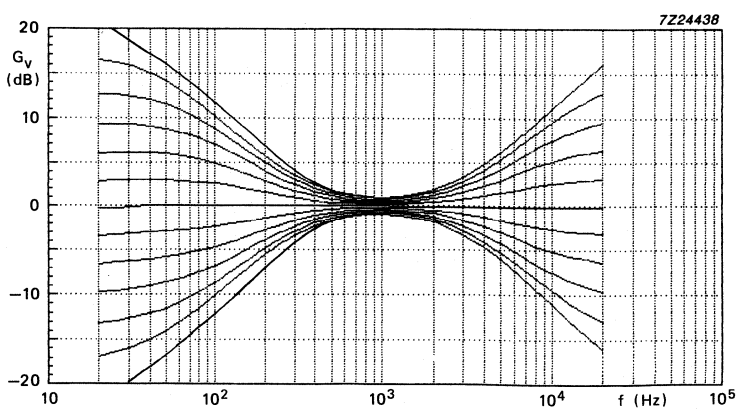


Fig.10 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

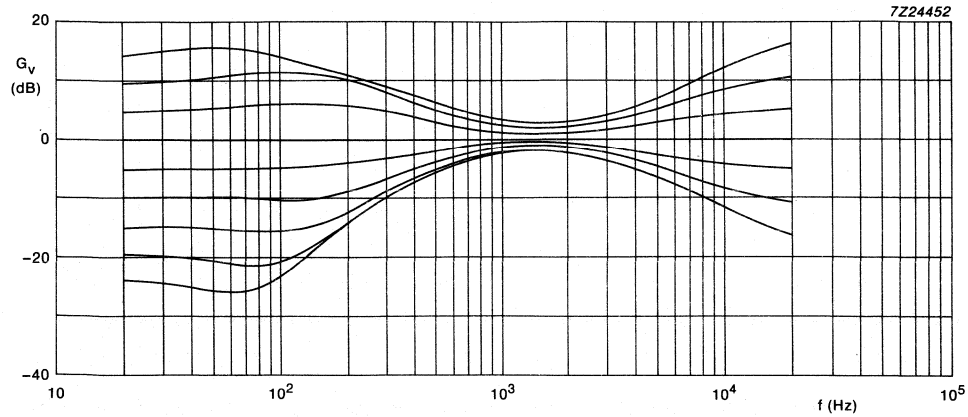


Fig.11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

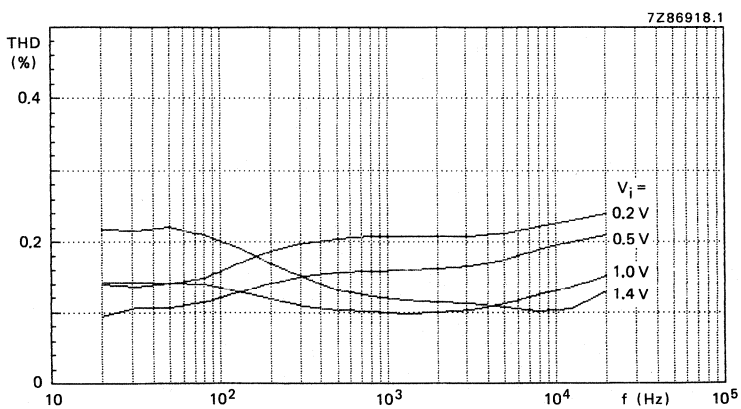


Fig.12 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig.1; V_P = 8.5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

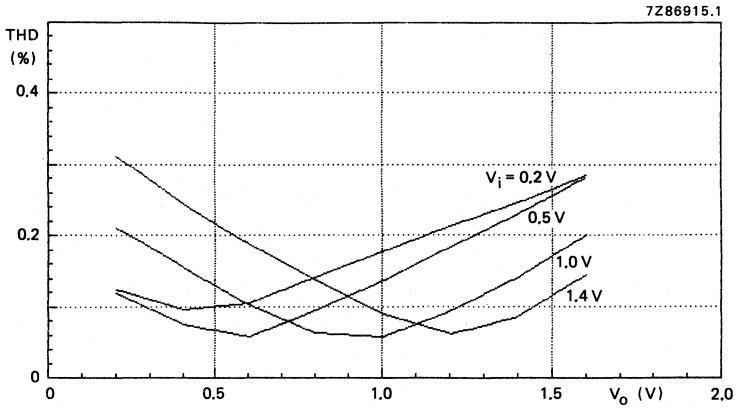


Fig.13 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig.1; V_P = 8.5 V; f_i = 1 kHz.

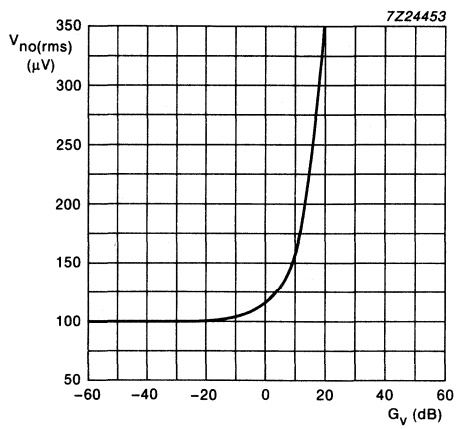


Fig.14 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig.1; V_P = 15 V; f = 20 Hz to 20 kHz.

Philips Semiconductors

Data sheet	
status	Objective specification
date of issue	February 1991

TDA1534

14-bit analog-to-digital converter (ADC)

GENERAL DESCRIPTION

An integrated 14-bit analog-to-digital converter (ADC) which uses the successive approximation conversion technique and includes the comparator, reference source and clock on the same chip.
The high linearity makes it very suitable for signal processing while the accurate, temperature-compensated reference source makes it applicable for instrumentation purposes.
The ADC accepts unipolar or bipolar input signals. Digital output data is in serial form.
All digital outputs are fully TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 5)	-	5	-	V
$-V_{N1}$	negative supply voltage 1 (pin 6)	-	5	-	V
$-V_{N2}$	negative supply voltage 2 (pin 9)	-	17	-	V
THD	total harmonic distortion including noise	-	−84	-	dB
S/N	signal-to-noise ratio	-	86	-	dB
ILE	integral linearity error	-	±1/2	-	LSB
P_{tot}	total power dissipation	-	500	-	mW
T_{amb}	operating ambient temperature range	−20	-	+70	°C
I_{FS}	full scale input current	-	4	-	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1534	28	DIL28	plastic	SOT117

14-bit analog-to-digital converter (ADC) TDA1534

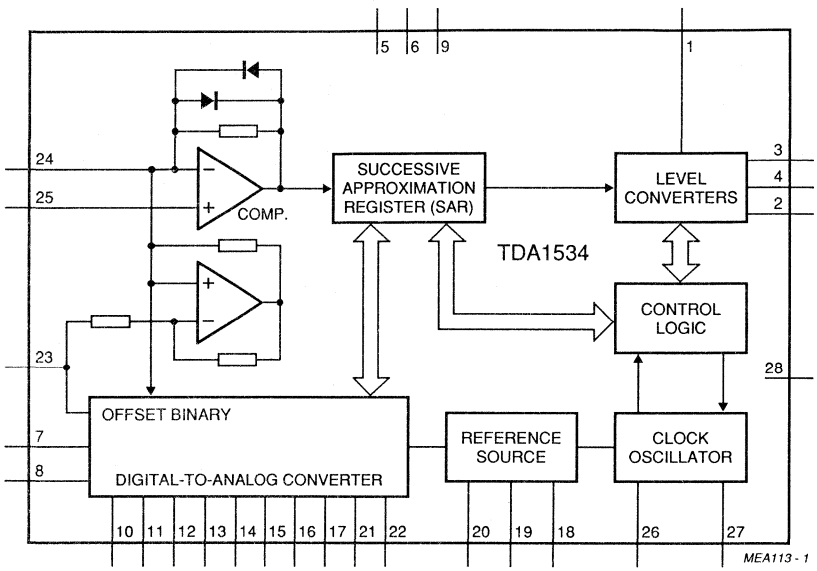


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SC	1	start conversion
SO	2	status out
DO	3	data out
DS	4	data strobe
V_P	5	positive supply voltage
V_{N1}	6	negative supply voltage 1
OSC DAC	7,8	DEM oscillator DAC
V_{N2}	9	negative supply voltage 2
DECOU	10 to 17	decoupling DEM current sources
I_{ref1}	18	I_{ref1}
I_{ref2}	19	I_{ref2}
I_{ref3}	20	I_{ref3}
DECOU	21,22	decoupling DEM current sources
OBI	23	offset binary input
AI	24	analog signal input
GND(A)	25	analog ground
COSC	26,27	oscillator system clock
GND(D)	28	digital ground

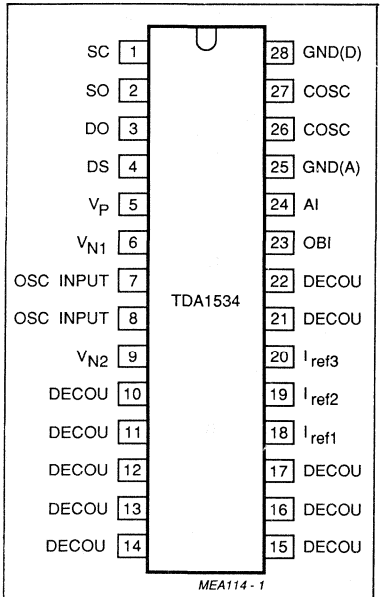


Fig.2 Pinning configuration.

FUNCTIONAL DESCRIPTION

The circuit consists of the following parts:

14-bit digital-to-analog converter (DAC)

Using "dynamic element matching", which results in high accuracy, linearity and long term stability, without the need of trimming. The main parts of the DAC are the dynamic element matching (DEM) circuitry and the bit switches. The DAC also delivers an offset binary current for bipolar operation of the ADC.

Fast settling comparator/substractor

Consisting of a high speed, clamped operational amplifier with special frequency compensation system.

Successive approximation register (SAR)

This register is an array of fourteen addressable latches, with the outputs connected to the bit switches of the DAC.

Logic-level converters

Converting the internally used current-mode-logic (CML) levels to TTL levels, for easy interface of the ADC with standard logic families.

Clock oscillator and control logic

Delivering the pulses and timing for the SAR and takes care of the communication with the peripheral circuits.

Reference source

Based on the bandgap voltage of silicon, with extra temperature compensation circuit.

For the timing of the output signals see Fig.3. At the leading edge of the start conversion (SC) pulse the ADC starts converting the input voltage. During the conversion cycle the following signals appear at the output pins:

Status (pin 2)

This signal can be used to force the Sample-and-Hold-Circuit, in front of the ADC, in hold mode.

Data strobe (pin 4)

This signal is used to clock the data-out signal into the peripheral devices.

Data out (pin 3)

The 14 bits serial, binary, output code of the ADC starting with the most significant bit (MSB). The data must be considered valid at the trailing edge of the data-strobe signal.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage (pin 5)	0	7	V
$-V_{N1}$	negative supply voltage 1 (pin 6)	0	7	V
$-V_{N2}$	negative supply voltage 2 (pin 9)	0	20	V
T_{stg}	storage temperature range	−65	+150	°C
T_{amb}	operating ambient temperature	−20	+70	°C
V_{es}	electrostatic handling*	−1000	+1000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	110	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS (see application circuit Figs 5a and 5b)

V_P = 5 V; $-V_{N1}$ = 5 V; $-V_{N2}$ = 17 V; T_{amb} = +25 °C, unless otherwisse specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 5)		4	5	6	V
$-V_{N1}$	negative supply voltage 1 (pin 6)		4	5	6	V
$-V_{N2}$	negative supply voltage 2 (pin 9)		16.5	17	18	V
I_P	positive supply current		-	30	40	mA
$-I_{N1}$	negative supply current		-	37	45	mA
$-I_{N2}$	negative supply current		-	10	13	mA
P_{tot}	total power dissipation		-	500	-	mW
	resolution		-	14	-	bits
Analog input						
I_{FS}	full scale input current	offset-binary current switched off	3.8	4.0	4.2	mA
TC_{IFS}	temperature coefficient	pin 23 short-circuited to ground; note 1	-	30	-	10^{-6}/K
Zero-offset						
$-V_o$	offset voltage	offset-binary current switched off	-	20	30	mV
TC_{Vo}	temperature coefficient		-	4	-	V/K
$-I_o$	offset current		-	500	2000	nA
TC	temperature coefficient		-	1.5	-	nA/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Linearity						
$\|DLE\|$	linearity error (differential)		0	-	0.9	LSB
$\|ILE\|$	linearity error (integral)		0	0.25	0.9	LSB
$\|ILE_T\|$	linearity error	T_{amb} = −20 to +70 °C	0	0.5	-	LSB
I_{BO}	offset binary current		$0.45I_{FS}$	$0.50I_{FS}$	$0.55I_{FS}$	mA
TC_{IBO}	temperature coefficient	note 1	-	30	-	10^{-6}/K
Distortion						
THD	total harmonic distortion including noise		-	−84	-	dB
S/N	signal-to-noise ratio	note 2	-	86	-	dB
Start conversion (pin 1)						
input voltages						
V_{IL}	input voltage LOW	$-I_{IL}$ < 1.6 mA	0	-	0.8	V
V_{IH}	input voltage HIGH	I_{IH} < 40 µA	2	-	5	V
input currents						
$-I_{IL}$	input current LOW	V_{IL} < 0.8 V	-	-	1.6	mA
I_{IH}	input current HIGH	V_{IH} > 2 V	-	-	40	µA
Data, strobe, status (pins 3,4 and 2)						
output voltages						
V_{OL}	output voltage LOW	$I_{OL} \leq$ 6.4 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	$-I_{OH}$ < 160 µA	2.4	-	5	V
output currents						
I_{OL}	output current LOW	$V_{OL} \leq$ 0.6 V	-	1.6	1.6	mA
$-I_{OH}$	output current HIGH	$-V_{OH} \geq$ 2.4 V	-	400	400	µA
Timing						
f_{clock}	oscillator clock (pin 26 and 27)		-	3.5	-	MHz
t_c	conversion time determined by C_{26-27}	note 3	6.5	0.042 x C (in pF)	-	µs
t_{sc}	signal width (pin 1)	start conversion	0.2	-	t_c	µs
t_{PDSH}	status delay time HIGH (pin 2)		-	60	200	ns
t_{PDDS}	data strobe delay time		-	900	1100	ns
t_{DSH}	pulse duration (pin 4)	data strobe HIGH	-	125	-	ns
t_{DSL}	pulse duration (pin 4)	data strobe LOW	-	435	-	ns
t_{DS}	set-up time (pin 3)	data out	-	25	350	ns
t_{PDSL}	status delay time LOW (pin 2)		-	200	350	ns
$f_{osc\ x\ DAC}$	oscillator DAC (pins 7 and 8)		100	160	200	kHz

Notes to the characteristics

1. I_{FS} and I_{BO} track with each other over temperature range.
2. Signal-to-noise ratio within 10 Hz and 20 kHz bandwidth of a 1 kHz full scale sinewave, generated at a sample rate of 44.1 kHz.
3. Minimum value is 150 pF and value used with testing is 820 pF. See Fig.4.

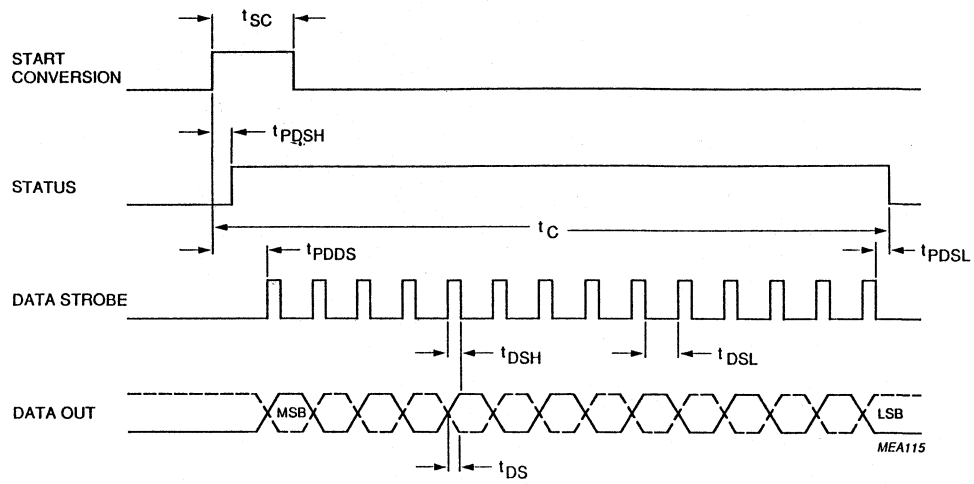


Fig.3 Timing diagram.

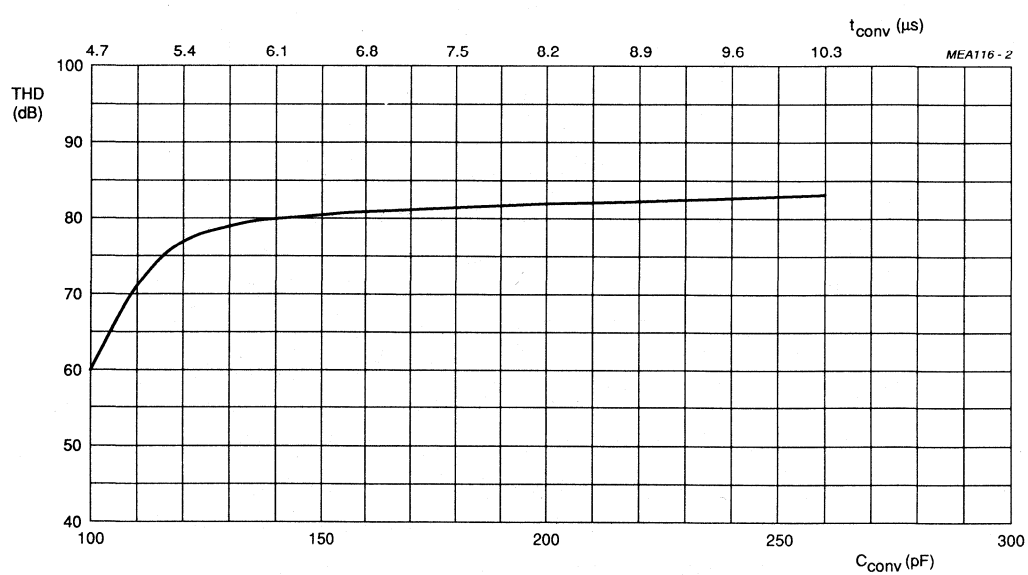


Fig.4 Distortion as a function of conversion time.

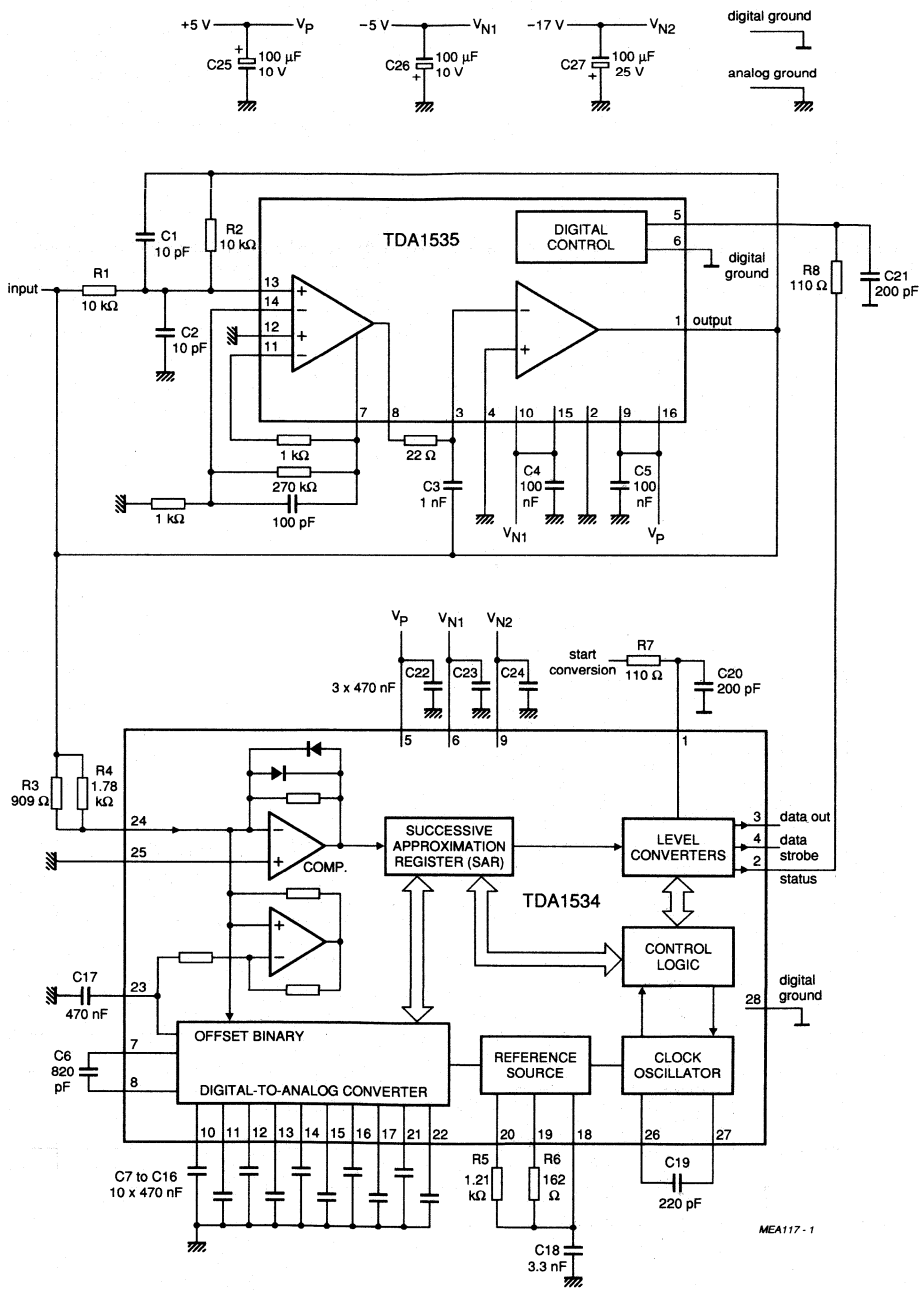


Fig.5a Application diagram.

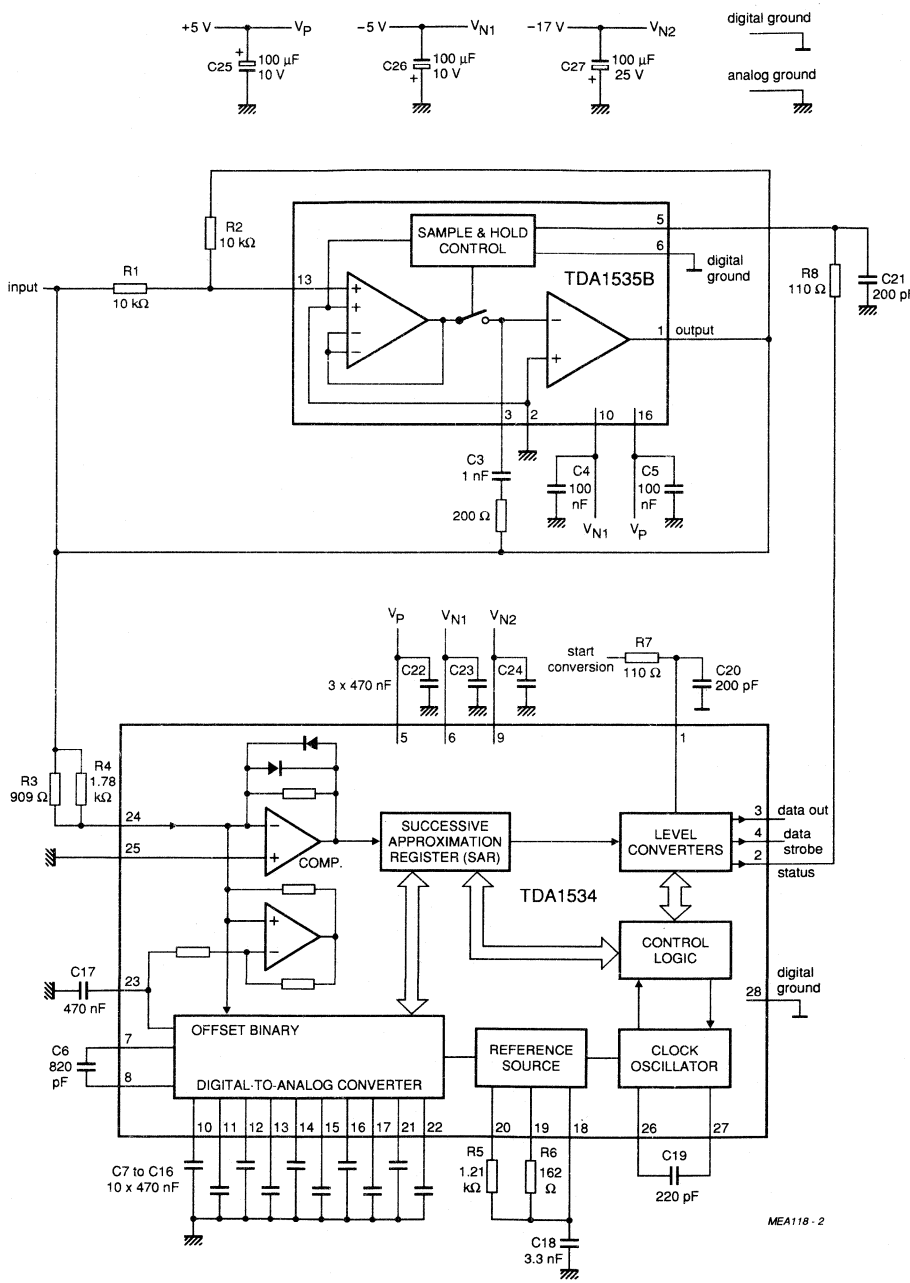


Fig.5b Basic evaluation circuit.

High-speed single sample-and-hold amplifier

TDA1535B

GENERAL DESCRIPTION

The TDA1535B is a high-speed sample-and-hold amplifier with a total harmonic distortion of 0.001%, and a very high signal-to-noise ratio.

The excellent performance of the circuit makes it suitable for data acquisition systems with resolution up to 16 bits. The control input is TTL compatible.

FEATURES

- High-speed: fast acquisition, hold-mode settling and aperture time
- Small sample-to-hold offset step, low droop rate
- Low noise: low total harmonic distortion and high signal-to-noise ratio
- Control circuit with TTL input.

FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained using the application diagram (Fig.3). The circuit is a single Sample-and-Hold circuit. The several parts of the diagram will be described in the next sections.

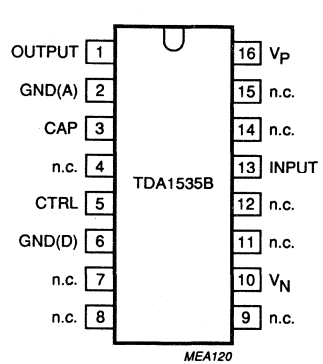


Fig.1 Pinning diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage	4.5	5.0	5.5	V
V_N	negative supply voltage	−5.5	−5.0	−4.5	V
THD	total harmonic distortion	–	−100	–	dB
		–	0.001	–	%
S/N	signal-to-noise ratio	–	110	–	dB
t_{ac}	acquisition time to 0.001% (8 V step)	–	2	–	µs
t_{av}	aperture uncertainty	–	0.1	–	ns
B	small signal bandwidth	–	2	–	MHz
V_{SHO}	sample-to-hold offset step	–	2	–	mV
dV/dt	droop rate	–	40	–	mV/s
t_{se}	hold-mode settling time	–	1	–	µs
P_{tot}	total power dissipation	–	225	–	mW
T_{amb}	operating ambient temperature range	−30	–	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1535B	16	DIL	plastic	SOT38

PINNING

SYMBOL	PIN	DESCRIPTION
OUTPUT	1	output
GND(A)	2	analog ground
CAP	3	S/H capacitor
n.c.	4	not connected
CTRL	5	S/H control
GND(D)	6	digital ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
V_N	10	negative supply voltage
n.c.	11	not connected
n.c.	12	not connected
INPUT	13	input
n.c.	14	not connected
n.c.	15	not connected
V_p	16	positive supply voltage

Supply block

The circuit must be supplied by a dual supply voltage. Nominally the supply voltages are plus and minus 5 V. This supply voltage is needed for a rated output voltage of 8 Vtt, but the circuit will also operate at lower supply voltages. Furthermore separate 'grounds' for analog and digital signals are used. The supply circuit consists of a current source circuit which contains separate sources for the voltage follower, and the hold amplifier to prevent feedthrough in the hold condition. The supply acts as a current source, so the current consumption is almost independent of the supply voltage resulting in a good supply ripple rejection.

Voltage follower amplifier

The voltage follower amplifier is an operational amplifier in voltage follower configuration. It contains two PMOS input stages controlled by the S/H switch, one input stage for the track mode, the other for the hold mode. The input stage that is used in the hold mode has it's + input connected to the analog ground forcing the output to analog ground too. In this way, feedthrough of the input signal is prevented in the hold mode.

Hold switch

The hold switch is a large NMOS transistor with an on-resistance of 50 Ω. In order to reduce the charge transfer of the digital signal into the analog path, two short-circuited NMOS transistors, with the inverse, digital signal on their gate, are added on both sides of the switching transistor.

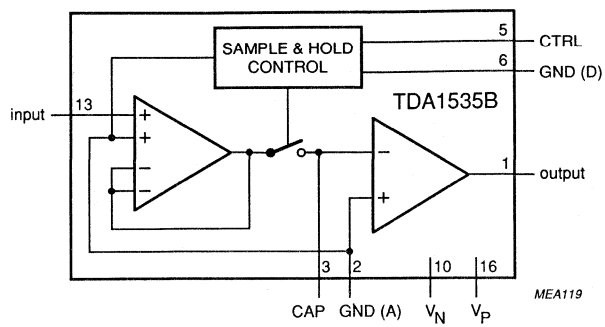


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	6	V
V_N	negative supply voltage		–6	–	V
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		–30	+85	°C
V_{es}	electrostatic handling	see note 1	–2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient	75	K/W

Hold amplifier

The hold amplifier is an operational amplifier similar to the voltage follower amplifier. The PMOS transistors of the input stage are very useful for a hold amplifier because of the very low input-current, resulting in a low droop rate and a low input current noise. The tail current and the W/L of the PMOS input transistors are chosen in such a way that a very good noise performance is achieved. The input stage is followed by a voltage gain stage. This stage is optimized for linearity and output voltage swing. The usual linearity problems, caused by the non-linearity of the current source load, are prevented by the use of a special PMOS cascoded current source. In this way linearity improves with more than 20 dB thus offering distortion figures in the track mode lower than - 100 dB for input frequencies up to 20 kHz and output voltages up to 8 Vtt.

Sample-and-hold control

The sample-and-hold control input is a TTL compatible input. The signal on this input controls the switches mentioned in the above sections in the correct timing order. The supply is taken from the 'V_p' pin via an on-chip separate supply line.

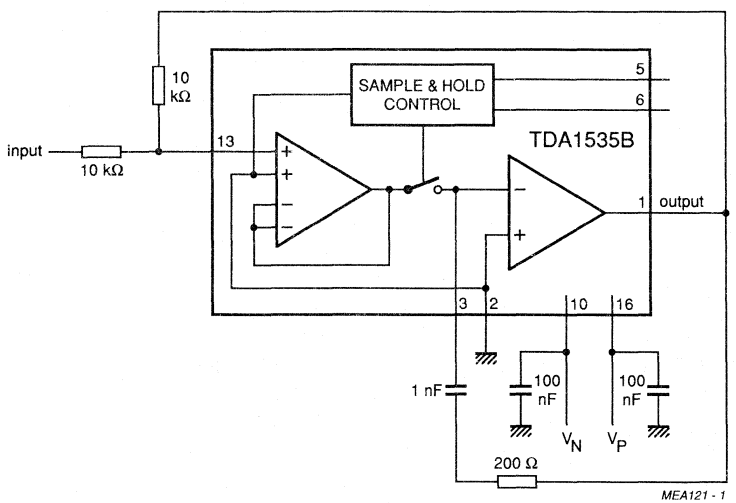


Fig.3 Test and application diagram.

CHARACTERISTICS

V_P = +5 V; T_{amb} = +25 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage		4.5	5.0	5.5	V
V_N	negative supply voltage		−5.5	−5.0	−4.5	V
I_P	positive supply current		–	22	–	mA
I_N	negative supply current		–	−23	–	mA
P_{tot}	total power dissipation		–	225	–	mW
Input/Output						
A_v	gain	note 2	–	−1	–	V/V
V_i	input voltage (RMS value)		–	–	2.82	V
Sample mode						
THD	total harmonic distortion	notes 1,2,3	–	−100	–	dB
SNR	S/N ratio	notes 1,2,3	–	110	–	dB
B	small signal band width		–	2	–	MHz
Sample/hold mode						
t_{ad}	aperture delay time	see Fig.4	–	100	–	ns
t_{av}	aperture uncertainly (RMS)	see Fig.4	0	0.1	0.2	ns
V_{SHO}	sample-to-hold (pedestal)	see Fig.4	–	2	–	mV
dV/dt	offset step droop rate	see Fig.4	–	40	–	mV/s
t_{ac}	acquisition time to 0.001%	see Fig.4	–	2	–	µs
t_{se}	hold-mode settling time	see Fig.4	–	1	–	µs
THDF	total harmonic distortion functional	notes 1,4	–	−100	−96	dB
Supply voltage ripple rejection						
SVRR		note 5	–	80	–	dB
SVRR		note 5	55	80	–	dB
Digital inputs						
V_{IH}	digital input voltage, hold mode (logic 1)		2	–	V_p	V
I_{IH}	digital input current, sample mode	V_{IH} = 2.4 V	–	–	20	µA
V_{IL}	digital input voltage, sample mode (logic 0)		0	–	0.8	V
I_{IL}	digital input current, hold mode	V_{IL} = 0.4 V	−400	–	–	µA

Notes

1. Over audio band (20 Hz to 20 kHz).
2. In sampling mode.
3. At maximum input signal.
4. Distortion of sampled signal at a sample frequency of 50 kHz.
5. The ripple rejection is measured at the output of the hold amplifier; amplitude = 0.5 Vtt. f = 100 Hz to 10 kHz.

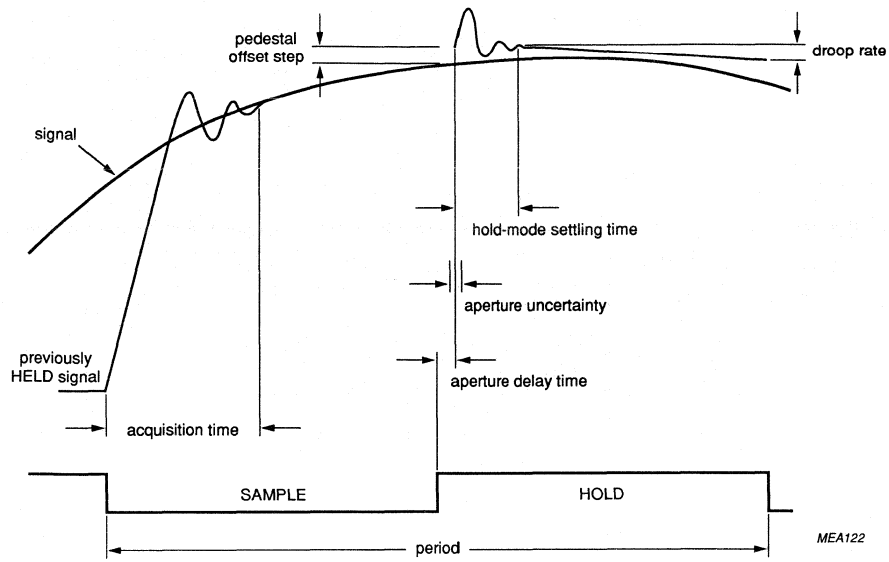


Fig.4 Sample/hold timing characteristics (not to scale).

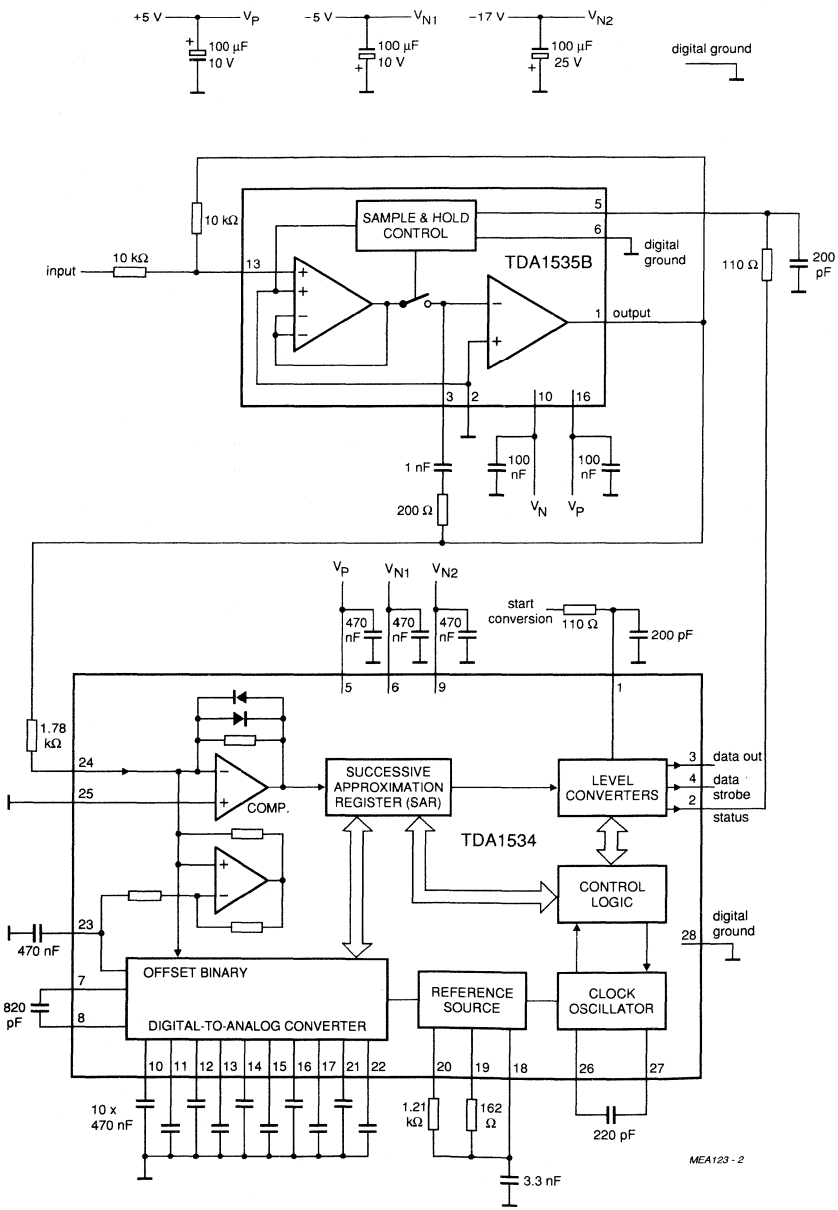


Fig.5 Application diagram of TDA1535B in combination with TDA1534.

High-speed stereo sample-and-hold amplifier

TDA1537

GENERAL DESCRIPTION

The TDA1537 is a high-speed stereo sample-and-hold amplifier with a total harmonic distortion of 0.001%, and a very high signal-to-noise ratio.

The excellent performance of the circuit makes it suitable for data acquisition systems with a resolution up to 16 bits, such as hi-fi digital audio equipment. The control input is TTL compatible.

FEATURES

- Low noise: low total harmonic distortion and high signal-to-noise ratio
- High-speed: fast acquisition time, hold-mode settling and aperture time
- Small sample-to-hold offset step, low droop rate
- Control circuit with TTL input.

FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained using the application diagram (Fig.3). The circuit is a stereo Sample-and-hold circuit. The several parts of the diagram will be described in the next sections.

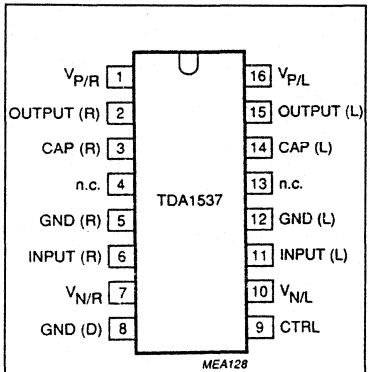


Fig.1 Pinning diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{P/R}$, $V_{P/L}$	positive supply voltage	4.5	5.0	5.5	V
$V_{N/R}$, $V_{N/L}$	negative supply voltage	−5.5	−5.0	−4.5	V
THD	total harmonic distortion	–	−100	–	dB
		–	0.001	–	%
S/N	signal-to-noise ratio	–	110	–	dB
t_{ac}	acquisition time to 0.001% (8 V step)	–	2	–	µs
t_{av}	aperture uncertainty	–	0.1	–	ns
B	small signal bandwidth	–	2	–	MHz
V_{SHO}	sample-to-hold offset step	–	2	–	mV
dV/dt	droop rate	–	40	–	mV/s
t_{se}	hold-mode settling time	–	1	–	µs
P_{tot}	total power dissipation	–	455	–	mW
T_{amb}	operating ambient temperature range	−30	–	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1537	16	DIL	plastic	SOT38

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{P/R}$	1	VP (right)
OUTPUT (R)	2	output (right)
CAP (R)	3	S/H capacitor (right)
n.c.	4	not connected
GND (R)	5	ground (right)
INPUT (R)	6	input (right)
$V_{N/R}$	7	VN (right)
GND (D)	8	digital ground
CTRL	9	S/H control input
$V_{N/L}$	10	VN (left)
INPUT (L)	11	input (left)
GND (L)	12	ground (left)
n.c.	13	not connected
CAP (L)	14	S/H capacitor (left)
OUTPUT (L)	15	output (left)

Supply block

The circuit must be supplied by a dual supply voltage. Nominally the supply voltages are plus and minus 5 V. This supply voltage is needed for a rated output voltage of 8 Vtt, but the circuit will also operate at lower supply voltages. Furthermore separate 'grounds' for analog and digital signals are used. The supply circuit consists of two separate PTAT current source circuits, for 'left' and the 'right' S/H circuit. In this way a channel separation of more than 100 dB is realized. Each PTAT current source circuit contains separate sources for the voltage follower, and the hold amplifier to prevent feedthrough in the hold condition. The supply acts as a current source, so the current consumption is almost independent of the supply voltage resulting in a good supply ripple rejection.

Voltage follower amplifier

The voltage follower amplifier is an operational amplifier in voltage follower configuration. It contains two PMOS input stages controlled by the S/H switch, one input stage for the track mode, the other for the hold mode. The input stage that is used in the hold mode has it's + input connected to the analog ground forcing the output to analog ground too. In this way, feedthrough of the input signal is prevented in the hold mode.

Hold switch

The hold switch is a large NMOS transistor with an on-resistance of 50 Ω. In order to reduce the charge transfer of the digital signal into the analog path, two short-circuited NMOS transistors, with the inverse, digital signal on their gate, are added on both sides of the switching transistor.

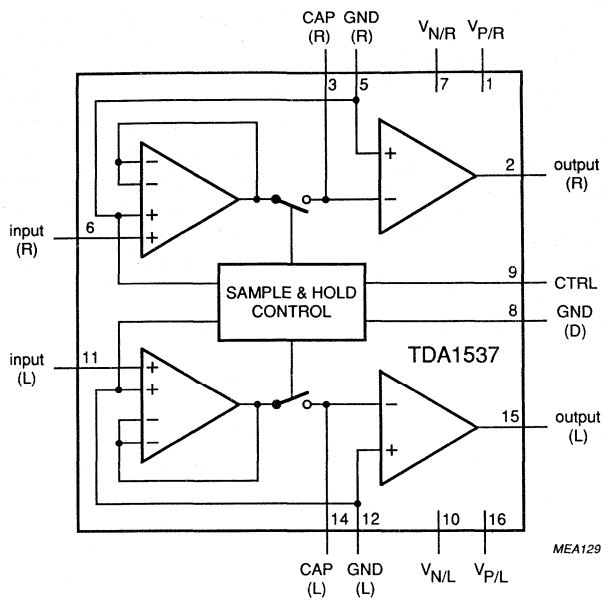


Fig.2 Block diagram.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{P/R}$, $V_{P/L}$	positive supply voltage		–	6	V
$V_{N/R}$, $V_{N/L}$	negative supply voltage		–6	–	V
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		–30	+85	°C
V_{es}	electrostatic handling	see note 1	–2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient	75	K/W

High-speed stereo sample-and-hold amplifier

TDA1537

Hold amplifier

The hold amplifier is an operational amplifier similar to the voltage follower amplifier. The PMOS transistors of the input stage are very useful for a hold amplifier because of the very low input-current, resulting in a low droop rate and a low input current noise. The tail current and the W/L of the PMOS input transistors are chosen in such a way that a very good noise performance is achieved. The input stage is followed by a voltage gain stage. This stage is optimized for linearity and output voltage swing. The usual linearity problems, caused by the non-linearity of the current source load, are prevented by the use of a special PMOS cascoded current source. In this way linearity improves with more than 20 dB thus offering distortion figures in the track mode lower than - 100 dB for input frequencies up to 20 kHz and output voltages up to 8 Vtt.

Sample-and-hold control

The sample-and-hold control input is a TTL compatible input. The signal on this input controls the switches mentioned into above sections in the correct timing order. The supply is taken from the 'V_p left' pin via an on-chip separate supply line.

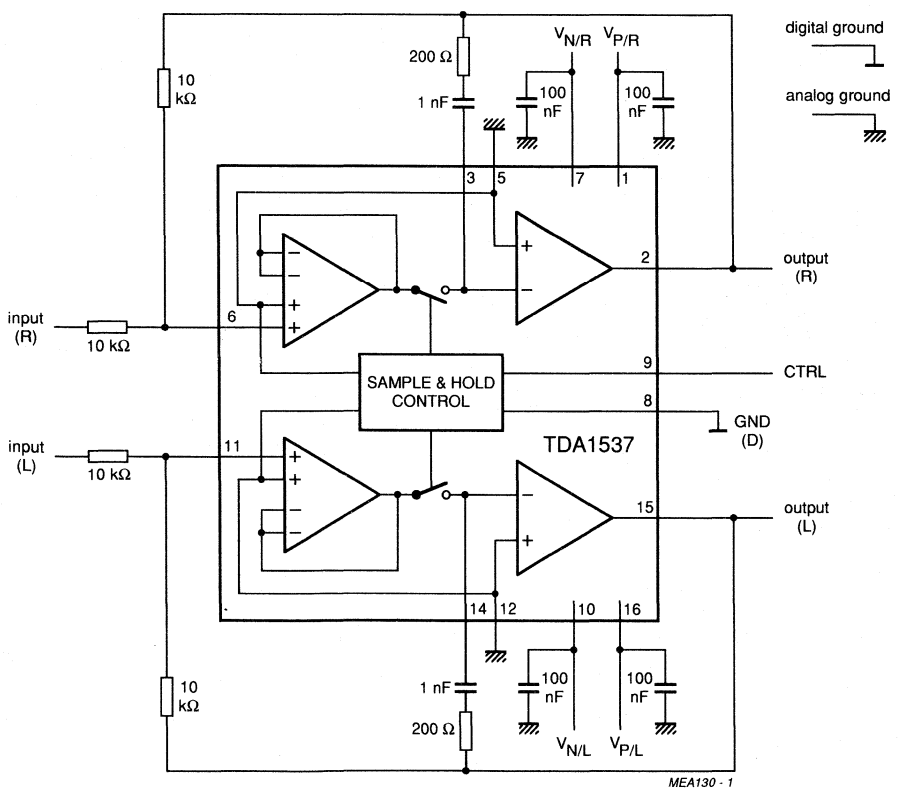


Fig.3 Test and application diagram.

CHARACTERISTICS

$V_{P/R}$, $V_{P/L}$ = +5 V; $V_{N/R}$, $V_{N/L}$ = −5 V; T_{amb} = +25 °C; f = 1 kHz, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{P/R}$, $V_{P/L}$	positive supply voltage		4.5	5.0	5.5	V
$V_{N/R}$, $V_{N/L}$	negative supply voltage		−5.5	−5.0	−4.5	V
I_P	positive supply current		–	45	–	mA
I_N	negative supply current		–	−46	–	mA
P_{tot}	total power dissipation		–	455	–	mW
Input/Output						
A_v	gain	note 2	–	−1	–	V/V
V_i	input voltage (RMS value)		–	–	2.82	V
Sample mode						
THD	total harmonic distortion	notes 1,2,3	–	−100	–	dB
SNR	S/N ratio	notes 1,2,3	–	110	–	dB
B	small signal band width		–	2	–	MHz
Sample/hold mode						
t_{ad}	aperture delay time	see Fig.4	–	100	–	ns
t_{av}	aperture uncertainly (RMS)	see Fig.4	0	0.1	0.2	ns
V_{SHO}	sample-to-hold (pedestal)	see Fig.4	–	2	–	mV
dV/dt	offset step droop rate	see Fig.4	–	40	–	mV/s
t_{ac}	acquisition time to 0.001%	see Fig.4	–	2	–	µs
t_{se}	hold-mode settling time	see Fig.4	–	1	–	µs
THDF	total harmonic distortion functional	notes 1,4	–	−100	−96	dB
Supply voltage ripple rejection						
SVRR		note 5	–	80	–	dB
SVRR		note 5	55	80	–	dB
Digital inputs						
V_{IH}	digital input voltage, hold mode (logic 1)		2	–	V_p	V
I_{IH}	digital input current, sample mode	V_{IH} = 2.4 V	–	–	20	µA
V_{IL}	digital input voltage, sample mode (logic 0)		0	–	0.8	V
I_{IL}	digital input current, hold mode	V_{IL} = 0.4 V	−400	–	–	µA

Notes

1. Over audio band (20 Hz to 20 kHz).
2. In sampling mode.
3. At maximum input signal.
4. Distortion of sampled signal at a sample frequency of 50 kHz.
5. The ripple rejection is measured at the output of the hold amplifier;amplitude = 0.5 Vtt. f = 100 Hz to 10 kHz.

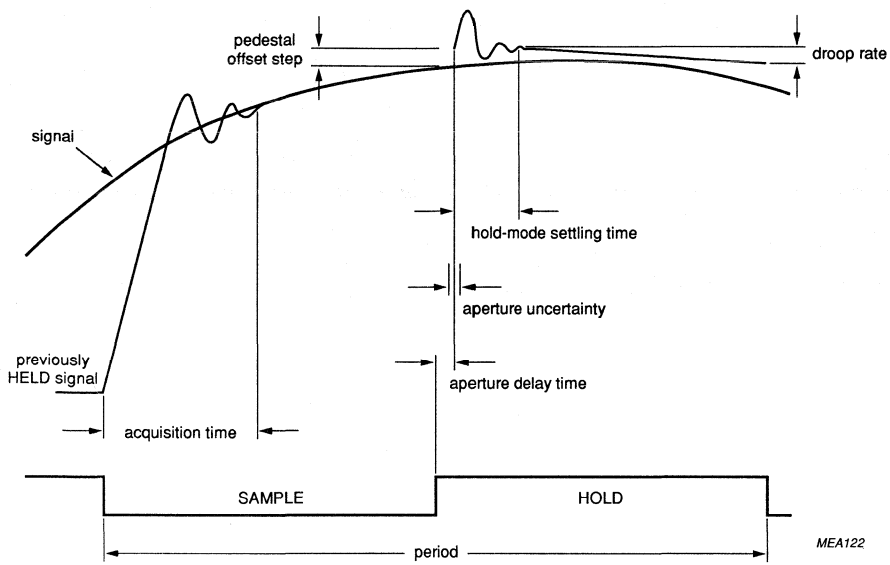


Fig.4 Sample/hold timing characteristics (not to scale).

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA1541A

Stereo high performance 16-bit DAC

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- High sound quality
- High performance: low noise and distortion, wide dynamic range
- 4 x or 8 x oversampling possible
- Selectable two-channel input format
- TTL compatible inputs

GENERAL DESCRIPTION

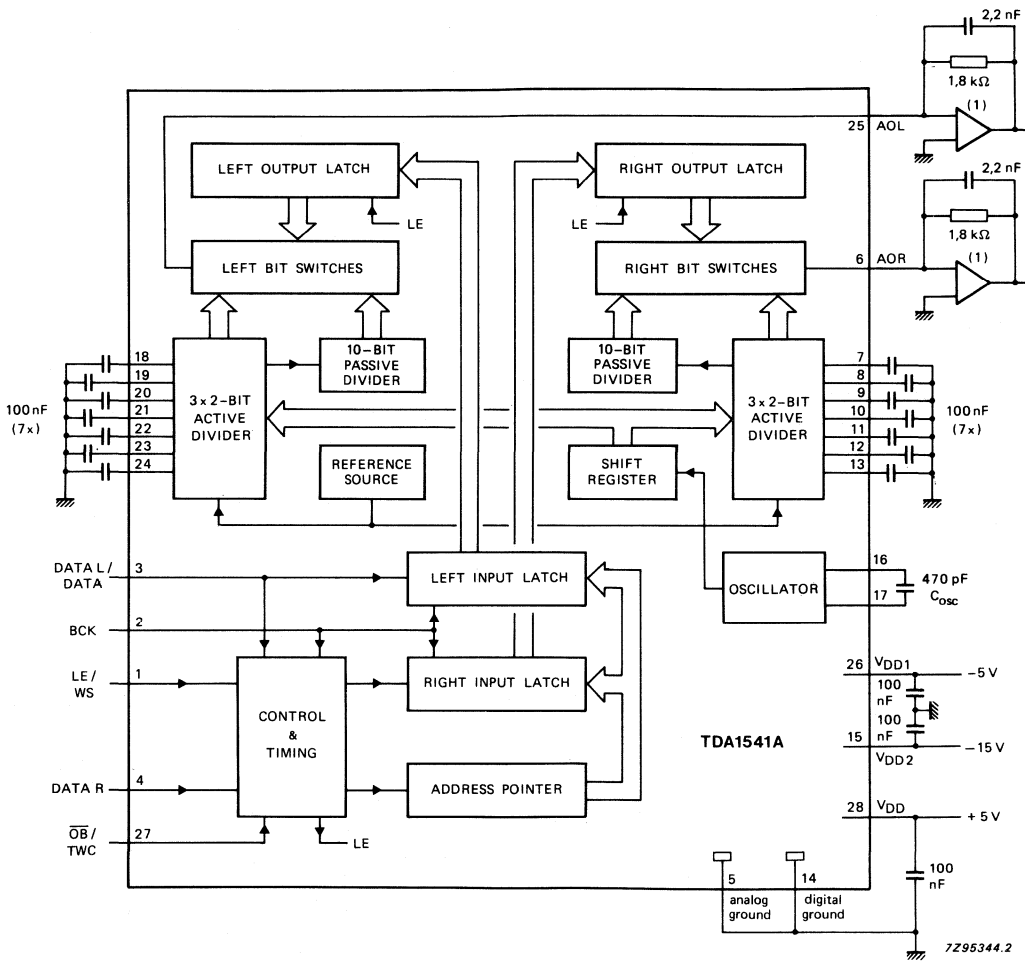
The TDA1541A is a stereo 16-bit digital-to-analog converter (DAC). The ingenious design of the electronic circuit guarantees a high performance and superior sound quality. The TDA1541A is therefore extremely suitable for use in top-end high-fi digital audio equipment such as high quality Compact Disc players or digital amplifiers.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1541A	28	DIL	plastic	SOT117

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
THD	total harmonic distortion	including noise	-	−95	−90	dB
		at 0 dB	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise	-	−42	-	dB
		at −60 dB	-	0.79	-	%
NL	non-linearity	at T_{amb} = −20 to +85 °C	-	0.5	1.0	LSB
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input; (pin 3 and 4)		-	-	6.4	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	6.4	MHz
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 200 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−40	-	+85	°C
P_{tot}	total power dissipation		-	700	-	mW



(1) TDA1542
(2) 2 x NE5534 or equivalent

Fig.1 Block diagram.

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543

Dual 16-bit DAC (economy version) (I^2S input format)

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1543 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in TV sets and in digital amplifiers.

ORDERING INFORMATION

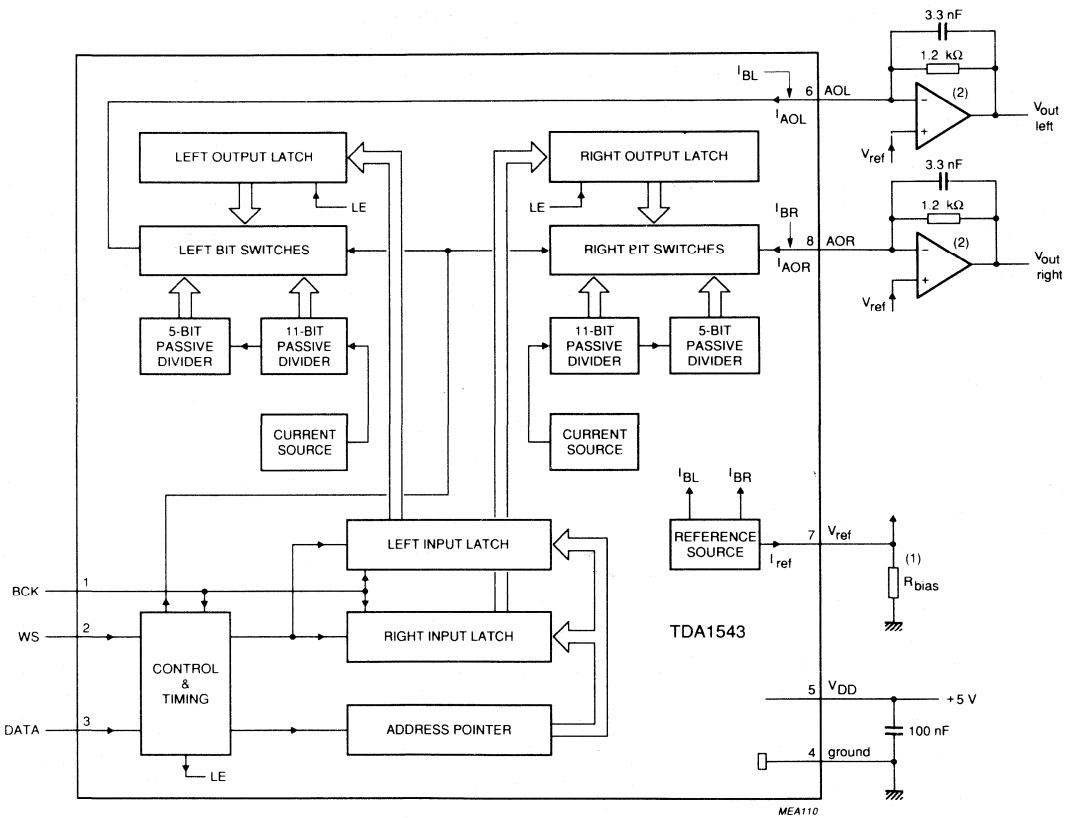
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543	8	DIL	plastic	SOT97
TDA1543T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−30	−23	dB
		at −60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543A

Dual 16-bit DAC (economy version) (Japanese input format)

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- Japanese input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1543A is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders and in digital amplifiers.

ORDERING INFORMATION

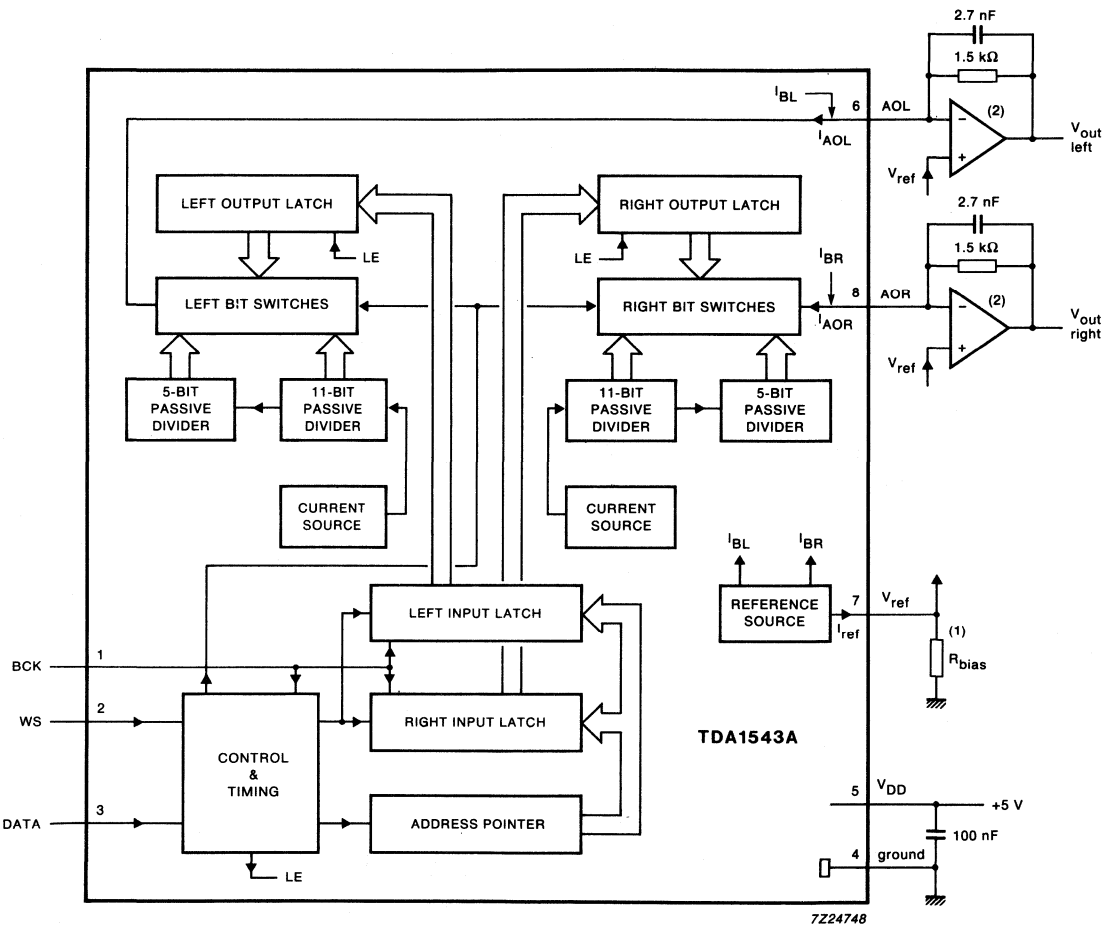
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543A	8	DIL	plastic	SOT97
TDA1543AT	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−30	−23	dB
		at −60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543(A)/S6

Dual 16-bit low-cost economy DAC (relaxed version of TDA1543A)

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

GENERAL DESCRIPTION

The TDA1543(A)/S6 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as a low-cost economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in television systems and digital amplifiers.

The S6 version is a relaxed version of the TDA1543(A). The differences in performance between the S6 selection and the standard version are limited to only three parameters:

QUICK REFERENCE VALUES STANDARD VERSION

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB	-	–70	dB
T_{amb}	operating ambient temperature range		–30	+85	°C
AI_{bias}	bias current gain		1.9	2.1	

QUICK REFERENCE VALUES S6 VERSION

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB	-	–60	dB
T_{amb}	operating ambient temperature range		–20	+75	°C
AI_{bias}	bias current gain		1.85	2.1	

The other characteristics of the S6 version can be found in the data sheets of the TDA1543 and the TDA1543A.

Data sheet	
status	Objective specification
date of issue	February 1991

TDA1544

Dual 16-bit low-noise DAC

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- 16-bit resolution and 4 x oversampling
- High performance: low distortion, wide dynamic range and high signal-to-noise ratio
- Single 5 V power supply
- No external components required
- Adjustable bias current
- Japanese-input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1544 is a dual 16-bit digital-to-analog converter (DAC) and is designed for use in hi-fi digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1544	8	DIL	plastic	SOT97
TDA1544T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		2.7	3.0	3.3	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−33	−23	dB
		at −60 dB	-	2.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio		99	101	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

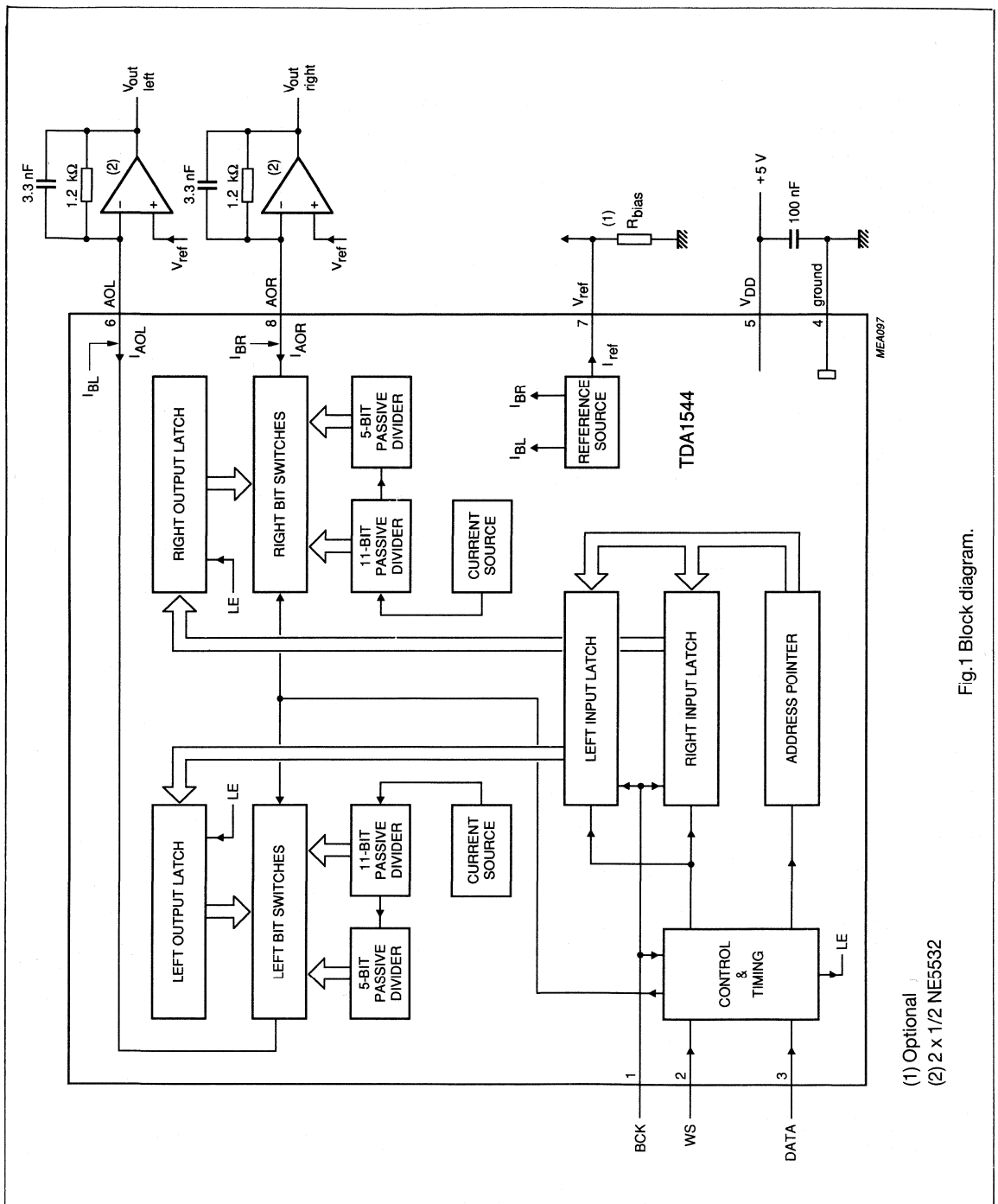


Fig.1 Block diagram.

(1) Optional
(2) 2 x 1/2 NE5532

PAL – NTSC ENCODER

GENERAL DESCRIPTION

The TDA2501 encodes two colour-difference signals R-Y and B-Y onto one subcarrier. Quadrature modulation allows the coding to be in accordance with either the PAL or NTSC system.

Features

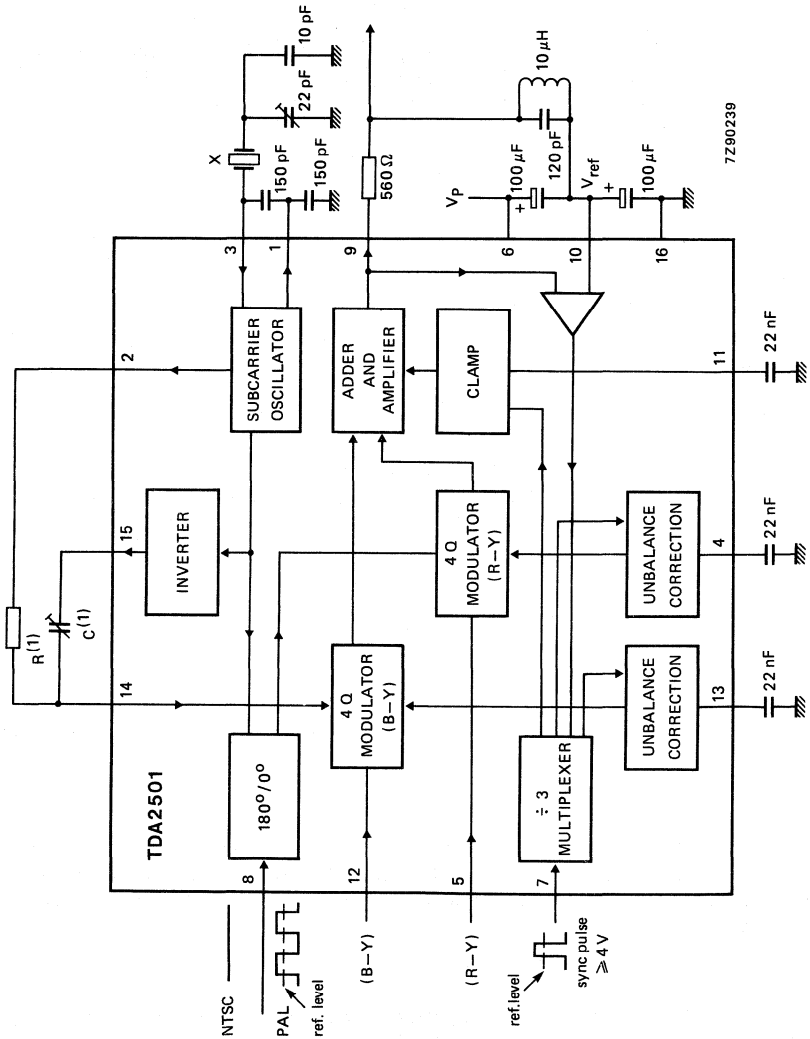
- Generates two sinusoidal subcarriers with a relative phase of 90° (also accepts external subcarriers)
- Modulates the two subcarriers with the colour difference signals
- Inverts the output from one modulator on command of an external signal (as in case of PAL)
- Sums the output from the modulators to obtain a quadrature modulated output signal
- Clamps the output DC level to a reference voltage
- Divides the frequency of horizontal sync pulses by three so that the output level can be clamped and the balance of the two modulators sequentially controlled during the line-blanking minus burst-key period

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6)	V_P	5.5	6.8	10	V
Supply current range (pin 6)	I_P	28	40	64	mA
Chrominance output voltage (pin 9) (peak-to-peak value)	$V_{9(p-p)}$	–	–	1.4	V
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINES

TDA2501 : 16-lead DIL; plastic (with internal heat spreader) (SOT38).
TDA2501T: 16-lead mini-pack; plastic (SO16L; SOT162A).



(1) R = 0.885 (2 π fC); for PAL f = 4.433 619 MHz, R = 963 Ω and C = 33 pF.

Fig.1 Block diagram; also test and application diagram.

DESCRIPTION

The colour difference signals B-Y and R-Y with a maximum amplitude of 1.4 volt are to be applied at pin 12 and pin 5. DC-coupling of the input signals is allowed if their DC levels are within specified limits from the DC level at pin 10 (V_{ref}). The following table shows these limits as a function of supply voltage. The table also shows the limits of the reference voltage range as a function of the supply voltage.

supply voltage V_{6-16} (V)	input DC (R-Y) (B-Y) min. (V)*	V_{5-16} V_{12-16} (V) max. (V)**	reference voltage ▲ V_{10-16} (V)		
			min	typ.	max.
5.5	2.4	3.3	2.3	3.0	3.5
6.0	$> V_{ref} - 1.4$ V	3.8	2.4	3.3	3.9
7.0	$> V_{ref} - 1.4$ V	4.8	2.6	4.0	4.7
8.0	$> V_{ref} - 1.4$ V	5.8	2.8	4.8	5.5
9.0	$> V_{ref} - 1.4$ V	6.8	3.0	5.5	6.3
10.0	$> V_{ref} - 1.4$ V	7.8	3.2	6.3	7.1

* Minimum 2.4 V.
** At $V_S - 2.2$ V.
▲ Minimum values at $0.2\ V_S + 1.2$ V.
Typical values without pull-up or pull-down resistor.
Maximum values at $0.8\ V_S - 0.9$ V.

The inputs (B-Y) and (R-Y) should be zero, independent of their (limited) DC-levels, during the line-blanking minus burst-key period (LB – BK). Clamping the output and correcting the out-of-balance of the modulators, is achieved by applying a HIGH level to pin 7 within the (LB–BK) period (e.g. line sync pulse).

Modulation at output:
V_8 = LOW; output = sc x (B-Y) + sc' x (R-Y)
V_8 = HIGH; output = sc x (B-Y) – sc' x (R-Y)
in which sc' = subcarrier
sc = 90° phase-shifted subcarrier to sc' (sc lags).

The bandpass filter at the output suppresses the DC components of the (R-Y) + (B-Y) signal. Luminance (Y) is not processed by this circuit.

Internal subcarrier

The internal subcarrier oscillator is crystal controlled. The oscillator generates a sinewave with low harmonic distortion and an amplitude of about 500 mV peak-to-peak. The amplitude can be changed if necessary with a current input at pin 1. The adjustment range is 0 to 800 mV, with a corresponding current range of +250 to –150 μA.

Phase shift

To obtain a 90° phase-shifted carrier, two low impedance subcarrier outputs are provided, pins 2 and 15, the last being the inverse of the first. Between pins 2 and 15 an external RC combination must be used to obtain the desired 90° shift. The capacitor value must be limited to 33 pF to minimize subcarrier distortion.

The resistor required between pins 2 and 14 is $0.885\ (2\pi\ fC)$.

External subcarrier

The (B-Y) and (R-Y) signals can also be multiplied with an external subcarrier. In this event the external subcarrier is connected to pin 1. For maximum input impedance at pin 1 $V_3 = V_{16}$ ($Z_{mi} > 1400\ \Omega$). The same RC network generates the 90° phase-shifted subcarrier. For the use of an externally generated subcarrier, applied at pin 14, the DC level must be the same as that of an RC-network generated one.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6 to pin 16)	V_P	–	13.2	V
Total power dissipation	P_{tot}	see Fig.2		W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−55	+150	°C

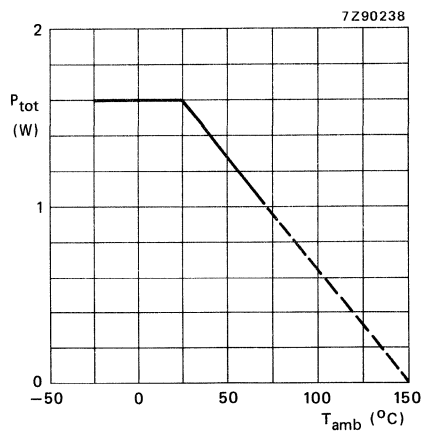


Fig.2 Power derating curve.

CHARACTERISTICS

$V_P = V_{6-10} = -V_{16-10} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Single supply voltage	V_{6-16}	5.5	6.8	10	V
Dual supply voltage					
positive (pin 6)	V_{6-10}	2.0	3.0	5.0	V
negative (pin 16)	$-V_{16-10}$	2.3	3.0	5.0	V
Supply current (pin 10)	I_{10}	−1	0	3.5	mA
positive (pin 6)	I_6	28	40	64	mA
negative (pin 16)	$-I_{16}$	28	40	64	mA
Limitation DC level oscillator feedback	V_1	−30	0	+30	mV
Nominal amplitude input signal (peak-to-peak value)					
pin 5	$V_{5(p-p)}$	–	1	1.4	V
pin 12	$V_{12(p-p)}$	–	1	1.4	V
Input voltages (R-Y) and (B-Y) zero DC level					
pin 5	V_5	2.4	3.3	3.9	V
pin 12	V_{12}	2.4	3.3	3.9	V
Required level of sync input					
HIGH	V_7	4	–	V_P	V
LOW	V_7	–	–	V_{10}	V
Required level of PAL pulse (H/2)					
HIGH	V_8	$V_{10}+0.8$	–	V_P	V
LOW	V_8	$-V_P$	–	0	V
Sync input current $V_7 = V_P + 1$ V	I_7	–	4	15	μA
PAL input current (H/2) $V_8 = V_{10} + 0.8$ V	I_8	–	1.5	5	μA
Chrominance output voltage swing (R-Y) = (B-Y) = 1.4 V; subcarrier pulse = 0.5 V (peak-to-peak value)	$V_{9(p-p)}$	–	–	1.4	V
Amplitude of suppressed subcarrier	V_9	0	7	16	mV
Input currents					
$V_4 = V_{10}$	I_4	0	1.5	5	μA
$V_{11} = V_{10}$	I_{11}	0	1.5	5	μA
$V_{13} = V_{10}$	I_{13}	0	1.5	5	μA
$V_5 = V_{10}$	I_5	0	9	30	μA
$V_{12} = V_{10}$	I_{12}	0	9	30	μA
$V_{14} = V_{16} + 2.3$ V	I_{14}	–	6	–	μA
Input impedance					
(R-Y)	Z_5	–	160	–	kΩ
(B-Y)	Z_{12}	–	160	–	kΩ

SECAM ENCODER

GENERAL DESCRIPTION

The TDA2506/T converts colour-difference signals (D'_R and D'_B) into sequential, frequency modulated signals according to the SECAM system. The signals (D'_R) and (D'_B) are the colour difference signals before low-frequency pre-emphasis; D'_R = -1,9 (R-Y) and D'_B = +1,5(B-Y). The circuit is intended for use in video cameras, games, recorders and players, PAL-SECAM transcoding circuits and SECAM test signal generators.

Synchronizing pulses required for operation of the TDA2506/T may be obtained from a universal sync generator SAA1043 or other pulse generator. All pulses are to be active HIGH and are as follows:

Horizontal sync pulses to pin 11
Half-rate horizontal sync (H/2) pulses to pin 9
Vertical sync pulses to pin 12
Chrominance blanking pulses to pin 13 (may include colour-killer pulses)

Frequency modulation is performed in conjunction with modulator-controller TDA2507.

Features

- Chrominance processor
- Vertical identification signal generator
- Timing pulse output to TDA2507
- Sample and hold circuit for control signal from TDA2507
- No adjustments of external components required (except high-frequency pre-emphasis (bell filter) stage)

QUICK REFERENCE DATA

Supply voltage	V_{4-2}	typ.	5 V
Supply current	I_4	typ.	45 mA
Reference voltage	V_{7-2}, V_{22-24}	typ.	3,5 V
Operating ambient temperature range	T_{amb}	−25 to	+70 °C
Storage temperature range	T_{stg}	−55 to	+150 °C

PACKAGE OUTLINES

TDA2506: 24-lead DIL; plastic (with internal heat spreader) (SOT101B).
TDA2506T: 24-lead mini-pack; plastic (SO24; SOT137A).

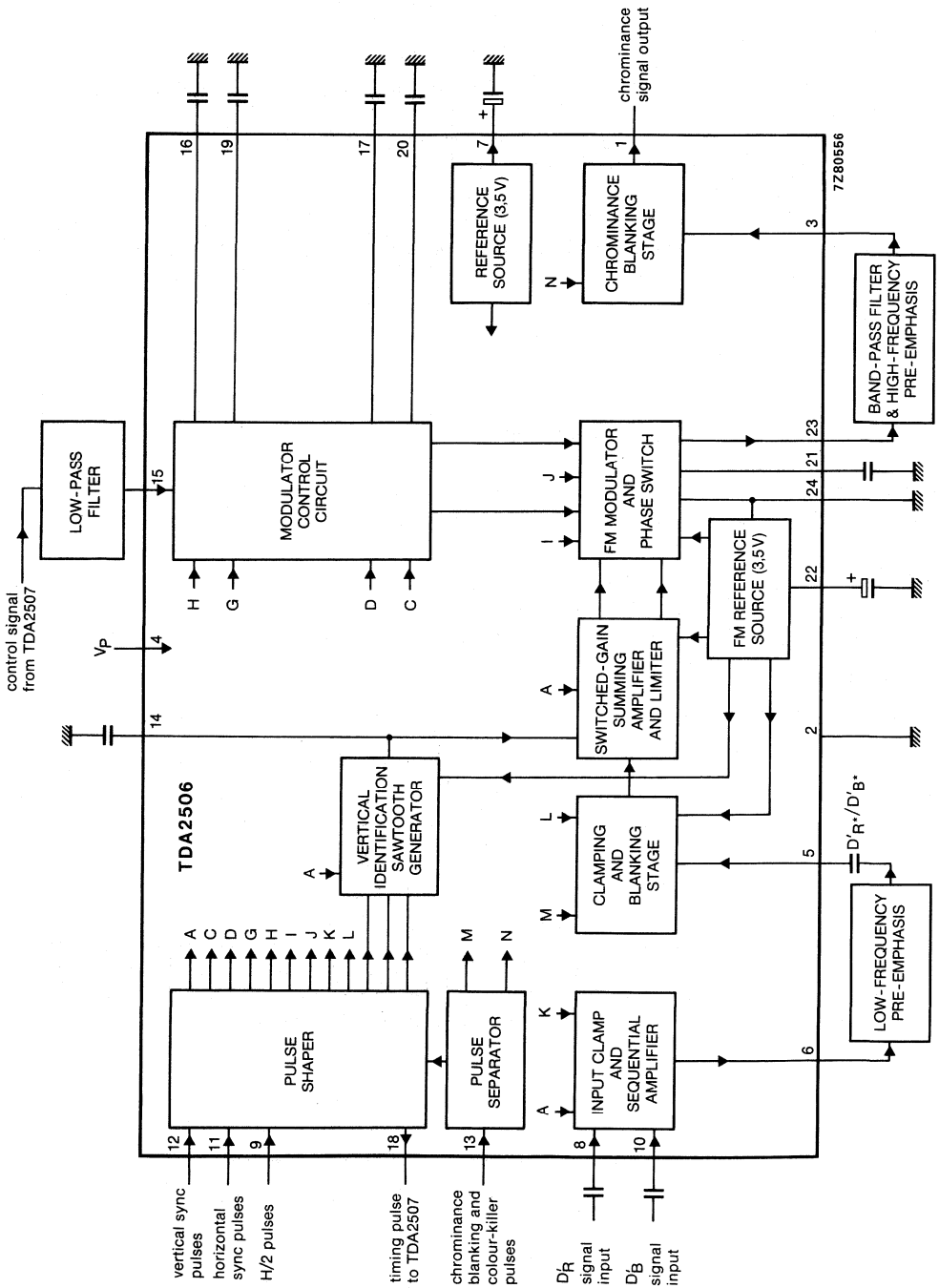


Fig. 1 Block diagram.

Pin functions

1. Chrominance signal output.
2. Ground.
3. Input to chrominance blanking stage from high-frequency pre-emphasis and band-pass filter.
4. Positive supply voltage.
5. Input to clamping and blanking stage from low-frequency pre-emphasis filter.
6. Output from sequential amplifier to low-frequency pre-emphasis filter.
7. Reference voltage output.
8. D'_R signal input.
9. H/2 pulse input (required only if specific phase sequencing is desired; should be connected to ground if not used).
10. D'_B signal input.
11. Horizontal sync pulse input.
12. Vertical sync pulse input.
13. Chrominance blanking and colour-killer pulse input.
14. Capacitor for vertical identification sawtooth.
15. Control signal input from TDA2507 via low-pass filter.
16. 4 406,250 kHz hold capacitor.
17. (R-Y) control.
18. Timing pulse output to TDA2507.
19. 4 250,000 kHz hold capacitor.
20. (B-Y) control.
21. FM modulator tuning capacitor (fixed).
22. FM reference voltage output.
23. FM modulator output to high frequency pre-emphasis and band-pass filter.
24. Ground connection for FM modulator.

FUNCTIONAL DESCRIPTION

Input clamp and sequential amplifier

This circuit clamps the zero levels of the D'_R and D'_B input signals (pins 8 and 10) to the reference voltage from pin 7. The input signals are switched into the amplifier sequentially by an internally delayed H/2 waveform. The amplifier output at pin 6 is D'_R when the delayed H/2 waveform is HIGH and D'_B when it is LOW. The stage gain is 1,5.

Clamping and blanking stage

After external low-frequency pre-emphasis, the sequential $D'_R{}^*$ and $D'_B{}^*$ signals are returned to the IC at pin 5. The signal amplitude at pin 5 is typically 0,5 V (peak-to-peak value) for 75% colour bar (EBU). Black levels are clamped to the FM reference voltage (pin 22). Blanking takes place during the chrominance blanking pulse and, if required, during the video blanking and/or colour killing pulses.

FUNCTIONAL DESCRIPTION (continued)

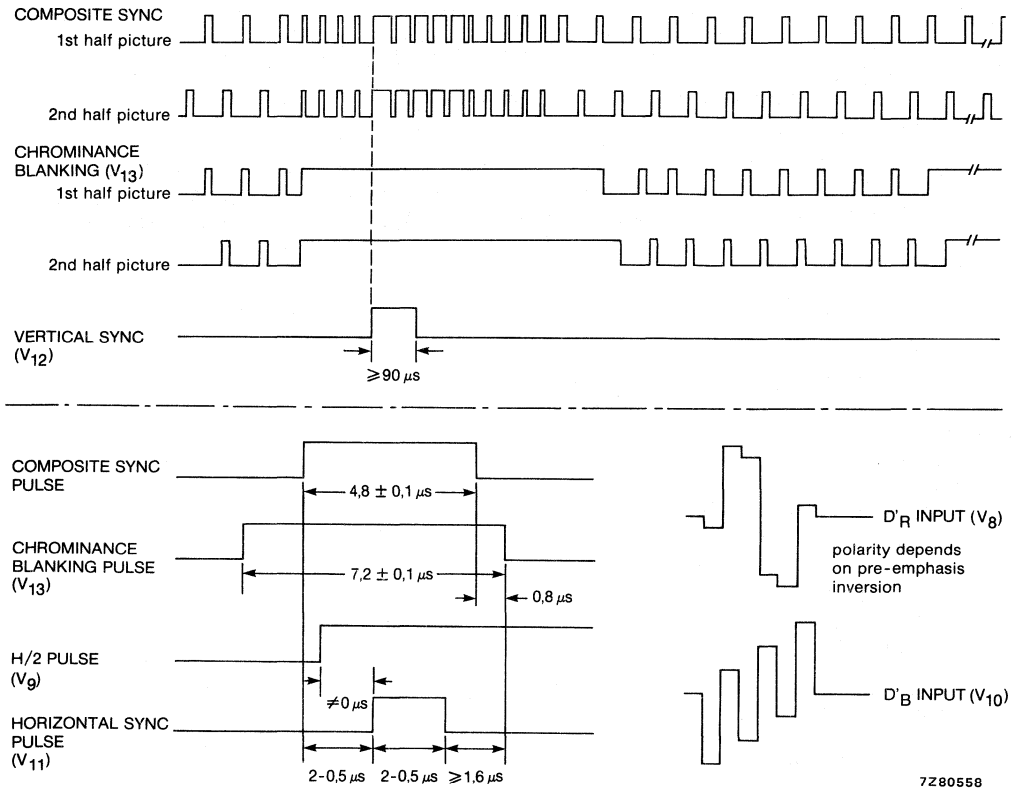


Fig. 2 Survey of input signals in relation to composite sync.

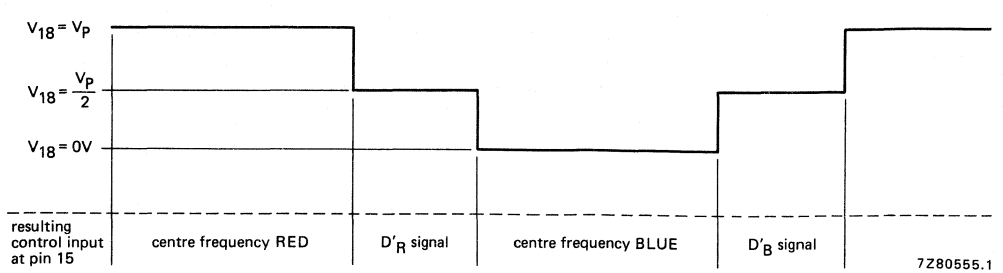


Fig. 3 Timing pulse output (pin 18) and resulting control input (pin 15).

Switched-gain summing amplifier and limiter

Inputs into the summing amplifier are the sequential D'_R* and D'_B* signals, the vertical identification sawtooth waveform and reference d.c. levels. The gain of the amplifier is switched by the internally delayed H/2 waveform to give the correct input amplitudes for the FM modulator (D'_R* gain = 280/230 x D'_B* gain). An offset is also introduced between the black levels of the D'_R* and D'_B* signals which corresponds to the upper and lower thresholds of the limiter.

FM modulator and phase switch

The FM modulator provides accurate FM modulation which follows the amplitude envelopes of the sequential D'_R* and D'_B* waveforms. The centre frequencies of 4 406,250 kHz for the D'_R* signal and 4 250,000 kHz for the D'_B* signal are controlled by d.c. levels from the sample and hold circuit (which in turn are controlled by the TDA2507). The upper and lower frequency limits are 4 756,000 ± 35 kHz and 3 900,000 ± 35 kHz.

Reference d.c. levels are switched within the FM modulator to define the starting phase of the modulator output (pin 23) at the initiation of each horizontal and vertical scan. The starting phase sequence is as follows:

vertical scan (frame to frame) 0^o, 180^o, 0^o, 180^o, repeating;

horizontal scan (line to line) 0^o, 0^o, 180^o, 0^o, 0^o, 180^o, repeating.

Chrominance blanking stage

The frequency modulated colour difference signals are passed via high-frequency pre-emphasis and band-pass filters to the chrominance blanking input at pin 3. The d.c. level of this input should be equal to the reference voltage at pin 7. Blanking occurs during the chrominance blanking pulse. The stage gain is 1,75.

Vertical identification sawtooth generator

Vertical sync, horizontal sync and chrominance blanking pulses are used to determine vertical identification (see Fig. 4). The vertical identification sawtooth generator is driven in opposite directions for identification signals IdR and IdB; the capacitor for the generator is connected at pin 14. If no vertical identification is required, pin 14 should be connected to the FM reference voltage at pin 22.

Pulse shaper

This stage developes all pulses that are required within the TDA2506 and also the timing pulses required for the modulator controller TDA2507 (see Fig. 3). Internal H/2 pulses are generated by a flip-flop working from the horizontal sync input (pin 11), this makes the H/2 input at pin 9 necessary only if it is required to lock the modulator into a specific phase sequence. If the H/2 input is not required, pin 9 should be connected to ground. A pulse separator at the chrominance blanking/colour-killer input (pin 13) allows this input to be used for blanking the sequential D'_R*/D'_B* signal.

Sample and hold circuit

This circuit provides reference voltages to the FM modulator which set the centre modulation frequencies for the sequential D'_R* and D'_B* signals. The reference voltage levels are supplied to pin 15 from the TDA2507 in a sequence that is time-related to D'_R*/D'_B* switching. The levels are sampled and then held for D'_R* using capacitors at pins 16 and 17, and for D'_B* using capacitors at pins 19 and 20.

FUNCTIONAL DESCRIPTION (continued)

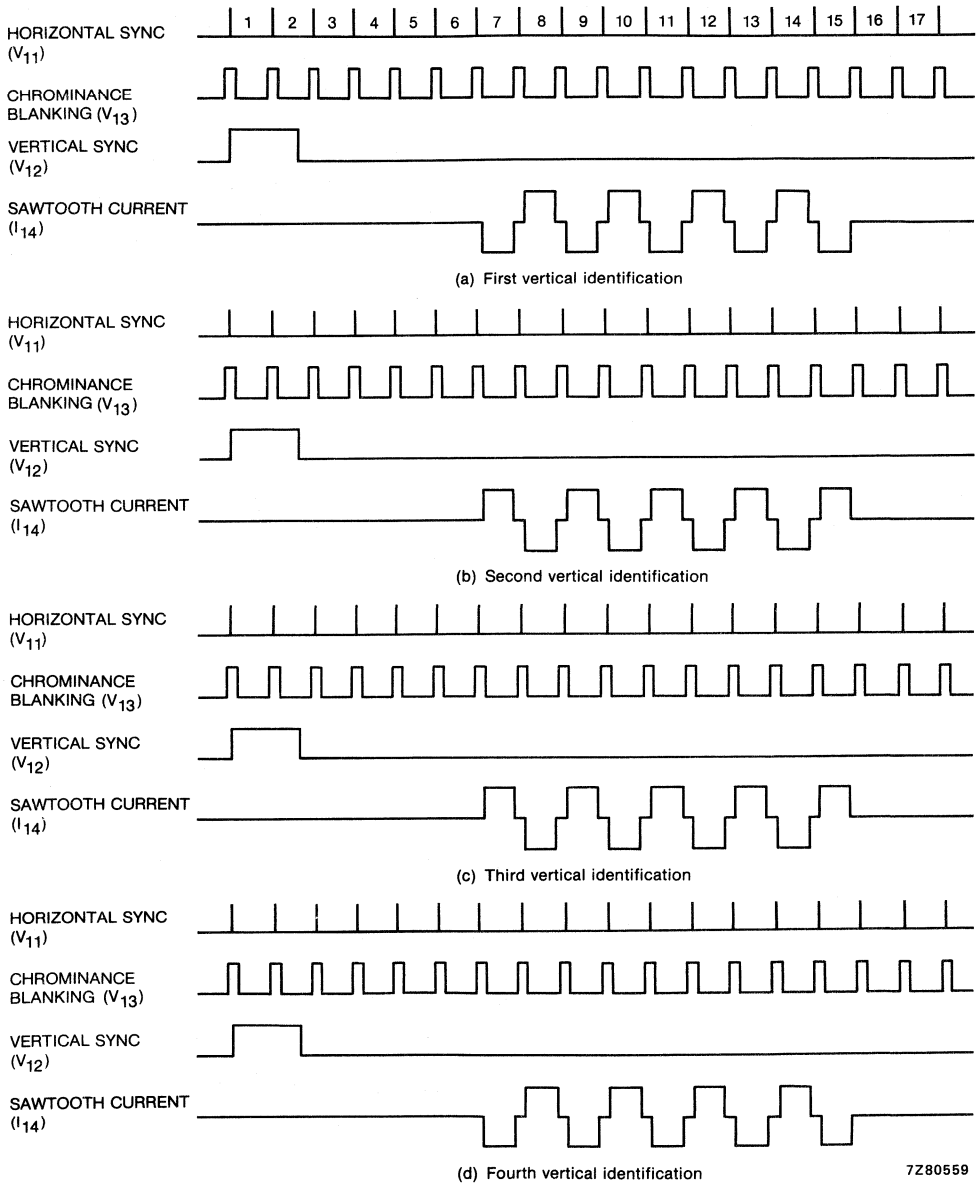


Fig. 4 Vertical identification generation.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

Supply voltage	V_{4-1}	max. 13,2 V
Total power dissipation	P_{tot}	see Figs 5 and 6
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +150 °C

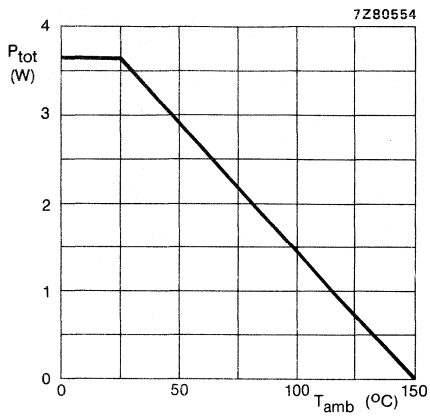


Fig. 5 Power derating curve for DIL package (SOT-101B).

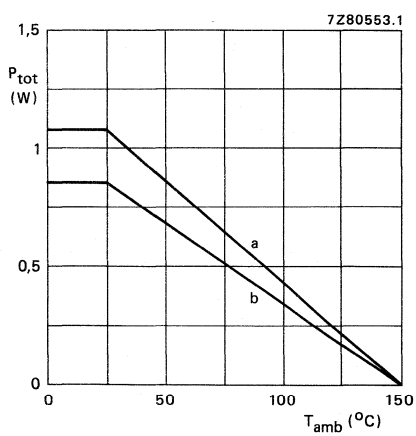


Fig. 6 Power derating curve.

a = device mounted on a ceramic substrate.
b = device mounted on a printed circuit board.

CHARACTERISTICS

$V_p = V_{4-2} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground (pins 2 and 24); all currents stated are positive into the IC; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 4)	$V_p = V_{4-2}$	4.75	5	7	V
Supply current	$I_p = I_4$	30	45	60	mA
Reference voltage (pin 7)	V_{7-2}	3.4	3.55	3.7	V
Reference voltage (pin 22)	V_{22-24}	3.35	3.5	3.65	V
Pulse shaper (pins 9,11 and 12, emitter follower inputs; pin 18, collector output)					
Bias current (pins 9 and 12)	I_9, I_{12}	–	–	10	μA
Bias current (pin 11)	I_{11}	–	–	15	μA
Input resistance (pin 9,11,12)	R_9, R_{11}, R_{12}	200	–	–	kΩ
Input pulse amplitude (pin 9,11,12)	V_9, V_{11}, V_{12}	2.5	–	–	V
Timing pulse output (pin 18) high level	V_{18}	4.7	–	–	V
intermediate ($V_p/2$) level	V_{18}	2.2	2.5	2.8	V
low level	V_{18}	–	–	0.4	V
Pulse separator (pin 13, emitter follower)					
Input resistance	R_{13}	100	–	–	kΩ
Chrominance blanking pulse amplitude	V_{13}	3.6	–	–	V
D'_R*/D'_B* blanking pulse amplitude (colour killing)	V_{13}	1.7	1.8	1.9	V
Vertical identification sawtooth generator (pin 14)					
Voltage clamping level ($I_{14} = \pm 50$ μA	V_{14}	$V_{22}-15$ mV	V_{22}	$V_{22}+15$ mV	V
Ramp current (occurs in lines 7 to 15 after vertical sync)	$\pm I_{14}$	45	65	85	μA
Maximum voltage level	V_{14}	$V_{22}+0.5$	$V_{22}+0.7$	$V_{22}+0.8$	V
Minimum voltage level	V_{14}	$V_{22}-0.8$	$V_{22}-0.7$	$V_{22}-0.5$	V
Voltage level during line blanking	V_{14}	$V_{22}-7$ mV	V_{22}	$V_{22}+7$ mV	V
Inputs D'_R*, D'_B* (pins 8 and 10)					
Signal level during clamping ($I_8, I_{10} = \pm 50$ μA)	V_8, V_{10}	V_7-25 mV	V_7	V_7+25 mV	V
Input bias current	I_8, I_{10}	–	–	1.5	μA

parameter	symbol	min.	typ.	max.	unit
Sequential amplifier output (pin 6)					
(Pins 8 and 10 AC coupled to fixed DC voltage)					
DC output	V_6	1.6	$\frac{V_7 - 10\ mV}{2}$	1.85	V
Output resistance	R_6	–	8	16	Ω
Amplifier voltage gain (pin 8 or 10 to pin 6)	$G_{8,10\text{-}6}$	1.4	1.5	1.6	
Clamping and blanking stage (pin 5)					
Input voltage (clamped; $I_5 = \pm 50\ \mu A$)	V_5	$V_{22} - 12\ mV$	V_{22}	$V_{22} + 12\ mV$	V
Input bias current ($V_5 = V_{22}$)	I_5	–	–	2.5	μA
Modulator control circuit (pin 15, buffer amplifier non-inverting input)					
Bias current ($V_{15} = V_7$)	I_{15}	–	–	1.25	μA
Permitted input signal d.c. levels	V_{15}	2	–	4.3	V
FM modulator output (pin 23, emitter follower)					
Output resistance	R_{23}	–	50	80	Ω
High DC output level at $V_{21} = 3.8\ V$	V_{23}	$V_{22} - 0.85$	–	$V_{22} - 0.7$	V
Output signal amplitude	V_{23}	0.9	1.0	1.15	V

CHARACTERISTICS (Continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance blanking stage (pin 3, emitter follower input; pin 1, amplifier output)					
Input current ($V_3 = V_7$)	I_3	–	–	15	μA
Input resistance	R_3	300	–	–	kΩ
Required DC level of input signal	V_3	–	V_7	–	V
Output resistance	R_1	–	–	10	Ω
Temperature coefficient of output DC level	V_1/T	–	1.8	—	mV/K
Amplifier gain	$\Delta V_1/\Delta V_3$	1.69	1.75	1.79	
Output DC level during blanking(V_{13} = HIGH)	V_1	V_7–0.88	V_7–0.79	V_7–0.70	V
Output DC level unblanked ($V_3 = V_7$; V_{13} = LOW)	V_1	V_7–0.88	V_7–0.79	V_7–0.70	V

A.C. CHARACTERISTICS

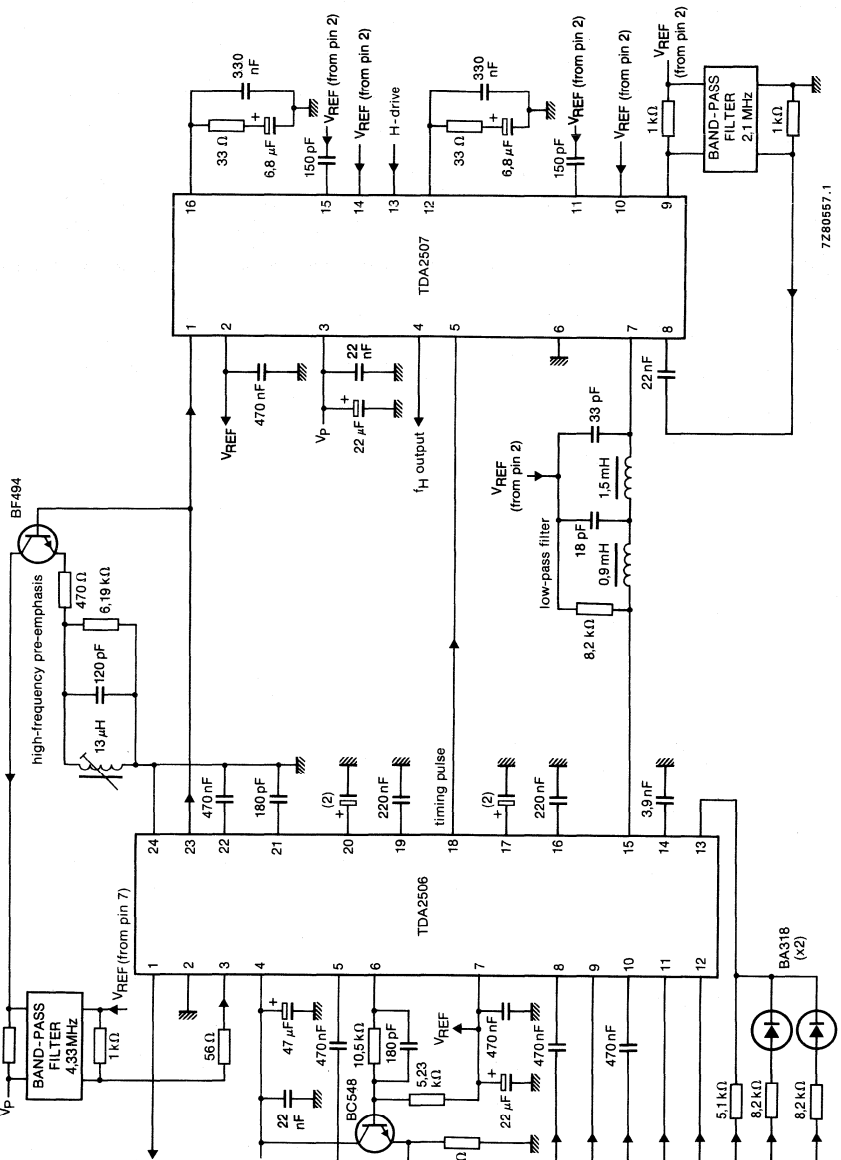
Values are valid for TDA2506 operating with TDA2507. Horizontal frequency (f_H) = 15 625 Hz.

parameter	symbol	min.	typ.	max.	unit
Centre frequency RED	f_{0R}	–	4 406,250 ± 2	–	kHz
Centre frequency BLUE	f_{0B}	–	4 250,000 ± 2	–	kHz
Ident. frequency RED *	f_{IdR}	–	4 756,250 ± 35	–	kHz
Ident. frequency BLUE *	f_{IdB}	–	3 900,000 ± 35	–	kHz
Minimum frequency RED **	$-f_R$	–	4 126,250 ± 12	–	kHz
Maximum frequency RED **	$+f_R$	–	4 686,250 ± 12	–	kHz
Minimum frequency BLUE **	$-f_B$	–	4 020,000 ± 12	–	kHz
Maximum frequency BLUE **	$+f_B$	–	4 480,000 ± 12	–	kHz

* The ident. frequencies are also the maximum and minimum output frequencies of the encoder.

** Values are valid for 75% colour bar saturation (EBU) (V_5 = ± 250 mV deviation from clamping level).

APPLICATION INFORMATION



(1) Signal amplitude for 75% colour bar (EBU) = 0,5 V (peak-to-peak value).
(2) For $V_P = 4{,}75$ to 5,3 V, $C_{17} = C_{20} = 0{,}68\ \mu F$; for $V_P > 5{,}3$ V, $C_{17} = C_{20} = 2{,}2\ \mu F$.

Fig. 7 Application using TDA2507 with PLL tuning: Vp = 5 V.

FM MODULATOR CONTROLLER

GENERAL DESCRIPTION

The TDA2507 accepts FM signals that are sequentially modulated by two alternating subcarrier frequencies (SECAM signals) and provides sequential DC output levels to control the FM modulator.

The IC is intended for use with the SECAM encoder TDA2506 but can be adapted for other applications. Timing reference pulses from the modulator are required.

Two frequency reference phase-lock loops are contained within the IC; one for 4.40625 MHz, and one for 4.250 MHz. Other frequencies can be accomplished by using external reference sources.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		$V_P = V_{3-6}$	4.75	5.0	7.0	V
Supply current	V_P = 5 V; both PLL circuits on	I_3	–	40	–	mA
Reference voltage		V_{2-6}	3.34	3.45	3.56	V
Storage temperature range		T_{stg}	−55	–	+150	°C
Operating ambient temperature range		T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

TDA2507 : 16-lead DIL; plastic (with internal heat spreader) (SOT38).
TDA2507T: 16-lead mini-pack; plastic (SO16L; SOT162A).

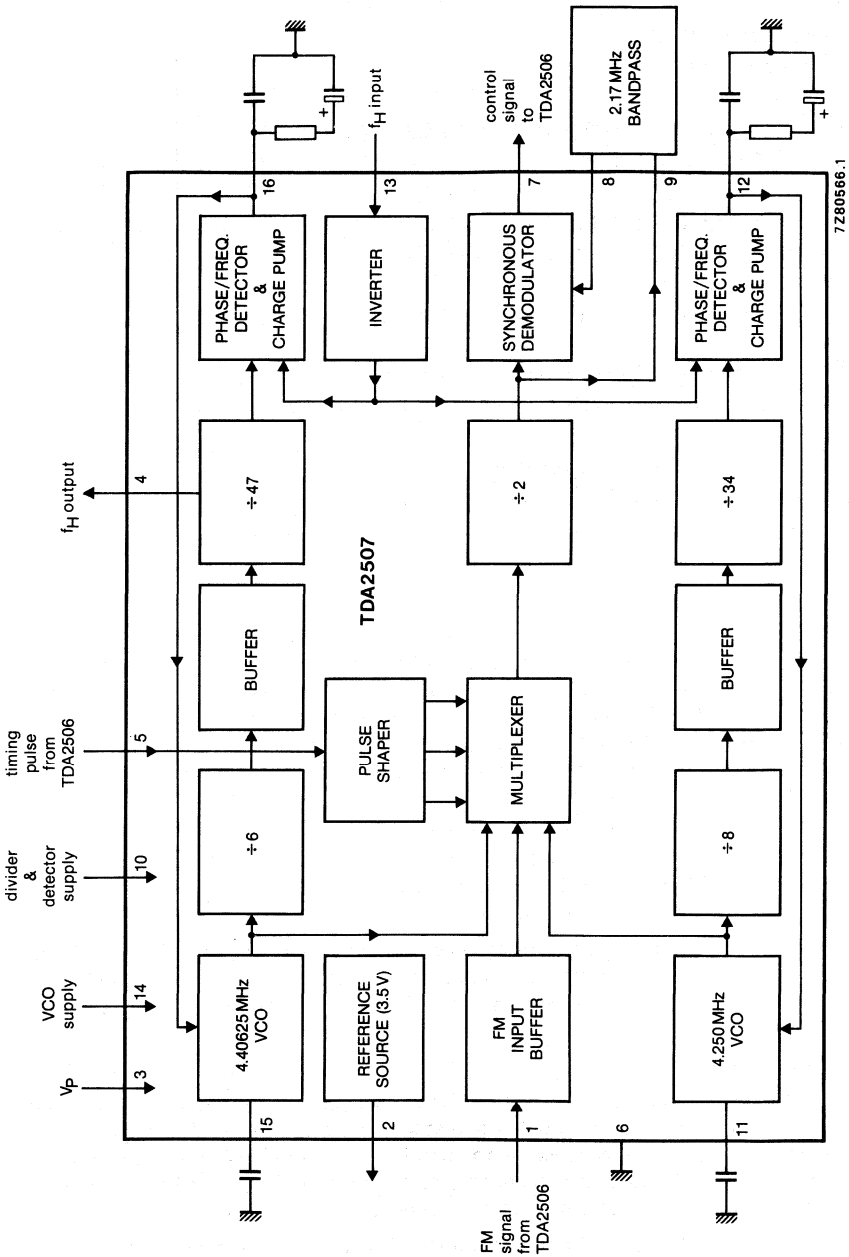


Fig.1 Block diagram.

PINNING

Pin functions

pin	description
1	FM signal input (from TDA250b)
2	Reference voltage output
3	Positive supply voltage
4	Horizontal sync output (f_H = 4 406.250/282 = 15.625 kHz)
5	Timing pulse input (from TDA2506)
6	Ground
7	Control signal output to TDA2506 via low-pass filter
8	Input to synchronous demodulator from band-pass filter
9	Output to band-pass filter
10	Supply voltage for the divider stages and phase/frequency detectors of the two phase-lock loops (PLL)
11	Tuning capacitor for the 4.250 MHz reference oscillator
12	Filter for the phase/frequency detector of the 4.250 MHz phase-lock loop
13	Horizontal sync input (f_H)
14	Supply voltage for the two reference oscillators
15	Tuning capacitor for the 4.40625 MHz reference oscillator
16	Filter for the phase/frequency detector of the 4.40625 MHz phase-lock loop.

FUNCTIONAL DESCRIPTION

Phase-lock loops

The two phase-lock loops each comprise a voltage-controlled reference oscillator, two frequency divider stages and a phase/frequency detector circuit. The loops are closed by charge pumping the reference oscillators from the phase/frequency detector outputs. The centre frequencies of the loops are set by external capacitors at pin 15 (4.40625 MHz) and pin 11 (4.250 MHz). The divider stages which follow the reference oscillators reduce the frequencies of both the loops to 15.625 kHz (f_H) at their respective inputs to the phase/frequency detectors. The reference signals to both phase/frequency detectors are obtained from the horizontal sync input at pin 13.

The divider and phase/frequency detector circuits can be switched off by connecting pin 10 to ground. This leaves only the VCO of each PLL in circuit and allows external signals to be injected at pins 15 and 11, or crystals to be used for tuning the oscillators.

The accuracy of crystal tuning using only one crystal can be obtained by connecting pins 10, 14 and 16 to the reference voltage at pin 2 and connecting a 4.40625 MHz crystal to pin 15. The 4.250 MHz PLL will follow the crystal-derived f_H reference from pin 4 via pin 13 and its phase/frequency detector.

Multiplexer and pulse shaper

The multiplexer receives the 4.40625 and 4.250 MHz reference frequencies from the two VCOs and the FM signals $D'_R{}^*$ and $D'_B{}^*$ from the TDA2506 modulator. The signals are gated one at a time to the multiplexer output in a sequence determined by the timing pulses from TDA2506. The levels of the timing pulses (pin 5) are used in the pulse shaper to generate enable pulses for the multiplexer (see Figs 2 and 3). The multiplexer output sequence is as follows:

4.40625 MHz (2 lines); $D'_R{}^*$ FM signal (1 line); 4.250 MHz (2 lines); $D'_B{}^*$ FM signal (1 line); repeating. The selection of $D'_R{}^*$ or $D'_B{}^*$ FM signal is a feature of the timing of the input at pin 5.

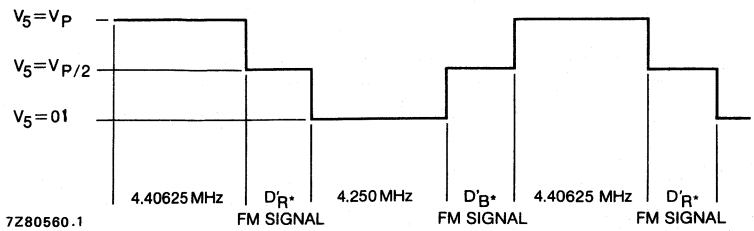


Fig.2 Timing pulse waveform for multiplexer output sequence.

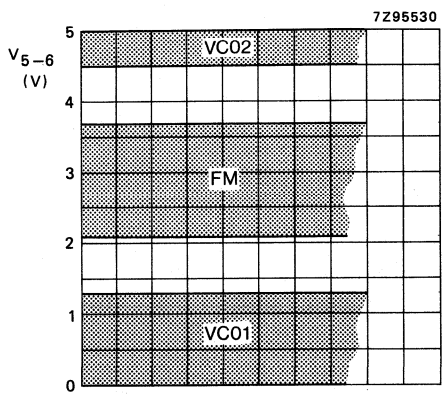


Fig.3 Switching levels of the timing pulse at pin 5.

Divide-by-two stage and synchronous demodulator

The divide-by-two stage halves the frequencies present in the multiplexer output and equalizes the amplitude and pulse shapes of the sequential signals.

Demodulation of the multiplexed signal is performed by filtering the signal via a 2.17 MHz band-pass filter (between pins 8 and 9) and using this filtered signal as a synchronous switch for the main signal. The DC level of the signal from pin 9 is referred externally to the reference voltage from pin 2. An external low-pass filter is required for the output signal from pin 7.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	13.2	V
Total power dissipation	P_{tot}	see Fig.4		W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−55	+150	°C

CHARACTERISTICS

$V_P = V_{3-6} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 3)		V_P	4.75	5.0	7.0	V
Supply current	$V_{14} = V_{10} = V_2$	I_P	–	35	–	mA
Supply current	$V_{14} = V_2$	I_P	–	20	–	mA
Reference voltage (pin 2)		V_{2-6}	3.34	3.45	3.56	V
Phase-lock loops						
DC voltage output level						
pin 11		V_{11-6}	2.4	2.6	2.8	V
pin 15		V_{15-6}	2.4	2.6	2.8	V
Amplitude of oscillation (peak-to-peak value)						
pin 11		$V_{11(p-p)}$	–	130	–	mV
pin 15		$V_{15(p-p)}$	–	130	–	mV
Input current	see Fig.5					
pin 11	$V_{12-6} = 1.5$ V	I_{11}	–	130	–	μA
pin 15	$V_{16-6} = 1.5$ V	I_{11}	–	130	–	μA
Limiting values for VCO control voltages						
pin 12		V_{12}	0.8	–	1.9	V
pin 16		V_{16}	0.8	–	1.9	V
Output resistance at pin 4	V_4 = HIGH	R_4	5.1	6.8	8.5	kΩ
Input resistance at pin 13		R_{13}	200	–	–	kΩ
Amplitude of f_H pulse required at pin 13	note 1	V_{13}	2	–	–	V
FM input buffer (pin 1)						
Input resistance		R_1	180	–	–	kΩ
Switching level of FM input		V_1	2.2	2.3	2.4	V
Required input amplitude		V_1	0.5	–	2.0	V
Pulse shaper input (pin 5)						
Input resistance		R_5	200	–	–	kΩ
Demodulator						
Sink current at pin 9 into divide-by-two circuit	V_9 = LOW	I_9	0.6	0.9	1.2	mA
Demodulator input bias voltage at pin 8		V_8	1.60	1.68	1.76	V
Demodulator output current from pin 7	see Fig.6					
output current at A		$-I_7$	0.6	0.9	1.2	mA
output current at B		I_7	1.2	0.9	0.6	mA

Note to the characteristics

1. Duty factor and timing not important.

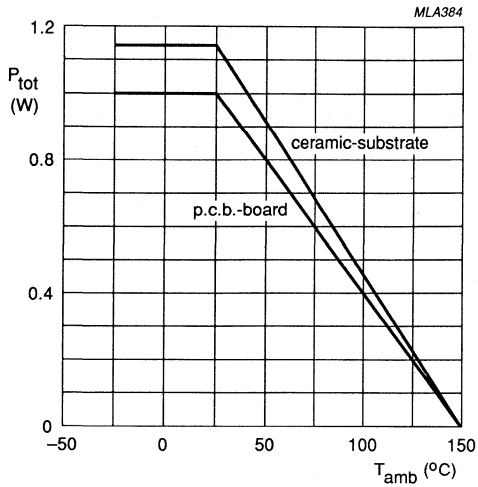


Fig.4a Power derating curve (TDA2507).

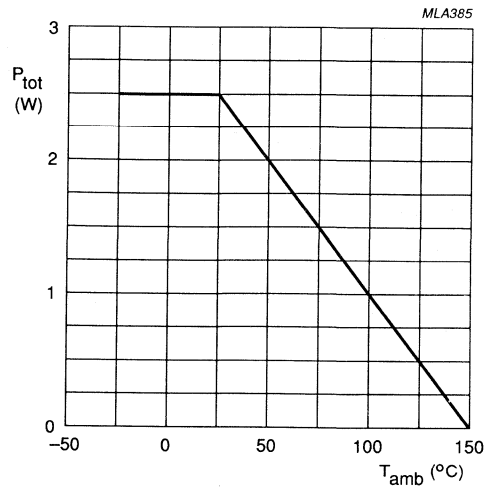


Fig.4b Power derating curve (TDA2507T).

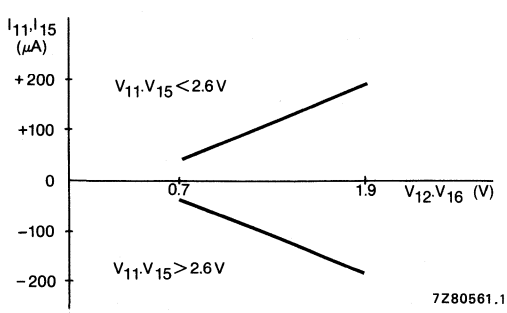


Fig.5 Current input to pins 11 and 15 as a function of voltage at pins 12 and 16 (typical values).

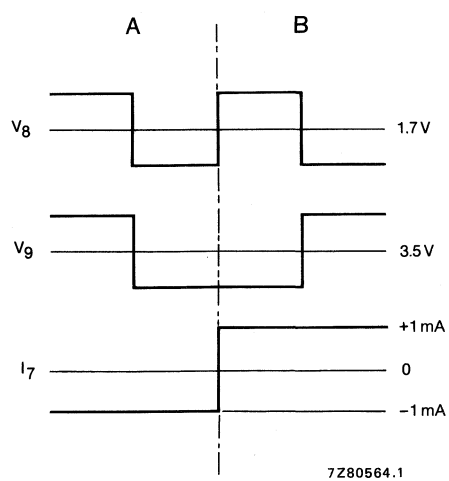


Fig.6 Demodulator output current from pin 7 (typical values).

APPLICATION INFORMATION (continued)

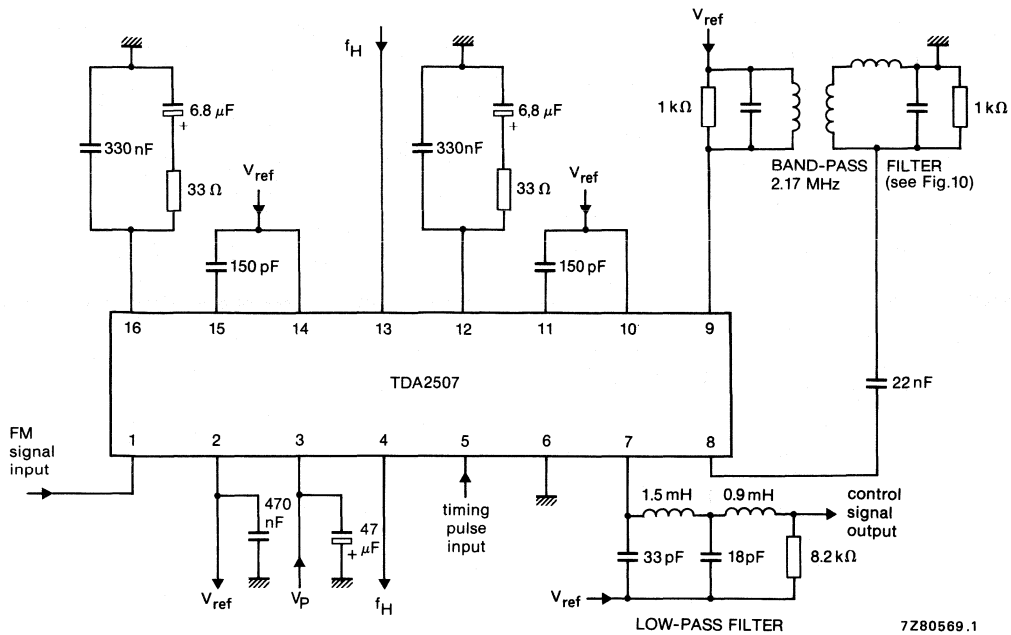


Fig.7 Application diagram using PLL tuning; V_P = 5 V.

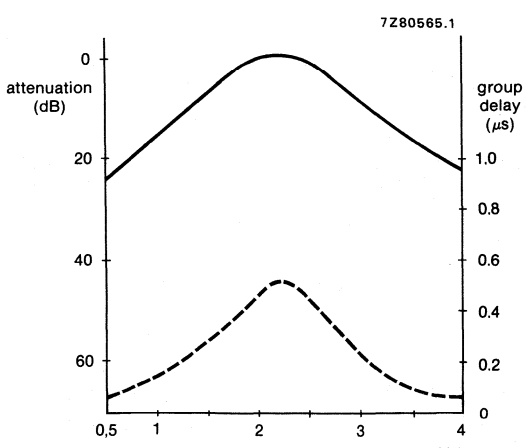


Fig.8 Typical response of 2.17 MHz band-pass filter.

DUAL FM MODEM FOR VHS HIFI AUDIO SYSTEM

GENERAL DESCRIPTION

The TDA2515 is a dual FM modulator/demodulator for processing the FM audio signal (stereo or bilingual) in VHS video recorders. The device has two channels, A and B, which are tested at 1.4 and 1.8 MHz respectively.

Features

The following features (in sequence) are used for recording and apply to both channels.

- An AF buffer amplifier
- An adjustable AF limiter
- An AF driven Current Controlled Oscillator (CCO)
- An HF output buffer

The following features (in sequence) are used for playback and also apply to both channels.

- An HF amplifier limiter
- A Phase Locked Loop (PLL) detector with CCO and filter section
- A voltage to current converter
- An AF amplifier with Sample and Hold (S & H) circuit

Further features are:

- An internal voltage stabilizer
- An HF level detector (in channel A)
- A mute timing and delay circuit (in channel A)
- A record/playback switch (connected to channels A and B)
- A logic circuit for mute and mute enable
- A pulse shaper, driven by the Head Identification (HID) signal, to generate the hold pulse for the S & H circuits (channels A and B)

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Operating supply voltage		V_P	4.75	5	5.25	V
Supply current						
playback	$V_{22} \leqslant 1.5$ V	I_P	–	50	60	mA
recording	$V_{22} \geqslant 3.5$ V	I_P	–	35	40	mA

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

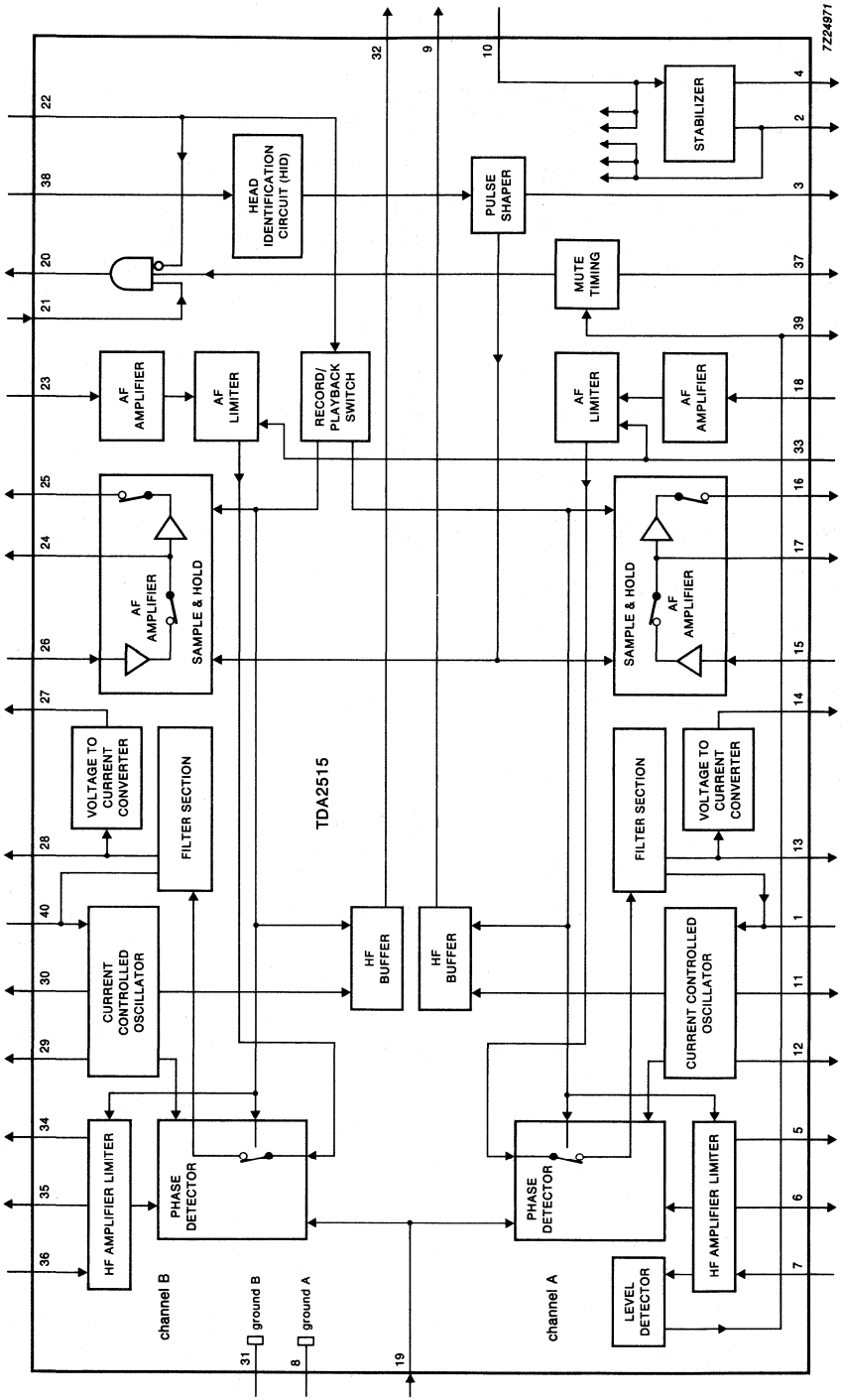


Fig.1 Block diagram.

PINNING

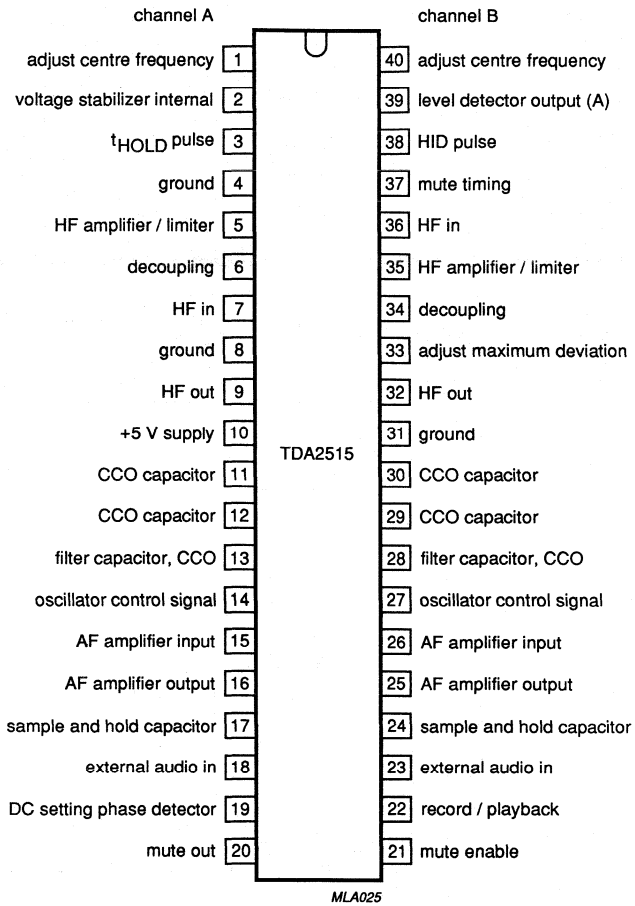


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134). All voltages with reference to pin 8; all currents positive into the device.

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)	V_P	0	–	6	V
Voltage on all pins	V	0	–	V_P	V
Total power dissipation	P_{tot}		see Fig.3		
Operating ambient temperature range	T_{amb}	−20	–	+70	°C
Storage temperature range	T_{stg}	−65	–	+150	°C

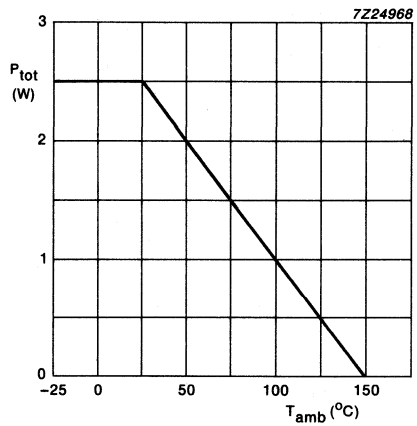


Fig.3 Power derating curve.

DC CHARACTERISTICS

According to the test set-up illustrated by Fig.4; V_P = 5 V; T_{amb} = 25 °C; unless otherwise specified; pins 31 and 4 connected to pin 8. All voltages with respect to pin 8.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_P	4.75	5	5.25	V
Supply current						
playback	$V_{22} \pm 1.5$ V	I_P	–	50	60	mA
record	$V_{22} \pm 3.5$ V	I_P	–	35	40	mA
difference playback/recording		$\|\Delta I_P\|$	–	15	25	mA
Total power dissipation						
playback	$V_{22} \pm 1.5$ V	P_{tot}	–	250	–	mW
record	$V_{22} \pm 3.5$ V	P_{tot}	–	175	–	mW
Voltage on pins 1 and 40		$V_{1,40}$	–	1.9	–	V
Voltage on pin 2	note 1	V_2	2.4	2.5	2.6	V
Voltage on pins 5 and 34	note 2	$V_{5,34}$	–	3.3	–	V
Voltage on pins 6 and 35	note 2	$V_{6,35}$	–	3.3	–	V
Voltage on pins 13 and 28		$V_{13,28}$	–	1.9	–	V
Voltage on pins 15 and 26		$V_{15,26}$	–	2.5	–	V
Voltage on pins 16 and 25	note 2	$V_{16,25}$	–	2.4	–	V
Voltage on pins 18 and 23		$V_{18,23}$	–	2.5	–	V
Voltage on pin 19		V_{19}	–	1.9	–	V
Voltage on pins 14 and 27		$V_{14,27}$	–	1.2	–	V
Voltage on pin 33		V_{33}	–	2.5	–	V
Current supplied from pin 2		$-I_2$	–	–	1	mA

Notes to DC characteristics

1. Temperature drift V_{ref} = typically 50 μV/°C.
2. Playback ($V_{22} \leqslant 1.5$ V).

AC CHARACTERISTICS

All voltages with reference to pin 8.

parameter	conditions	symbol	min.	typ.	max.	unit
Recording circuit	AF input frequency = 1 kHz; $V_{22} \geqslant 3.5$ V					
Overall performance						
Total harmonic distortion of HF	$\Delta f = 50$ kHz	THD	–	0.2	–	%
	$\Delta f = 150$ kHz; note 1	THD	–	0.4	0.6	%
External audio current (pins 18 and 23)	$\Delta f = 150$ kHz	I_I	25	30	33	μA
Maximum deviation setting (pin 33)	$R13 = V_{ref}/I_I$	Δf	–	150	–	kHz
difference (in channel)		$\pm\Delta f$	–	–	7.5	kHz
difference of channels A and B		$\pm\Delta f$	–	–	7.5	kHz
High frequency output stage						
Output voltage (pin 9) (peak-to-peak)		V_O	0.43	0.5	0.57	V
Output voltage (pin 32) (peak-to-peak)		V_O	1.3	1.51	1.73	V
Current difference	$I_{32}/I_9 = 3\ (1 + \Delta)$	$\lvert\Delta\rvert$	–	–	6	%
Output resistance (pin 9)		$R_{9\text{-}10}$	400	500	600	Ω
Output resistance (pin 32)		$R_{32\text{-}10}$	400	500	600	Ω
Second harmonic suppression			–	48	–	dB
Intermodulation						
channel B to A		IM	–	–40	–	dB
channel A to B		IM	–	–40	–	dB
Ripple rejection	note 2	RR	–	40	–	dB
Playback circuit	input frequency = 1.4 or 1.8 MHz; $\Delta f = 150$ kHz and $f_{mod} = 1$ kHz; $V_{22} \leqslant 1.5$ V					
HF amplifier/limiter/PLL						
Input conductance		g_{ie}	–	1	–	μS
Input capacitance		C_{ie}	–	4	–	pF
Sensitivity	PLL locked	V_{IHF}	–	100	300	μV

parameter	conditions	symbol	min.	typ.	max.	unit
Signal-to-noise ratio	note 3					
	V_{IHF} = 300 μV	S/N	–	50	–	dB
	V_{IHF} = 10 mV	S/N	–	60	–	dB
AM rejection	note 4					
	V_{IHF} = 1 mV	AMR	–	53	–	dB
	V_{IHF} = 10 mV	AMR	–	58	–	dB
Current controlled oscillator (CCO)						
CCO frequency (adjustable)	note 5	f_{CCO}	–	1.4	–	MHz
		f_{CCO}	–	1.8	–	MHz
Input current (internal)	Δf = 150 kHz	I_{p-p}	25	30	33	μA
Lock range (deviation from f_{CCO}, channels A and B)	V_I = 10 mV	Δf_{CCO}	–	±550	–	kHz
Temperature coefficient		TC	–	–250	–	10^{-6}/°C
PLL demodulator circuit						
Phase response time	Δφ = 90 deg	t_s	–	4.5	–	μs
Phase detector current		$\|I_{PD}\|$	–	106	–	μA
Ratio of $+I_{PD}$/(sum of loop filter resistors)			6	10	14	nA/Ω
Output voltage at pins 14 and 27 (RMS value)	±Δf = 150 kHz	V_O	–	105	–	mV
Buffer amplifier and sample and hold circuit						
Input resistance		$R_{15,26}$	–	50	–	kΩ
Load resistor		$R_{16,25}$	2.5	–	–	kΩ
Voltage gain		G_v	–	20	–	dB
DC shift during hold pulse		V_{DCpeak}	–	3	8	mV
Hold time pulse from pulse shaper	note 6;Fig.5	t_{HOLD}	3.8	4.5	5.2	μs
Delay of HID pulse to hold pulse	Fig.5	t_D	0.35	1	1.2	μs
HID crosstalk $V_{38\text{-}16,25}$		$V_{(p-p)}$	–	0.4	–	mV
Overall performance	without S & H; V_{IHF} = 10 mV					
Output voltage (RMS value)		$V_{16,25}$	0.75	0.85	1.0	V
Signal-to-noise ratio	note 3	S/N	50	60	–	dB
Total harmonic distortion + noise		THD + N	–	0.2	0.6	%

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Level detector circuit						
Level detector output	V_{IHF} = 1 mV	V_{odc}	1.2	1.8	2.8	V
	V_{IHF} = 10 mV	V_{odc}	2.4	3.0	3.7	V
	V_{IHF} = 100 mV	V_{odc}	3.8	4.4	4.9	V
Mute activated		V_{IHF}	1.25	2.2	3.75	mV
Output resistance (internal)		R_{39-8}	–	10	–	kΩ
Head identification circuit	HID pulse = 25 Hz 50% duty factor					
Input voltage (pin 38)						
HIGH		V_{IH}	2.75	–	–	V
LOW		V_{IL}	–	–	2.25	V
Input current (pin 38)						
HIGH	V_I = 5 V	I_{IH}	–	–	0.2	μA
LOW	V_I = 0.3 V	I_{IL}	–	–	10	μA
Logic circuit						
Record, playback (pin 22)						
Playback voltage		V_{IL}	–	–	1.5	V
Playback current	V_I = 0 V	I_{IL}	65	–	400	μA
Record voltage		V_{IH}	3.5	–	–	V
Record current	V_I = 5 V	I_{IH}	–	–	14	μA
Mute enable FM (pin 21)						
HIGH (mute enabled)		V_I	1	–	–	V
Input current	V_I = 1 V	I_I	20	37	60	μA
LOW (mute disabled)	I_I = 0 A	V_I	–	–	0.5	V
Mute output (pin 20)						
HIGH	I_O = –0.4 mA	V_O	4	–	–	V
LOW	I_O = 0.4 mA	V_O	–	–	0.5	V
Level detector mute	$V_{IHF} < 1.25$ mV; V_{21} = 1 V	V_O	4	–	–	V
Mute delay (pin 37)	$V_{21} \geq 1$ V; $V_{22} \leq 1.5$ V					
Switch off (signal to no signal)		t_{OFF}	–	15	–	ms
Switch on (no signal to signal)		t_{ON}	–	400	–	ms

Notes to AC characteristics

1. Maximum deviation adjusted for 165 kHz.
2. V_{ripple} = 10 mV; with respect to Δf = 150 kHz.
3. AF bandwidth of 300 Hz to 15 kHz.
4. FM: f_{mod} = 1 kHz; Δf = 150 kHz
   AM: f_{mod} = 400 Hz; m = 0.3
5. For f_{CCO} = 1.4 MHz, R5 = 5.6 kΩ ± 5%;
   RT = R5 + R7 = 7.7 kΩ (nom.)
   For f_{CCO} = 1.8 MHz, R6 = 3.3 kΩ ± 5%;
   RT = R6 + R8 = 5.8 kΩ (nom.)
   with C7 and C8 = 470 pF ± 5%; R7 and R8 = 4.7 kΩ (potentiometers).
6. With fixed resistor and fixed capacitor (R15 = 10 kΩ; C23 = 680 pF; 1% tolerance).

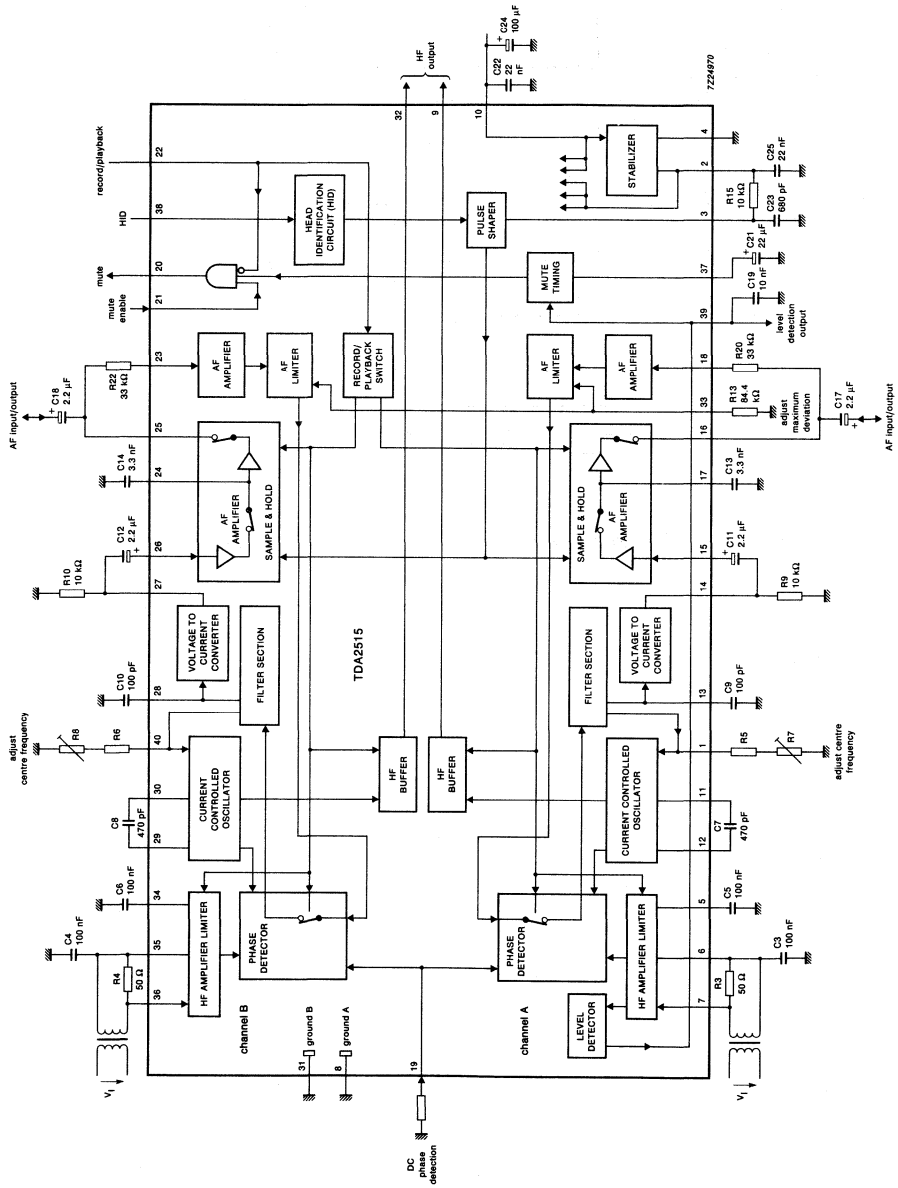


Fig.4 Test set-up diagram.

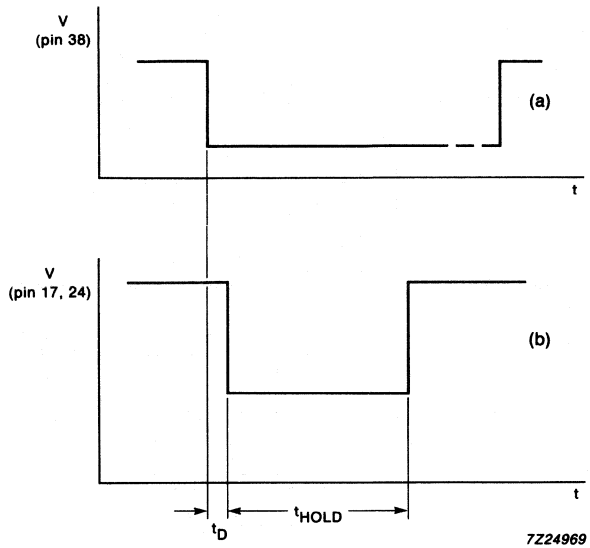


Fig.5 (a) Head identification pulse (HID) (b) Hold pulse.

QUASI-SPLIT-SOUND CIRCUIT

GENERAL DESCRIPTION

The TDA2545A is a monolithic integrated circuit for quasi-split-sound processing in television receivers.

Features

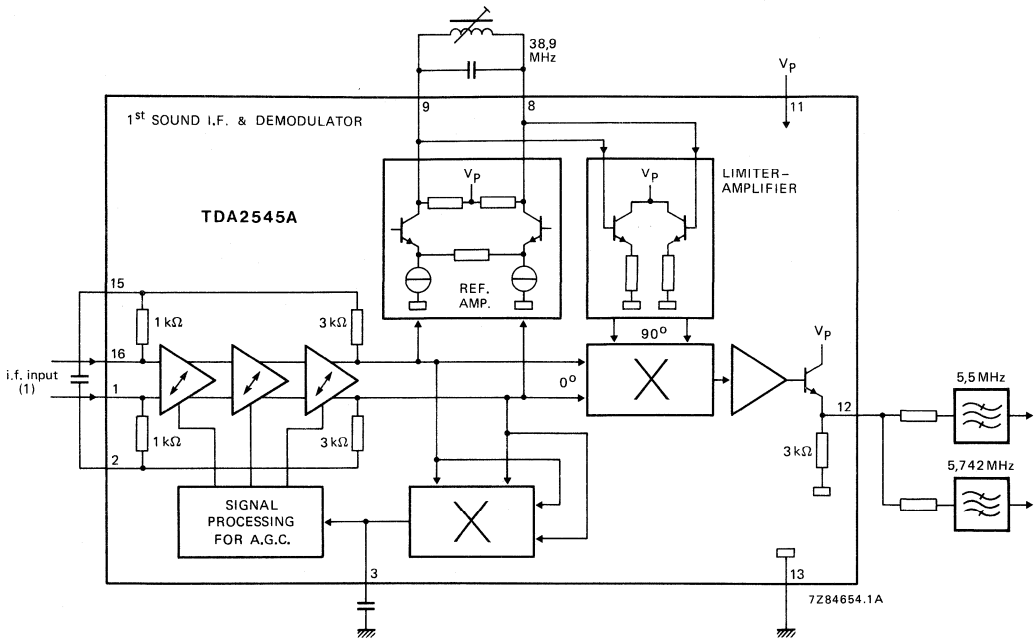
- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

QUICK REFERENCE DATA

Supply voltage (pin 11)	$V_P = V_{11\text{-}13}$	typ.	12 V
Supply current (pin 11)	$I_P = I_{11}$	typ.	45 mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}16(rms)}$	typ.	150 μV
Output voltage; 5,5 MHz (r.m.s. value)	$V_{12\text{-}13(rms)}$	typ.	100 mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{12\text{-}13(rms)}$	typ.	45 mV
I.F. control range	ΔG_V	typ.	64 dB
Signal-to-weighted-noise ratio (rel. to 1 kHz; 30 kHz deviation)			
at 5,5 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	58 dB
at 5,742 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	56 dB

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-13}$	max.	13,2	V
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

CHARACTERISTICS

$V_P = V_{11-13} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz:

Vision carrier (V.C.) modulated with different video signals (see below); modulation depth 100% (proportional to 10% residual carrier).

Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
Vision-to-sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB.

Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation $\Delta f = \pm 30$ kHz.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 11)					
Supply voltage	$V_P = V_{11-13}$	10,8	12	13,2	V
Supply current	$I_P = I_{11}$	33	45	55	mA
I.F. amplifier					
Input voltage for start of gain control (intercarrier signals −3 dB)	$V_{VC1-16(rms)}$	–	150	200	μV
Input voltage for end of gain control (intercarrier signals + 1 dB)	$V_{VC1-16(rms)}$	100	250	–	mV
I.F. gain control range	ΔG_v	60	64	–	dB
Control voltage range (see Fig. 3)	V_{3-13}	4	–	V_p	V
Input resistance	R_{1-16}	–	2,5	–	kΩ
Input capacitance	C_{1-16}	–	1,5	–	pF
Intercarrier generation					
Output voltage; 5,5 MHz (r.m.s. value)	$V_{12-13(rms)}$	60	100	140	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{12-13(rms)}$	27	45	63	mV
D.C. output voltage	V_{12-13}	–	5,9	–	V
Allowable d.c. load resistance at the output	R_{12-13}	7	–	–	kΩ
Allowable output current	$-I_{12}$	–	–	1	mA
Intercarrier signal-to-noise (see note 1) (measured behind the FM demodulators) weighted according to CCIR 468-2, quasi-peak					
a. 2T/20T pulses with white bars (see also Fig. 4)					
at 5,5 MHz	S+W/W	53	58	–	dB
at 5,742 MHz	S+W/W	51	56	–	dB
b. 6 kHz sinewave					
at 5,5 MHz	S+W/W	50	53	–	dB
at 5,742 MHz	S+W/W	50	53	–	dB
c. black level (sync pulses only)					
at 5,5 MHz	S+W/W	60	65	–	dB
at 5,742 MHz	S+W/W	58	63	–	dB

Note 1.
Incidental phase on the vision carrier, caused by TV transmitter, has to be less than 0,5 degrees for black to white transient (equivalent to S+W/W = 56 dB for 6 kHz sinewave).

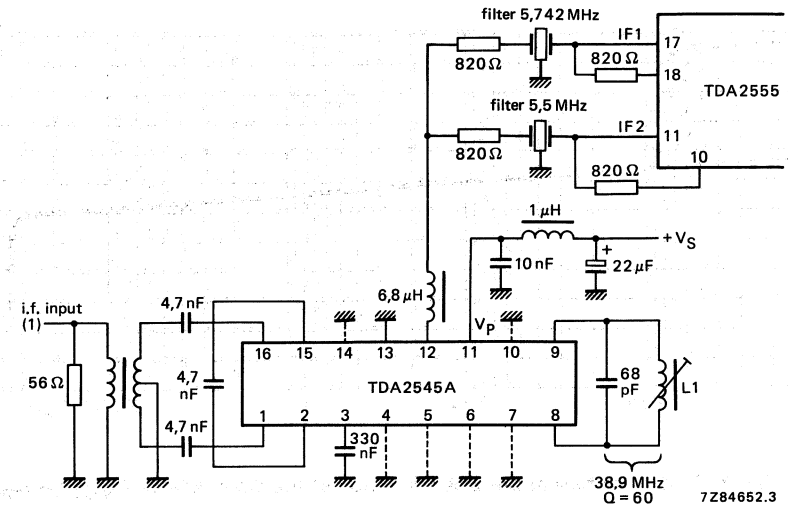


Fig. 2 Measuring circuit for TDA2545A.

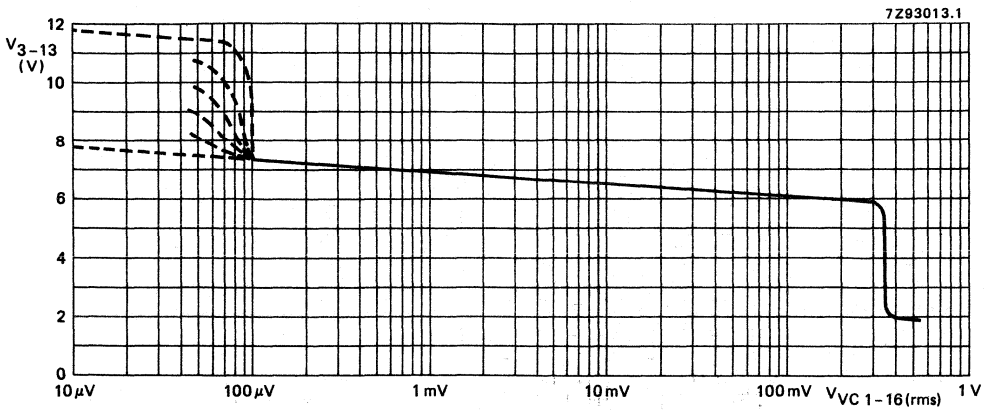


Fig. 3 Control voltage at pin 3 as a function of the input voltage $V_{VC1-16(rms)}$.

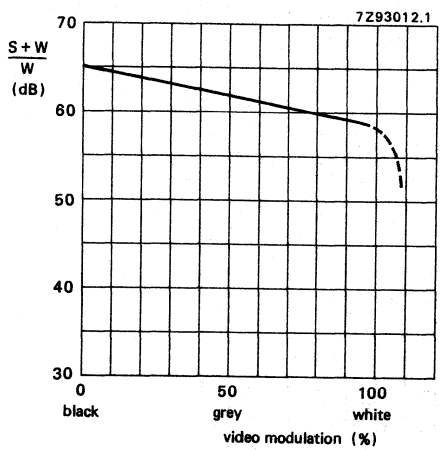


Fig. 4 Signal-to-weighted-noise ratio depending on video modulation.

QUASI-SPLIT-SOUND CIRCUIT WITH 5,5 MHz DEMODULATION

GENERAL DESCRIPTION

The TDA2546A is a monolithic integrated circuit for quasi-split-sound processing, including 5,5 MHz demodulation, in television receivers.

Features

1st i.f. (V.C.: vision carrier plus S.C.: sound carrier)

- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

2nd i.f. (5,5 MHz signal)

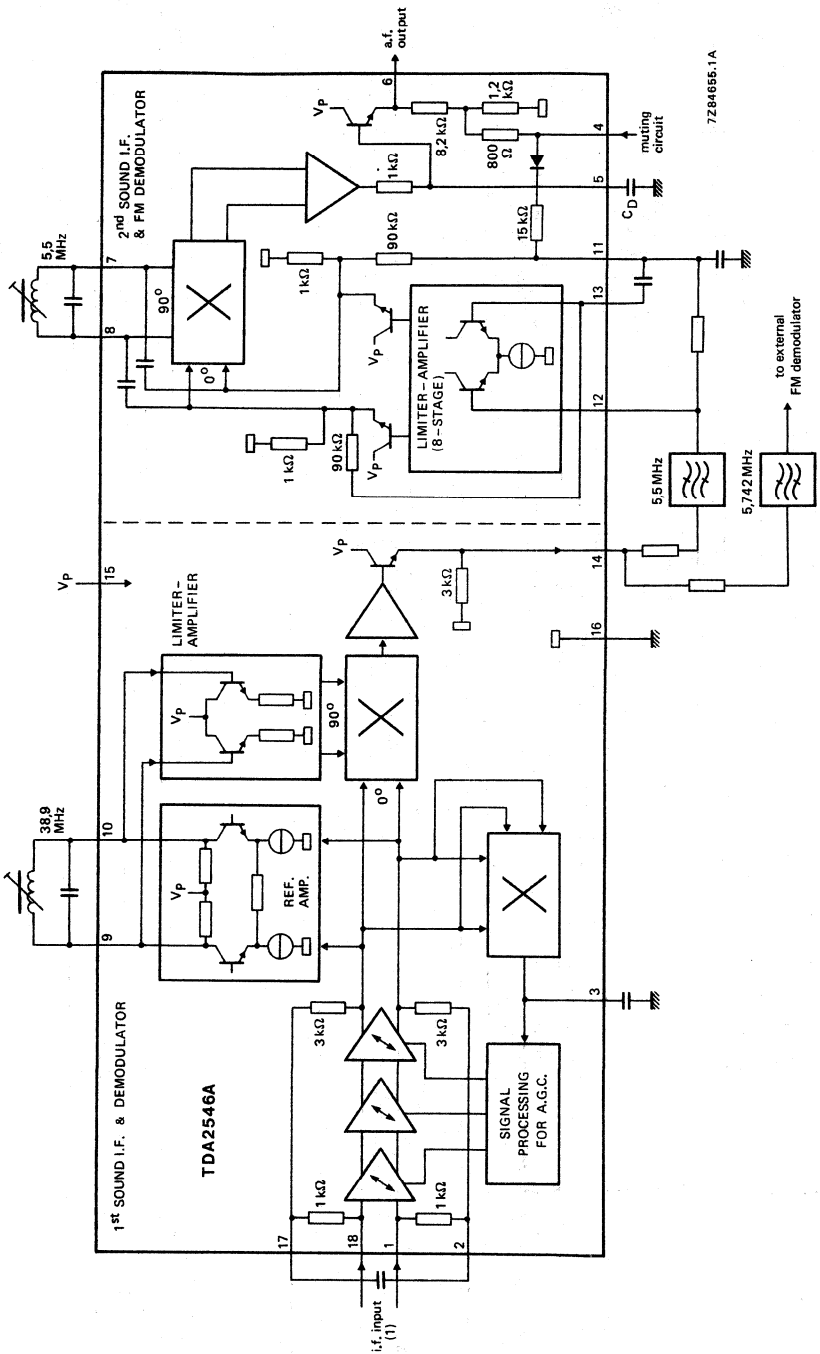
- 8-stage limiter amplifier
- Quadrature demodulator
- A.F. amplifier with de-emphasis
- AV switch

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_P = V_{15\text{-}16}$	typ.	12 V
Supply current (pin 15)	$I_P = I_{15}$	typ.	57 mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}18(rms)}$	typ.	150 μV
Output voltage; 5,5 MHz (r.m.s. value)	$V_{14\text{-}16(rms)}$	typ.	100 mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{14\text{-}16(rms)}$	typ.	45 mV
I.F. control range	ΔG_v	typ.	64 dB
Signal-to-weighted-noise ratio (rel. to 1 kHz; 30 kHz deviation)			
at 5,5 MHz (for 2T/20T pulses with white bars)	S + W/W	typ.	58 dB
at 5,742 MHz (for 2T/20T pulses with white bars)	S + W/W	typ.	56 dB
A.F. output voltage (r.m.s. value)	$V_{o6\text{-}16(rms)}$	typ.	0,6 V

PACKAGE OUTLINES

18-lead DIL; plastic (SOT102).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15\text{-}16}$	max.	13,2	V
Input current (pin 4)	I_4	max.	7	mA
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

CHARACTERISTICS

$V_P = V_{15-16} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz:

Vision carrier (V.C.) modulated with different video signals (see below); modulation depth 100% (proportional to 10% residual carrier).

Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
Vision-to-sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB.

Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation $\Delta f = \pm 30$ kHz.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15-16}$	10,8	12	13,2	V
Supply current	$I_P = I_{15}$	40	57	75	mA
I.F. amplifier					
Input voltage for start of gain control (intercarrier signals −3 dB)	$V_{VC1-18(rms)}$	–	150	200	μV
Input voltage for end of gain control (intercarrier signals + 1 dB)	$V_{VC1-18(rms)}$	100	250	–	mV
I.F. gain control range	ΔG_V	60	64	–	dB
Control voltage range (see Fig. 3)	V_{3-16}	4	–	V_p	V
Input resistance	R_{1-18}	–	2,5	–	kΩ
Input capacitance	C_{1-18}	–	1,5	–	pF
Intercarrier generation					
Output voltage; 5,5 MHz (r.m.s. value)	$V_{14-16(rms)}$	60	100	140	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{14-16(rms)}$	27	45	63	mV
D.C. output voltage	V_{14-16}	–	5,9	–	V
Allowable d.c. load resistance at the output	R_{14-16}	7	–	–	V
Allowable output current	$-I_{14}$	–	–	1	mA
Frequency demodulator (measured at f = 5,5 MHz)					
Input voltage vor start of limiting (r.m.s. value)	$V_{12-16(rms)}$	–	–	100	μV
Maximum input voltage (r.m.s. value)	$V_{12-16(rms)}$	–	200	–	mV
D.C. output voltage	$V_{11,12,13-16}$	–	2,2	–	V

parameter	symbol	min.	typ.	max.	unit
A.F. output voltage (r.m.s. value)	$V_{6\text{-}16(rms)}$	450	600	810	mV
D.C. output voltage	$V_{6\text{-}16}$	–	4	–	V
Allowable d.c. load resistance at the output	$R_{6\text{-}16}$	27	–	–	kΩ
Allowable a.c. load impedance at the output	$Z_{6\text{-}16}$	10	–	–	kΩ
Total harmonic distortion	THD	–	–	1	%
Internal de-emphasis resistance	$R_{i5\text{-}16}$	–	1	–	kΩ
Switching voltage (pin 4)					
for mute	$V_{4\text{-}16}$	9	–	–	V
for a.f. on	$V_{4\text{-}16}$	–	–	2,5	V
Intercarrier signal-to-noise (measured behind the FM demodulators)					
Signal-to-weighted-noise ratio according to CCIR 468-2, quasi-peak 2T/20T pulses with white bars (see also Fig. 4)					
at 5,5 MHz	S+W/W	53	58	–	dB
at 5,742 MHz	S+W/W	51	56	–	dB
6 kHz sine wave					
at 5,5 MHz	S+W/W	50	53	–	dB
at 5,742 MHz	S+W/W	50	53	–	dB
with black level (vision carrier modulated with sync pulses only)					
at 5,5 MHz	S+W/W	60	65	–	dB
at 5,742 MHz	S+W/W	58	63	–	dB

NOTES TO THE CHARACTERISTICS

1. Incidential phase on the vision carrier, caused by TV-transmitter, has to be less than 0,5 degrees for black to white transient.
   (Equivalent to S+W/W = 56 dB for 6 kHz sine wave).

(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

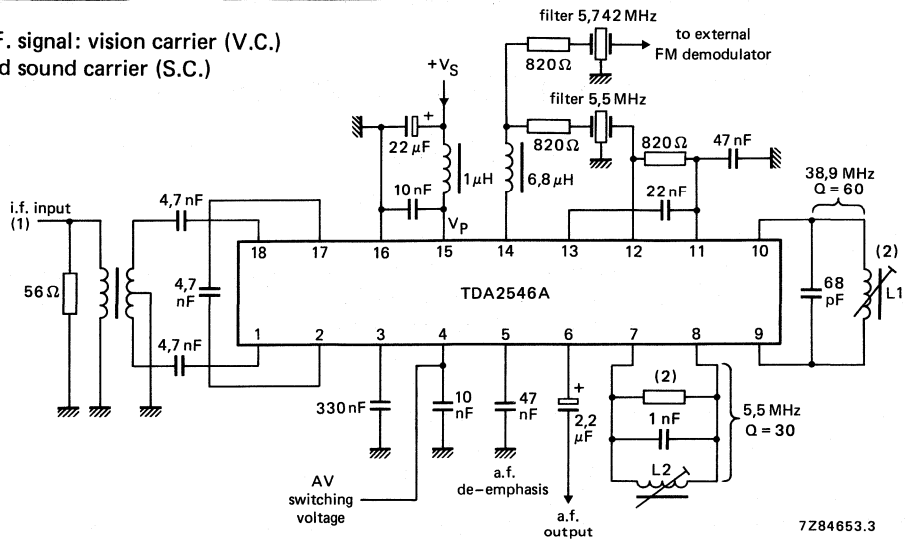


Fig. 2 Measuring circuit for TDA2546A.

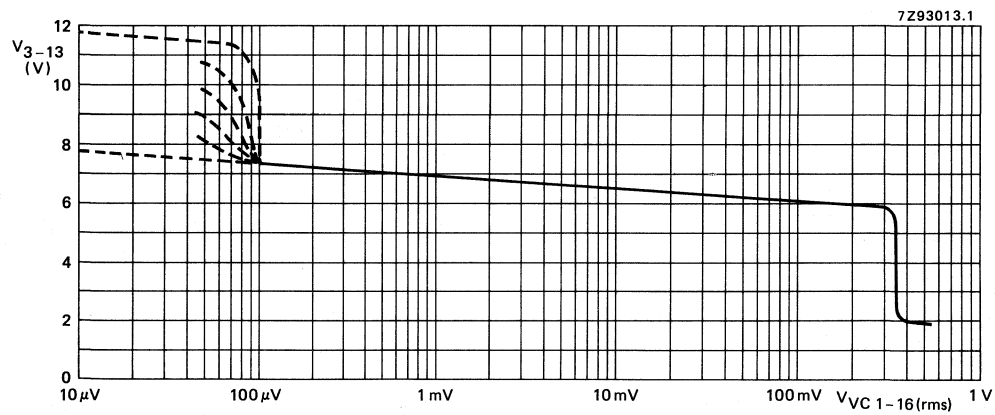


Fig. 3 Control voltage at pin 3 as a function of the input voltage $V_{VC1-18(rms)}$.

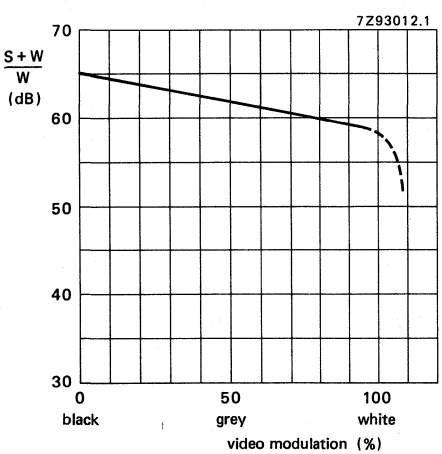


Fig. 4 Signal-to-weighted-noise ratio depending on video modulation.

I.F. AMPLIFIER AND DEMODULATOR FOR MULTISTANDARD TV RECEIVERS

GENERAL DESCRIPTION

The TDA2549 is a complete i.f. circuit with a.f.c., a.g.c., demodulation and video preamplification facilities for multistandard television receivers. It is capable of handling positively and negatively modulated video signals in both colour and black/white receivers.

Features

- Gain-controlled wide-band amplifier providing complete i.f. gain
- Synchronous demodulator for positive and negative modulation
- Video preamplifier with noise protection for negative modulation
- Auxiliary video input and output (75 Ω)
- Video switch to select between auxiliary video input signal and demodulated video signal
- A.F.C. circuit with on/off switch and inverter switch
- A.G.C. circuit for positive modulation (mean level) and negative modulation (noise gate)
- A.G.C. output for controlling MOSFET tuners

QUICK REFERENCE DATA

Supply voltage (pins 13 and 21)	$V_P = V_{13;21-3}$	typ.	12 V
Supply current (pins 13 and 21)	$I_P = I_{13;21-3}$	typ.	82 mA
I.F. input signal at V_o = 2 V (between pins 6 and 7)	$V_i = V_{6-7}$	typ.	50 μV
Video output voltage at V_i = 0 V (between pins 22 and 3)			
positive modulation	$V_o = V_{22-3}$	typ.	2 V
negative modulation	$V_o = V_{22-3}$	typ.	4 V
Gain control range	G_v	typ.	74 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	57 dB
A.F.C. output voltage swing (pin 15)	V_{15-3}	min.	10 V
Max. tuner a.g.c. output current (pin 10)	I_{10}	min.	0,3 mA
Video bandwidth (3 dB)	B	typ.	5,5 MHz
Auxiliary video input voltage (pin 12) at V_o = 2 V (peak-to-peak value)	$V_{12-3(p-p)}$	typ.	1 V
Auxiliary video output impedance (pin 14)	$\lvert Z_{14-3}\rvert$	typ.	7 Ω
Auxiliary video output voltage (pin 14)	V_{14-3}	typ.	2 V

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

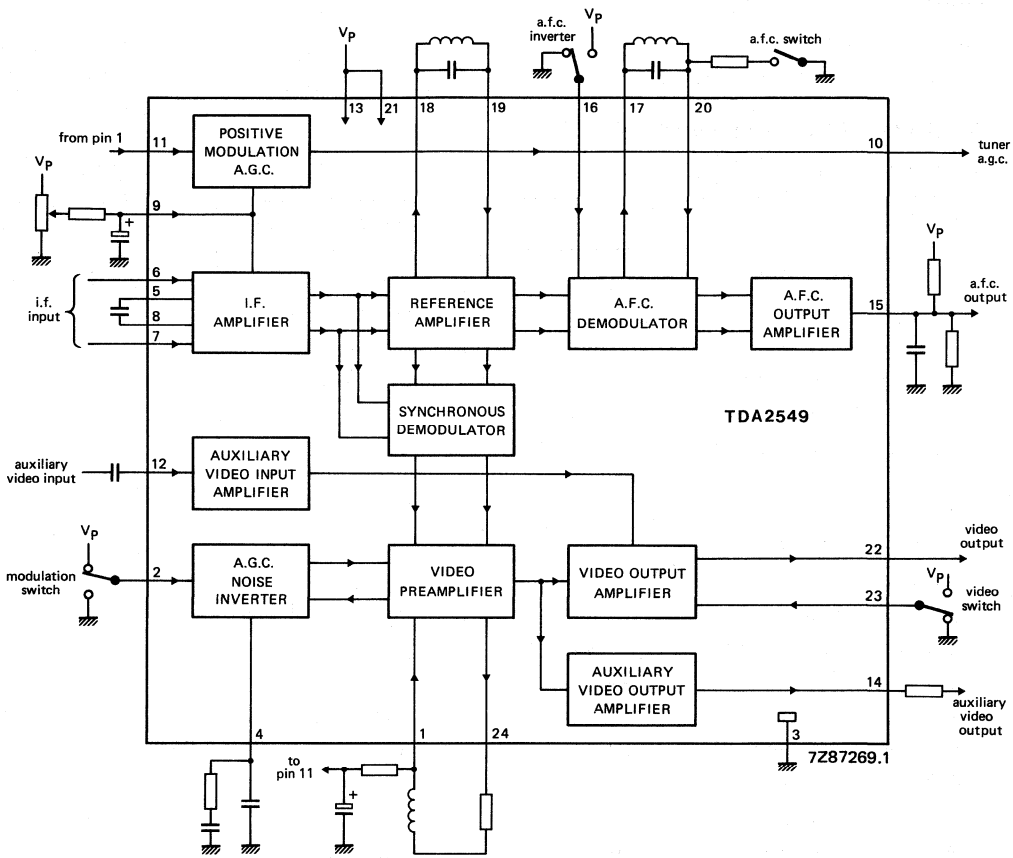


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 13 and 21)	V_P	13,8 V
Storage temperature range	T_{stg}	−25 to +125 °C
Operating ambient temperature range	T_{amb}	−25 to +70 °C

CHARACTERISTICS (measured in Fig. 5)

V_P = 12 V; T_{amb} = 25 °C

paramater	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	10,8	12	13,2	V
Supply current (pins 13 and 21)	I_P	–	82	–	mA
I.F. input signal for V_o = 2 V (between pins 6 and 7)	$V_i = V_{6-7}$	–	50	150	μV
Input impedance (differential)	$\lvert Z_{6-7} \rvert$	–	2	–	kΩ
Input capacitance (differential)	C_{6-7}	–	2	–	pF
Zero signal output level positive modulation	V_{22-3}	1,6	2	2,3	V
negative modulation	V_{22-3}	3,7	4	4,3	V
Top sync output level	V_{22-3}	1,7	2	2,3	V
Gain control range	G_v	50	74	–	dB
Signal-to-noise ratio at V_i = 10 mV (note 1)	S/N	50	57	–	dB
Maximum video output amplitude for positive modulation (peak-to-peak value)	$V_{22-3(p-p)}$	4,5	–	–	V
Bandwidth of video amplifier (3 dB)	B	–	5,5	–	MHz
Differential gain at V_o = 2 V	dG	–	4	10	%
Differential phase at V_o = 2 V	$d\varphi$	–	2	10	%
Residual carrier signal (r.m.s. value)	$V_{24-3(rms)}$	–	10	20	mV
Residual second harmonic of carrier signal (r.m.s. value)	$V_{24-3(rms)}$	–	20	60	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
A.F.C. output voltage swing	V_{15-3}	10	–	–	V
Change of frequency required for a.f.c. output voltage swing of 10 V	Δf	–	70	200	kHz
A.F.C. switch off for a voltage lower than:	V_{17-3}	–	–	1,5	V
A.F.C. inverter switch					
positive a.f.c. (Fig. 2)	V_{16-3}	0	–	1,5	V
negative a.f.c. (Fig. 3)	V_{16-3}	4	–	12	V
Tuner A.G.C.					
Leakage current	I_{10}	–	–	15	μA
Saturation voltage					
I_{10} = 0,3 mA	V_{10-3}	–	0,1	0,3	V
take-over point LOW	V_i	–	–	3	mV
take-over point HIGH	V_i	10	–	–	mV
Signal expansion at G_v = 50 dB	ΔV_{22-3}	–	–	0,5	dB
Negative modulation (Fig. 4)					
white spot inverter threshold level	V_{22-3}	–	4,6	–	V
white spot insertion level	V_{22-3}	–	3,2	–	V
noise inverter threshold level	V_{22-3}	–	0,9	–	V
noise insertion level	V_{22-3}	–	2,5	–	V
Positive modulation a.g.c. detector reference level	V_{11-3}	3,0	3,2	3,4	V
Auxiliary video input signal for $V_{o(p-p)}$ = 2 V	V_{12-3}	0,7	1	1,4	V
Auxiliary video output					
output signal (note 2)	V_{14-3}	–	1	–	V
top sync level	V_{14-3}	1	2	3	V
output impedance	$\lvert Z_{14-3} \rvert$	–	7	–	Ω
Levels for video switches					
positive video	V_{2-3}	–	–	1	V
negative video	V_{2-3}	3	–	–	V
internally demodulated signal	V_{23-3}	–	–	1	V
auxiliary video signal	V_{23-3}	3	–	–	V

Notes to the characteristics

1. Signal-to-noise ratio $S/N = \dfrac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.
2. Measured in application of Fig. 5.

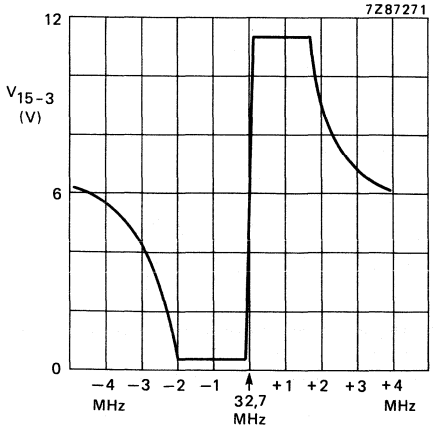


Fig. 2 A.F.C. output voltage V_{15-3} for positive a.f.c.

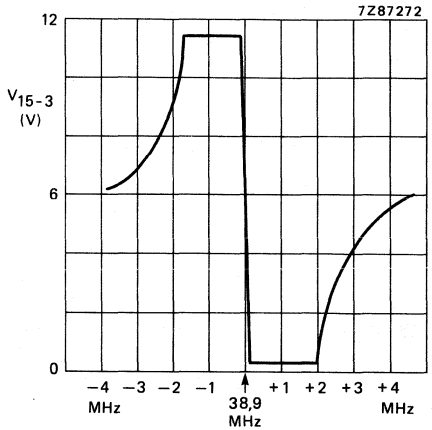


Fig. 3 A.F.C. output voltage V_{15-3} for negative a.f.c.

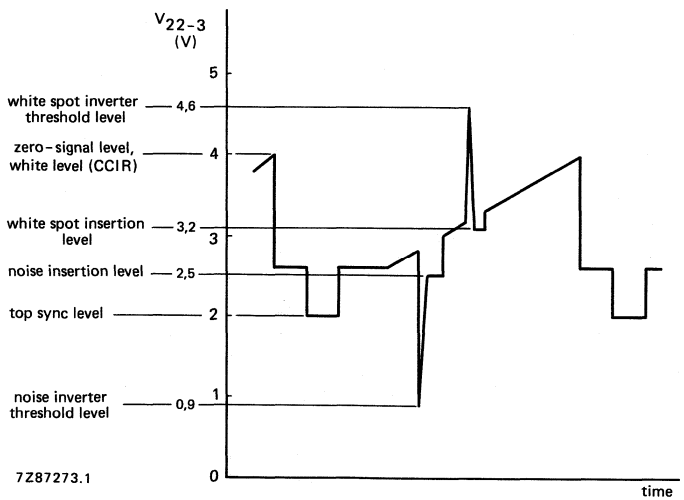


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

APPLICATION INFORMATION

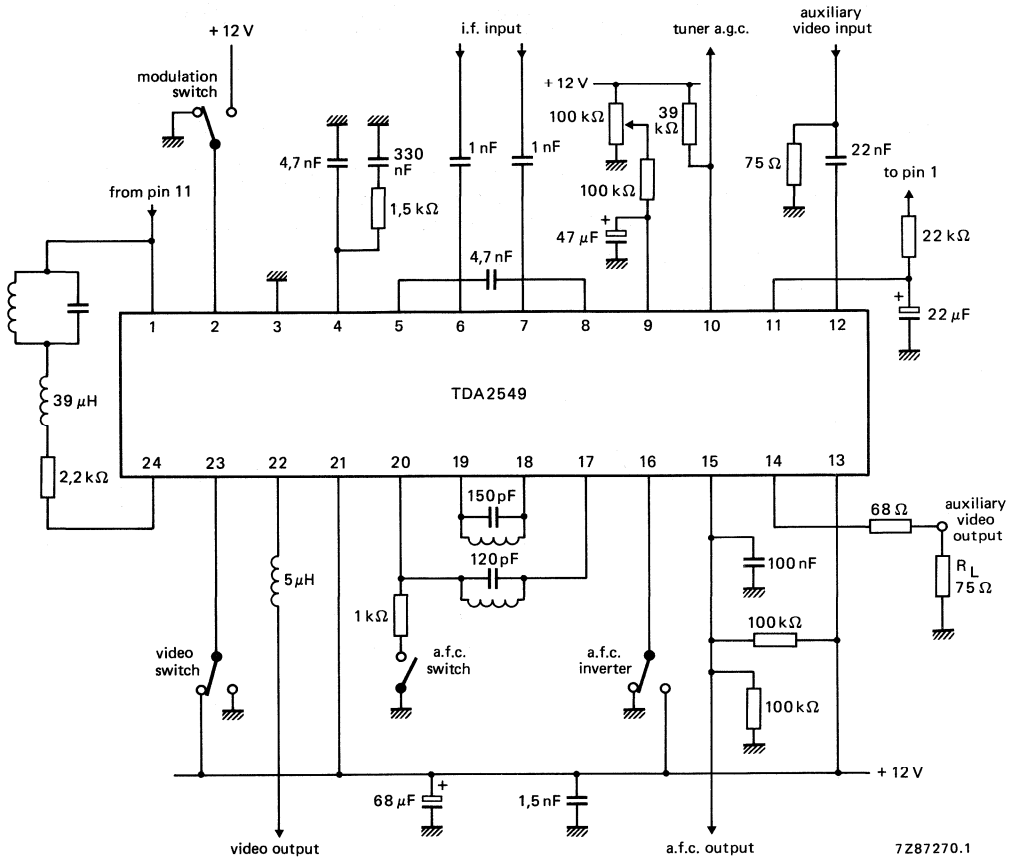


Fig. 5 Application diagram.

DUAL TV SOUND DEMODULATOR CIRCUITS

GENERAL DESCRIPTION

The circuits incorporate two FM demodulator systems to perform the demodulator functions required in a dual sound carrier TV system for demodulating the sound carriers.
The difference between TDA2555 and TDA2557 is the number of stages of the limiting amplifier.

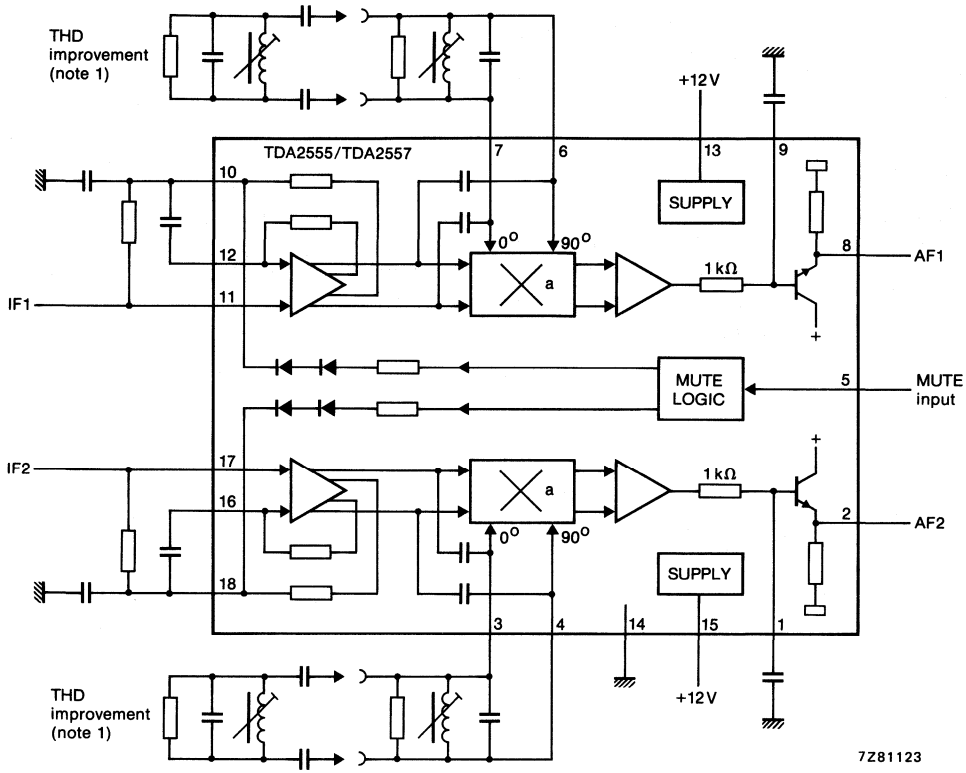
- **Eight** (TDA2555) or **five** (TDA2557) stage limiting amplifier
- Quadrature demodulator for FM detection
- De-emphasis stage
- Output amplifier
- Mute function for each FM demodulator

QUICK REFERENCE DATA

Supply voltage (pins 13 and 15)	V_P	typ.	12	V
Supply current (pins 13 and 15)	I_P	typ.	24,5	mA
AF output voltage (pins 2 and 8)	$V_{o(rms)}$	typ.	600	mV
Total harmonic distortion (note 1)	THD	<	0,1	%
Signal to weighted noise ratio	(S + N)/N	typ.	70	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



a = QUADRATURE DEMODULATOR

Fig. 1 Block diagram.
TDA2555 with 8-stage limiting amplifier;
TDA2557 with 5-stage limiting amplifier.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 13 and 15)	V_P	max.	13,2 V
Total power dissipation	P_{tot}	max.	400 mW
Storage temperature range	T_{stg}	−40 to + 150	°C
Operating ambient temperature	T_{amb}	0 to + 70	°C

CHARACTERISTICS

$V_P = V_{13,\,15\text{-}14} = 12$ V; $T_{amb} = 25$ °C; $f_{IF1} = 5{,}5$ MHz; $f_{IF2} = 5{,}74$ MHz; $f_{m1} = 1$ kHz;
$\Delta f = \pm 30$ kHz;
$V_{i(rms)} = 5$ mV for TDA2555;
$V_{i(rms)} = 10$ mV for TDA2557;
see test circuit Fig. 3, voltages with respect to ground (pin 14), unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Total current consumption	$I_{13,15}$	18	24,5	30	mA
LIMITING AMPLIFIER					
Maximum input voltage	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	200	–	mV
Input voltage for start of limiting (3 dB AF signal reduction)					
TDA2555	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	50	100	μV
TDA2557	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	250	500	μV
DC voltage (input limiting amplifier) pins 11, 12, 16, 17 to 14	V_i	–	2,0	–	V
DC voltage (feedback loop)	$V_{10,18\text{-}14}$	–	2,0	–	V
FM DEMODULATOR					
IF reference signal voltage	$V_{3\text{-}4(rms)}$ $V_{6\text{-}7(rms)}$	–	200	–	mV
DC voltage	$V_{3,4,6,7\text{-}14}$	–	3,1	–	V
AF output voltage	$V_{2\text{-}14(rms)}$	450	600	750	mV
Difference of output signals	$\frac{V_{2\text{-}14}}{V_{8\text{-}14}}$	–	± 0,1	± 0,5	dB
Total harmonic distortion at outputs AF1 and AF2 (note 1)	THD	–	–	0,5	%
A.M. suppression at outputs AF1 and AF2, $f_{FM} = 70$ Hz; $\Delta f = \pm 50$ kHz; $f_{AM} = 1$ kHz; m = 0,3	AMS	50	–	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
FM DEMODULATOR (continued)					
Signal to noise ratio at outputs AF1 and AF2 (CCIR weighted, quasi peak)	$(S+N)/N$	65	70	–	dB
Residual IF-signal without deemphasis	$V_{2,8\text{-}14(rms)}$	–	30	–	mV
Ripple rejection at outputs AF1 and AF2 f = 50 Hz to 20 kHz; $V_{i(rms)}$ = 200 mV	RR	–	40	–	dB
AUDIO OUTPUT STAGE					
emitter follower with 1,0 mA bias current					
DC output voltage	$V_{2,8\text{-}14}$	3,0	4,0	5,0	V
External DC load resistance	$R_{2,8\text{-}14}$	2	–	–	kΩ
AC output current (note 2)	$-I_{2,8\text{-}14(p\text{-}p)}$	–	–	0,5	mA
Deemphasis input resistance (note 3)	$R_{1,9\text{-}14}$	0,8	1,0	1,2	kΩ
DC voltage (deemphasis)	$V_{1,9\text{-}14}$	3,7	4,7	5,7	V
Crosstalk attenuation f = 1 kHz (note 4)	$\alpha_{12,21}$	60	–	–	dB
Crosstalk attenuation f = 10 kHz (note 4)	$\alpha_{12,21}$	60	–	–	dB
Output impedance	$R_{2,8\text{-}14}$	–	25	–	Ω
AF output level (Fig. 2, note 5) MUTE function $V_{i(rms)} < 60$ mV	α	60	–	–	dB
Switching input current					
$V_{5\text{-}14} = 0$ V	$-I_5$	–	–	500	μA
$V_{5\text{-}14} = V_P$	I_5	–	–	500	μA
Internal d.c. voltage no mute (pin 5 not connected)	$V_{5\text{-}14}$	–	6,2	–	V

Notes to the characteristics

1. THD < 0,1% requires a double tuned demodulator circuit (Q_L = 20). With a single tuned circuit a THD of < 0,5% is possible (see Figs 1 and 3).
2. If higher a.c. output current is required an external resistor must be applied from output (pins 2 and 8) to ground (min. 2 kΩ) in order to improve the THD performance ($-I_{2,8} < 4$ mA).
3. The deemphasis time constant is 50 μs.
4. Crosstalk attenuation is defined as:

$$o_{12} = \frac{V_{2\text{-}14 \text{ unmodulated}}}{V_{8\text{-}14}} \qquad o_{21} = \frac{V_{8\text{-}14 \text{ unmodulated}}}{V_{2\text{-}14}}.$$

5. In the MUTE state the a.f. output level attenuation is more than 60 dB. The MUTE function is only guaranteed for an r.m.s. value of the input voltage lower than 60 mV. See also Fig. 2.

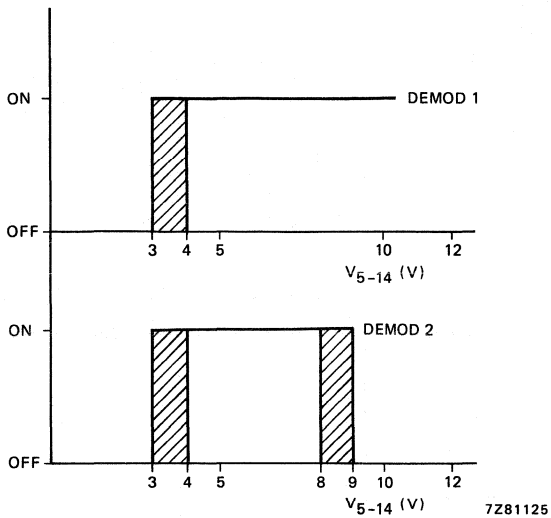


Fig. 2 Mute function.

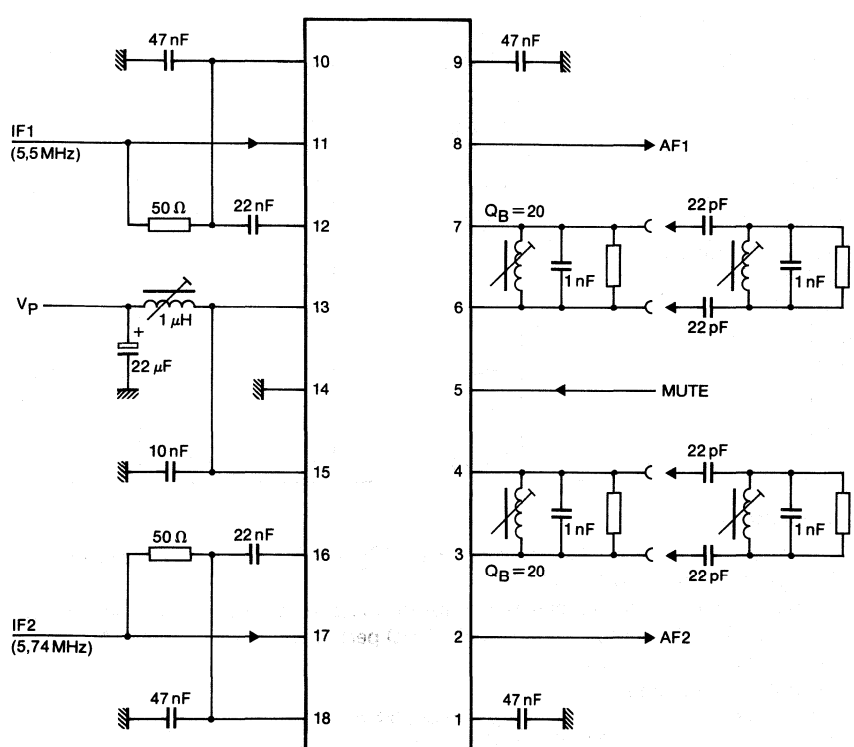


Fig. 3 Test and application circuit.

SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

GENERAL DESCRIPTION

The TDA2577A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector ($\varphi 2$) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 3% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical comparator with internal 3% pre-correction circuit for vertical oscillator/sawtooth generator
- Vertical driver stage
- Vertical blanking pulse generator with external adjustment of pulse duration (50 Hz: 21 lines; 60Hz: 17 lines)
- Vertical guard circuit

QUICK REFERENCE DATA

Supply			
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4,5 mA
Main supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
Supply current	$I_P = I_{10}$	typ.	55 mA
Input signals			
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5-9(p-p)}$	0,15 to 1	V
Output signals			
Horizontal output pulse (open collector) at I_{11} = 40 mA	V_{11-9}	<	0,5 V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	V_{1-9}	>	4 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

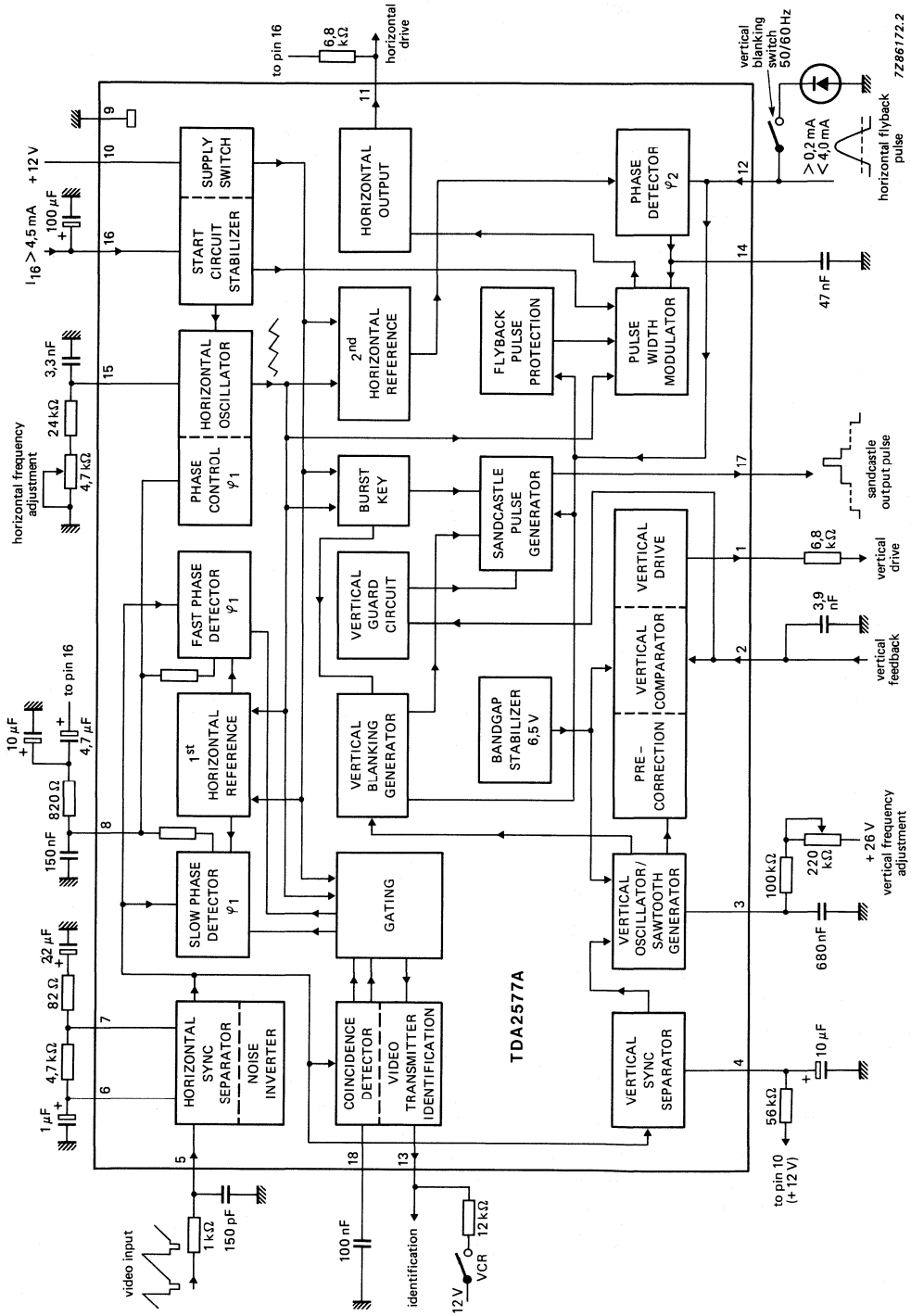


Fig. 1 Block diagram.

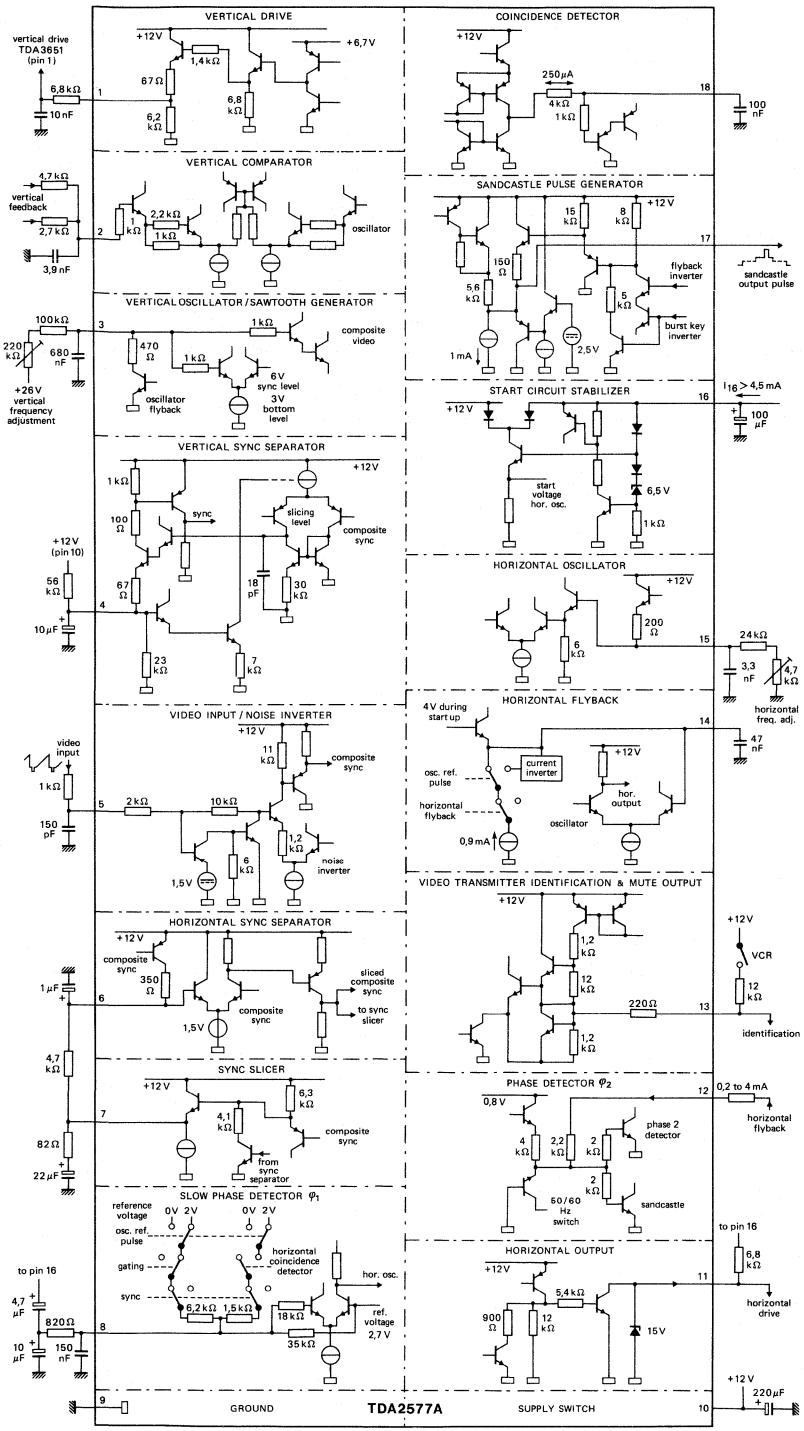


Fig. 2 TDA2577A circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	typ.	50	K/W

CHARACTERISTICS

I_{16} = 5 mA; V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}		4,5 to 8	mA
Stabilized supply voltage (pin 16)	V_{16-9}	typ.	8,7	V
			8,0 to 9,5	V
Supply current (pin 10)	I_{10}	typ.	55	mA
		<	70	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12	V
			10 to 13,2	V

Video input (pin 5)

Top-sync level	V_{5-9}	typ.	3,1	V
			1,5 to 3,75	V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5-9(p-p)}$	typ.	0,6	V
			0,15 to 1	V
Slicing level		typ.	50	%
			35 to 65	%
Delay between video input and detector output	t_1	typ.	0,35	μs

Noise gate (pin 5)

Switching level	V_{5-9}	typ.	0,7	V
		<	1	V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ.	± 800	Hz
Catching range	Δf	typ.	± 800	Hz
			±600 to ±1100	Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse				
for slow time constant		typ.	1	kHz/μs
for fast time constant		typ.	2,75	kHz/μs

Second control loop (horizontal output to flyback; pin 14)				
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400	$\mu s/\mu s$
Control range	t_d		1 to 50	μs
Controlled edge	negative			
Phase adjustment (via 2nd control loop; pin 14)				
Control sensitivity		typ.	25	$\mu A/\mu s$
Maximum permissible control current	$\pm I_{14}$	<	60	μA
Horizontal oscillator (pin 15)				
Frequency (no sync)	f_{osc}	typ.	15 625	Hz
Frequency spread (C_{osc} = 3,3 nF; R_{osc} = 24 kΩ)	Δf_{osc}	<	4	%
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. <	6 8	% %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}
Horizontal output (pin 11)				
Output voltage; high level	$V_{11\text{-}9}$	<	13,2	V
Voltage at which protection starts	$V_{11\text{-}9}$		13 to 15,8	V
Output voltage; low level start condition at I_{11} = 10 mA	$V_{11\text{-}9}$	typ. <	0,3 0,5	V V
normal condition at I_{11} = 40 mA	$V_{11\text{-}9}$	typ. <	0,3 0,5	V V
Duty factor of output signal during starting (no phase shift; voltage at pin 11 low)	δ	typ.	65	%
Duty factor of output signal without flyback pulse	δ	typ. 	50 47 to 57	% %
Controlled edge	negative			
Duration of output pulse (see Fig. 3)			$t_d + t_o + 2{,}5$	μs
Sandcastle output pulse (pin 17)				
Output voltage during: burst key	$V_{17\text{-}9}$	>	10	V
horizontal blanking	$V_{17\text{-}9}$	typ. 	4,6 4,2 to 5	V V
vertical blanking	$V_{17\text{-}9}$	typ. 	2,5 2 to 3	V V
Pulse duration				
burst key	t_p	typ. 	3,7 3,3 to 4,1	μs μs
horizontal blanking	flyback pulse (see note 3)			
vertical blanking for 50 Hz application ($-I_{12}$: 0 to 0,1 mA) for 60 Hz application ($-I_{12}$: typ. 0,2 mA)			21 17	lines lines

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ.	5,2 μs
			4,8 to 5,6 μs
Delay between the start of the sync and the trailing edge of the burst key	t_2	typ.	8,8 μs
			8,1 to 9,3 μs
Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 2			
Detector output current	$\pm I_{18}$	typ.	300 μA
Voltage during noise (note 4)	V_{18-9}	typ.	0,3 V
Voltage level for in-sync condition	V_{18-9}	typ.	7,5 V
Switching level slow to fast	V_{18-9}	typ.	3,5 V
			3,2 to 3,8 V
Switching level mute function active; φ_1 fast to slow	V_{18-9}	typ.	1,2 V
			1,0 to 1,4 V
vertical period counter 3 periods fast	V_{18-9}	typ.	0,12 V
			0,08 to 0,16 V
Switching level slow to fast (locking) mute function inactive	V_{18-9}	typ.	1,7 V
			1,5 to 1,9 V
Switching level fast to slow (locking)	V_{18-9}	typ.	5,0 V
			4,7 to 5,3 V
Switching level for VCR (fast time constant) without mute function	V_{18-9}	typ.	8,6 V
			8,2 to 9,0 V
Video transmitter identification output (pin 13)			
Output voltage active (no sync) at I_{13} = 1 mA	V_{13-9}	>	10 V
		typ.	11 V
Output voltage active (no sync) at I_{13} = 5 mA	V_{13-9}	>	7 V
		typ.	10 V
Output voltage inactive	V_{13-9}	<	0,5 V
		typ.	0,1 V
VCR switching (pin 13)			
Input current for fast time constant phase detector φ_1, with mute function active	I_{13}	typ.	0,6 mA
			0,4 to 0,8 mA
Flyback input pulse (pin 12)			
Switching level	V_{12-9}	typ.	1 V
Input current	I_{12}		0,2 to 4 mA
Input pulse amplitude (peak-to-peak value)	$V_{12-9(p-p)}$	<	12 V
Input resistance	R_{12-9}	typ.	2,7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; t_{fl} = 12 μs (see also note 2 and Fig. 4)	t_o	typ.	1,3 μs

Duration of vertical blanking pulse (pin 12)

Required input current (negative)			
for 50 Hz application; 21 lines blanking	$-I_{12}$	typ.	0,2 mA
		$>0,15$ to $<0,3$	mA
for 60 Hz application; 17 lines blanking	$-I_{12}$	$<$	0,1 mA
Maximum allowed input current	$-I_{12}$	$<$	0,4 mA

Vertical sawtooth generator (pin 3)

Vertical frequency (no sync)	f_s	typ.	46 Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 187 kΩ; at + 26 V)	Δf_s	$<$	4 %
Synchronization range		typ.	22 %
Input current at V_{3-9} = 6 V	I_3	$<$	2 μA
Frequency shift for V_P = 10 to 13 V	Δf_s	$<$	0,2 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}

Comparator (pin 2)

Input voltage; d.c. level	V_{2-9}	typ.	4,4 V
		4,0 to 4,8	V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	1,5 V
Input current at V_{2-9} = 6 V	I_2	$<$	2 μA
Sawtooth internal pre-correction (parabolic convex)		typ.	3 %

Vertical output stage; emitter follower (pin 1)

Output voltage at I_1 = 10 mA	V_{1-9}	typ.	3,6 V
		3,2 to 5	V
Output current	I_1	$<$	20 mA

Vertical guard circuit

Activating voltage levels (vertical blanking level is 2,5 V)

switching level low	V_{2-9}	typ.	3 V
		2,7 to 3,3	V
switching level high	V_{2-9}	typ.	5,8 V
		5,4 to 6,3	V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between negative transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.

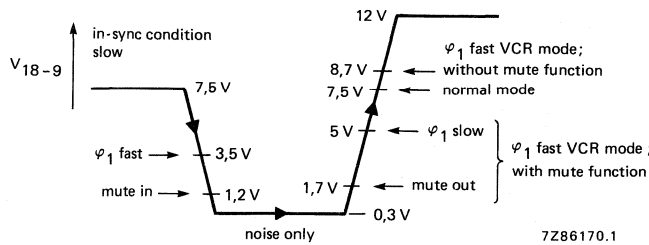


Fig. 3 Voltage levels at pin 18 (V_{18-9}).

APPLICATION INFORMATION

The TDA2577A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4{,}5$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the negative-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking interval of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

APPLICATION INFORMATION (continued)

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector φ_1				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7,5 V	X		X			X	video signal detected
7,5 to 3,5 V	X		X			X	video signal detected
3,5 to 1,2 V		X		X		X	video signal detected
1,2 to 0,1 V	X		X		X		noise only
0,1 to 1,7 V	X	*	X	*	X		new video signal detected
1,7 to 5,0 V		X		X		X	horizontal oscillator locked VCR playback with mute function
5,0 to 7,5 V	X		X			X	horizontal oscillator locked
8,7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground. Also a current of 0,6 mA into pin 13 sets the first phase detector to fast without affecting the mute output function (active HIGH with no video signal detected). For VCR playback without mute function, the first phase detector can be set to fast by connecting a resistor of 1 kΩ to the supply (pin 10).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 3,8 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4{,}5$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays

in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally precorrected by 3% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,5 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration is set by the negative voltage value of the horizontal flyback pulse at pin 12.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3 V or higher than 5,8 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

APPLICATION INFORMATION (continued)

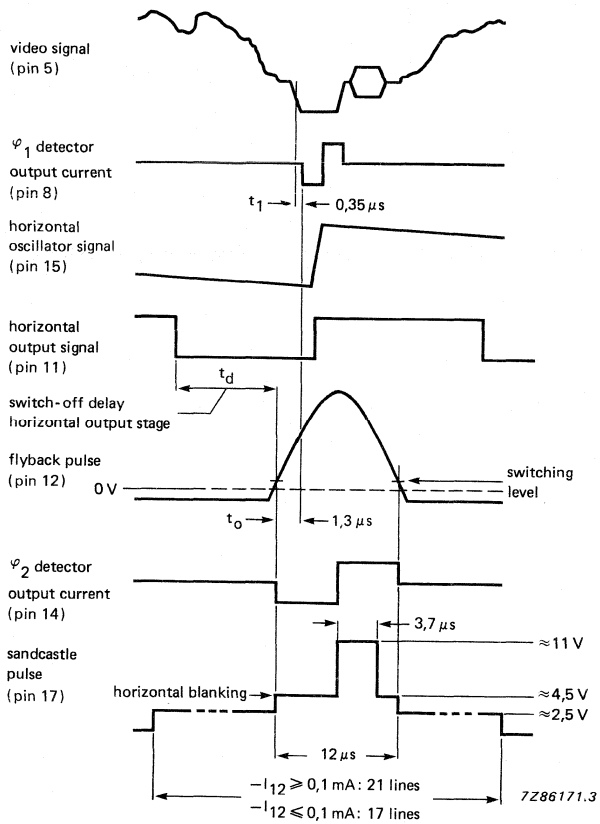


Fig. 4 Timing diagram of the TDA2577A.

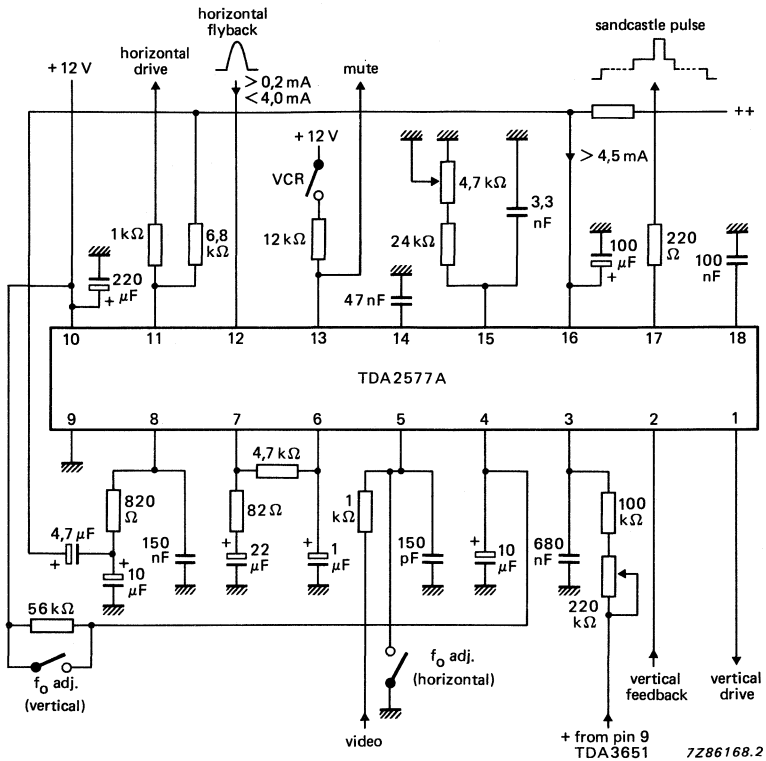


Fig. 5 Typical application circuit diagram; for combination of the TDA2577A with the TDA3651 see Fig. 7.

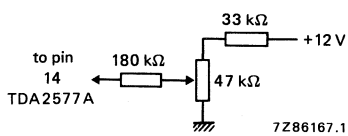


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

APPLICATION INFORMATION (continued)

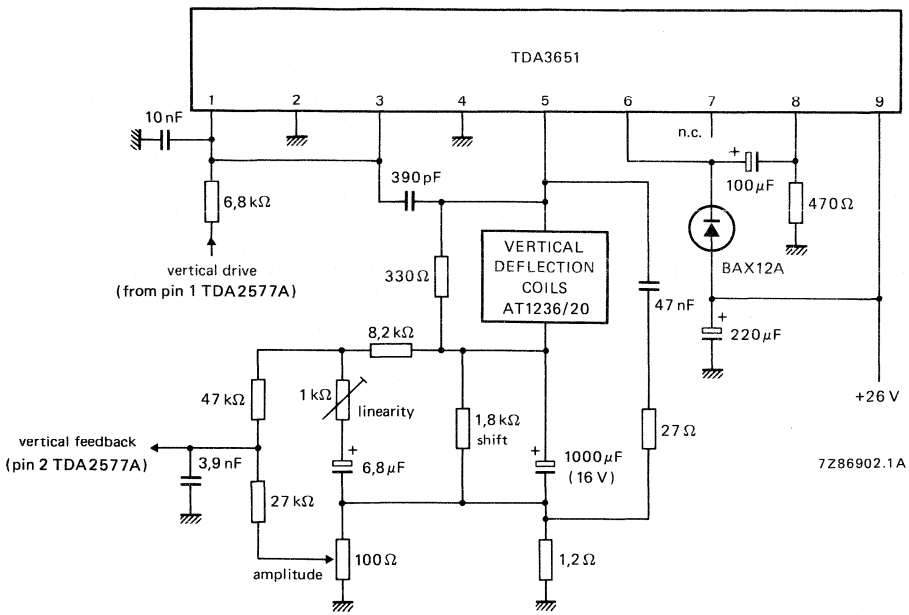


Fig. 7 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2577A (90° application).

SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

GENERAL DESCRIPTION

The TDA2578A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector (φ_2) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 6% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical driver stage
- Vertical blanking pulse generator
- 50/60 Hz detector
- 50/60 Hz identification output
- Automatic amplitude adjustment for 60 Hz
- Automatic adjustment of blanking pulse duration (50 Hz: 21 lines; 60 Hz: 17 lines)
- Vertical guard curcuit

QUICK REFERENCE DATA

Supply			
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4,5 mA
Main supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
Supply current	$I_P = I_{10}$	typ.	55 mA
Input signals			
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5-9(p-p)}$		0,15 to 1 V
Output signals			
Horizontal output pulse (open collector) at I_{11} = 40 mA	V_{11-9}	<	0,5 V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	V_{1-9}	>	4 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

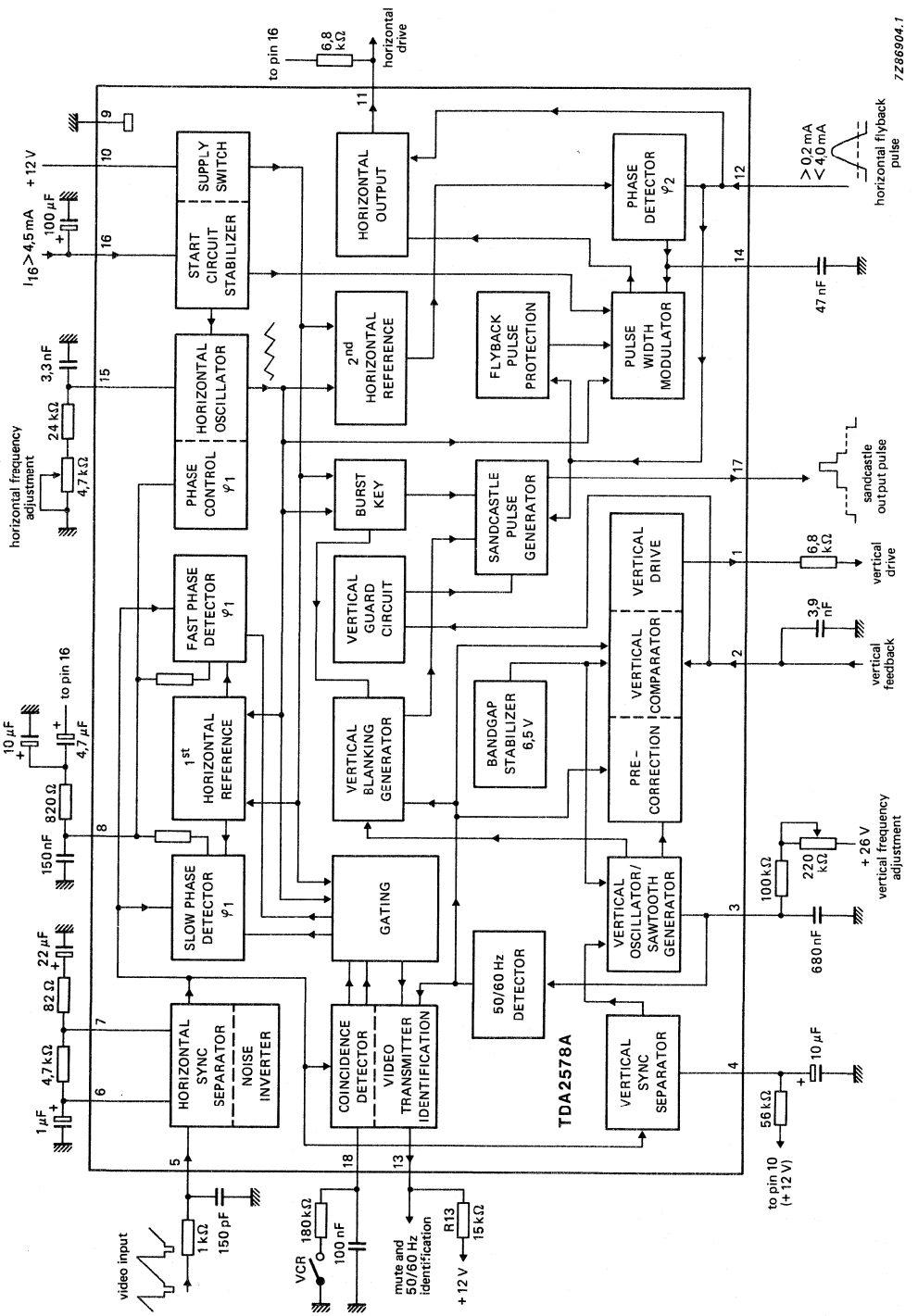


Fig. 1 Block diagram.

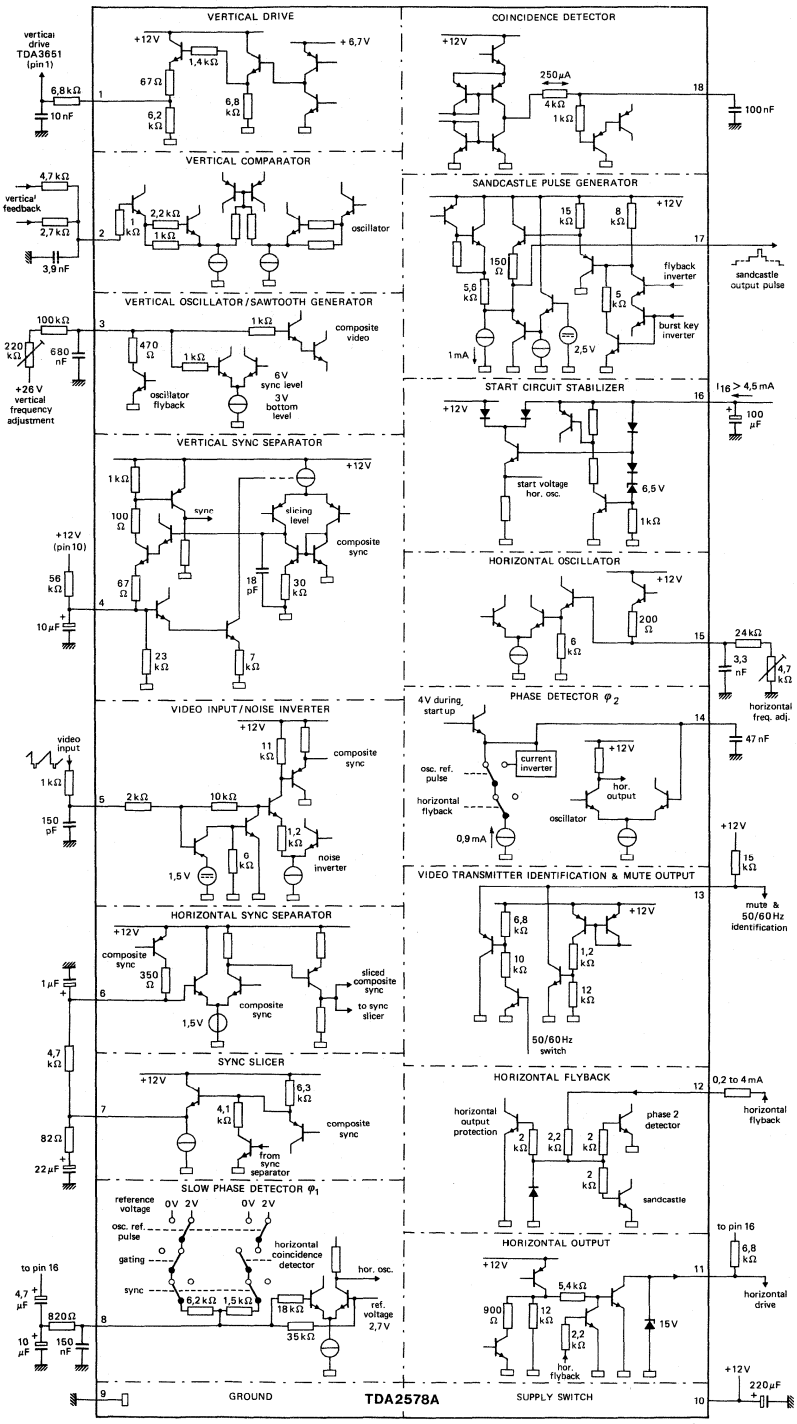


Fig. 2 TDA2578A circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−25 to	+65	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	typ.	50	K/W

CHARACTERISTICS

I_{16} = 5 mA; V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}		4,5 to 8	mA
Stabilized supply voltage (pin 16)	V_{16-9}	typ.	8,7	V
			8,0 to 9,5	V
Supply current (pin 10)	I_{10}	typ.	55	mA
		<	70	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12	V
			10 to 13,2	V

Video input (pin 5)

Top-sync level	V_{5-9}	typ.	3,1	V
			1,5 to 3,75	V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5-9(p-p)}$	typ.	0,6	V
			0,15 to 1	V
Slicing level		typ.	50	%
			35 to 65	%
Delay between video input and detector output	t_1	typ.	0,35	μs

Noise gate (pin 5)

Switching level	V_{5-9}	typ.	0,7	V
		<	1	V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ.	± 800	Hz
Catching range	Δf	typ.	± 800	Hz
			±600 to ±1100	Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse				
for slow time constant		typ.	1	kHz/μs
for fast time constant		typ.	2,75	kHz/μs

Second control loop (horizontal output to flyback; pin 14)				
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400	$\mu s/\mu s$
Control range	t_d		1 to 45	μs
Controlled edge	positive			
Phase adjustment (via 2nd control loop; pin 14)				
Control sensitivity		typ.	25	$\mu A/\mu s$
Maximum permissible control current	$\pm I_{14}$	<	60	μA
Horizontal oscillator (pin 15)				
Frequency (no sync)	f_{osc}	typ.	15 625	Hz
Frequency spread (C_{osc} = 3,3 nF; R_{osc} = 24 kΩ; no sync)	Δf_{osc}	<	4	%
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. <	6 8	% %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}
Horizontal output (pin 11)				
Output voltage; high level	V_{11-9}	<	13,2	V
Voltage at which protection starts	V_{11-9}		13 to 15,8	V
Output voltage; low level start condition at I_{11} = 10 mA	V_{11-9}	typ. <	0,3 0,5	V V
normal condition at I_{11} = 40 mA	V_{11-9}	typ. <	0,3 0,5	V V
Duty factor of output signal during starting (no phase shift) I_{16} = 4 mA (voltage at pin 11 low)	δ	typ.	65	%
Duty factor of output signal without flyback pulse	δ	typ. 	50 45 to 55	% %
Controlled edge	positive			
Duration of output pulse (see Fig. 4)	t_d + horizontal flyback pulse			
Sandcastle output pulse (pin 17)				
Output voltage during:				
burst key	V_{17-9}	>	10	V
horizontal blanking	V_{17-9}	typ. 	4,6 4,2 to 5	V V
vertical blanking	V_{17-9}	typ. 	2,5 2 to 3	V V
Pulse duration				
burst key	t_p	typ. 	3,7 3,3 to 4,1	μs μs
horizontal blanking	flyback pulse (see note 3)			
vertical blanking				
at 50 Hz	21 lines			
at 60 Hz	17 lines			

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ.	5,2 μs
			4,8 to 5,6 μs
Delay between start of sync and trailing edge of burst key	t_2	typ.	8,8 μs
			8,1 to 9,3 μs
Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 3			
Detector output current	$\pm I_{18}$	typ.	300 μA
Voltage during noise (note 4)	V_{18-9}	typ.	0,3 V
Voltage level for in-sync condition	V_{18-9}	typ.	7,5 V
Switching level slow to fast	V_{18-9}	typ.	3,5 V
			3,2 to 3,8 V
Switching level mute function active; φ_1 fast to slow	V_{18-9}	typ.	1,2 V
			1,0 to 1,4 V
vertical period counter 3 periods fast	V_{18-9}	typ.	0,12 V
			0,08 to 0,16 V
Switching level slow to fast (locking) mute function inactive	V_{18-9}	typ.	1,7 V
			1,5 to 1,9 V
Switching level fast to slow (locking)	V_{18-9}	typ.	5,0 V
			4,7 to 5,3 V
Switching level for VCR (fast time constant) without mute function	V_{18-9}	typ.	8,6 V
			8,2 to 9,0 V
Video transmitter identification output (pin 13)			
Output voltage active (no sync) at I_{13} = 1 mA	V_{13-9}	<	0,5 V
		typ.	0,3 V
Sink current active (no sync)	I_{13}	⩽	5 mA
Output current inactive (sync: 50 Hz)	I_{13}	<	1 μA
50/60 Hz identification (pin 13)			
R13 = 15 kΩ to + 12 V (note 5) at f = 50 Hz (in sync condition)	V_{13-9}	typ.	V_{10-9} V
at f = 60 Hz (in sync condition)	V_{13-9}	typ.	7,6 V
			7,2 to 8 V
Flyback input pulse (pin 12)			
Switching level	V_{12-9}	typ.	1 V
Input current	I_{12}		0,2 to 4 mA
Input pulse amplitude (peak-to-peak value)	$V_{12-9(p-p)}$	<	12 V
Input resistance	R_{12-9}	typ.	2,7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; t_{fl} = 12 μs (see also note 2 and Fig. 4)	t_o	typ.	1,3 μs

Vertical sawtooth generator (pin 3)

Vertical frequency (no sync)	f_s	typ.	46 Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 187 kΩ; at + 26 V)	Δf_s	<	4 %
Synchronization range (note 6)		typ.	33 %
Input current at V_{3-9} = 6 V	I_3	<	3 μA
Frequency shift for V_P = 10 to 13 V	Δf_s	<	0,2 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}

Comparator (pin 2)

Input voltage; d.c. level	V_{2-9}	typ.	4,4 V
			4,0 to 4,8 V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	0,8 V
Input current at V_{2-9} = 6 V	I_2	<	2 μA
Sawtooth internal pre-correction (parabolic convex)		typ.	6 %

Vertical output stage; emitter follower (pin 1)

Output voltage at I_1 = 10 mA	V_{1-9}	typ.	3,6 V
			3,2 to 5 V
Output current	I_1	<	20 mA

Vertical guard circuit

Activating voltage levels (vertical blanking level is 2,5 V)			
switching level low	V_{2-9}	typ.	3,35 V
			3,0 to 3,7 V
switching level high	V_{2-9}	typ.	5,15 V
			4,75 to 5,55 V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.
5. For 60 Hz a p-n-p emitter clamp is activated.
6. When f_o = 46 Hz the 50/60 Hz detector switches over to 60 Hz; video input signal at pin 5 ≈ 55 Hz.

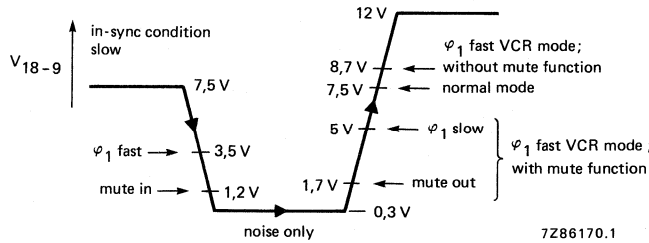


Fig. 3 Voltage levels at pin 18 (V_{18-9}).

APPLICATION INFORMATION

The TDA2578A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4{,}5$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the positive-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking internal of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector φ_1				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7,5 V	X		X			X	video signal detected
7,5 to 3,5 V	X		X			X	video signal detected
3,5 to 1,2 V		X		X		X	video signal detected
1,2 to 0,1 V	X		X		X		noise only
0,1 to 1,7 V	X	*	X	*	X		new video signal detected
1,7 to 5,0 V		X		X		X	horizontal oscillator locked VCR playback with mute function
5,0 to 7,5 V	X		X			X	horizontal oscillator locked
8,7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

APPLICATION INFORMATION (continued)

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground (see Fig. 7).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 4,2 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4,5$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally pre-corrected by 6% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,7 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration and sawtooth amplitude is automatically adjusted via the 50/60 Hz detector.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3,35 V or higher than 5,15 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

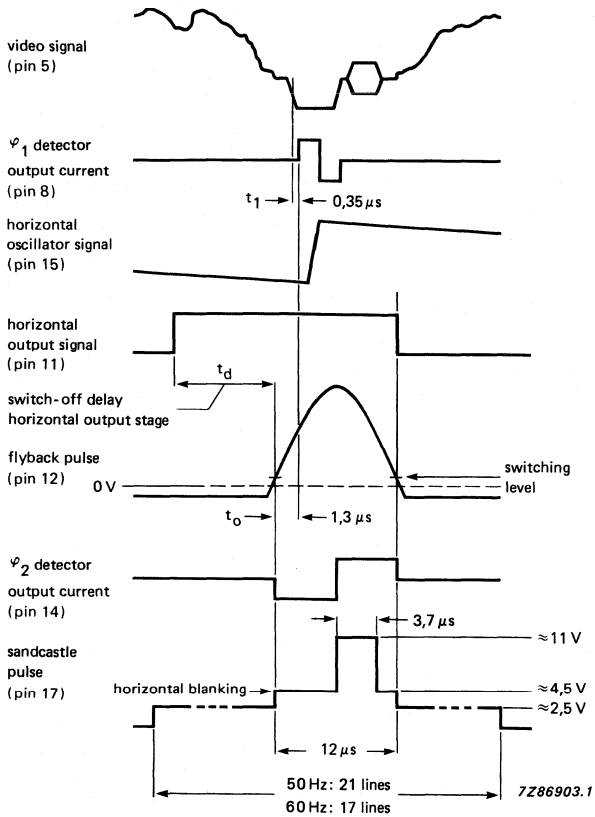
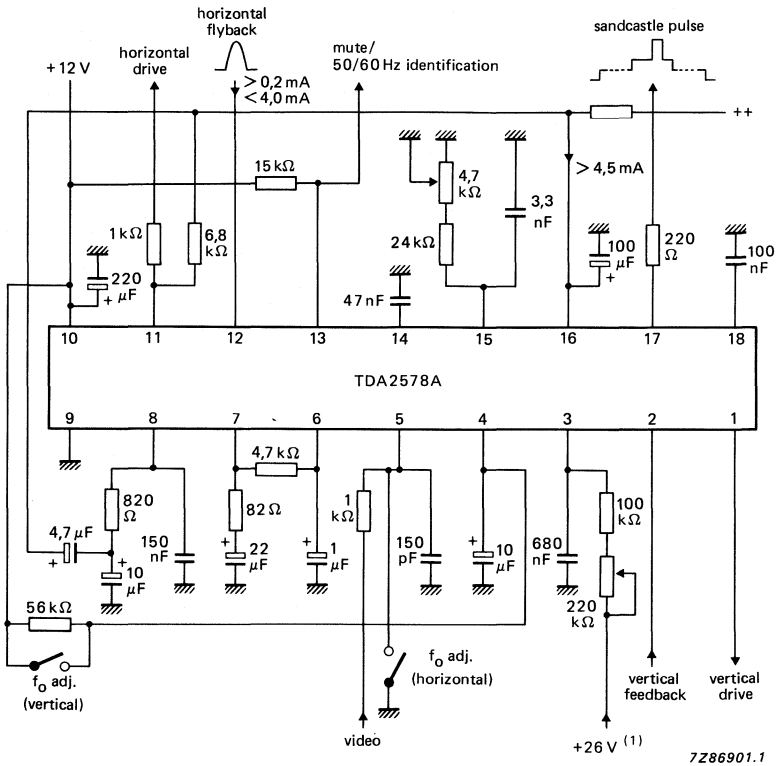


Fig. 4 Timing diagram of the TDA2578A.

APPLICATION INFORMATION (continued)



(1) ⩾ 26 V for linear scan.

Fig. 5 Typical application circuit diagram; for application of the TDA2578A with the TDA3651 see Fig. 8.

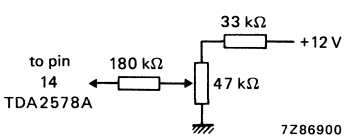


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

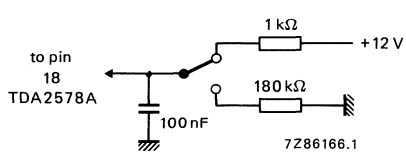


Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
180 kΩ between pin 18 and ground: with mute function.

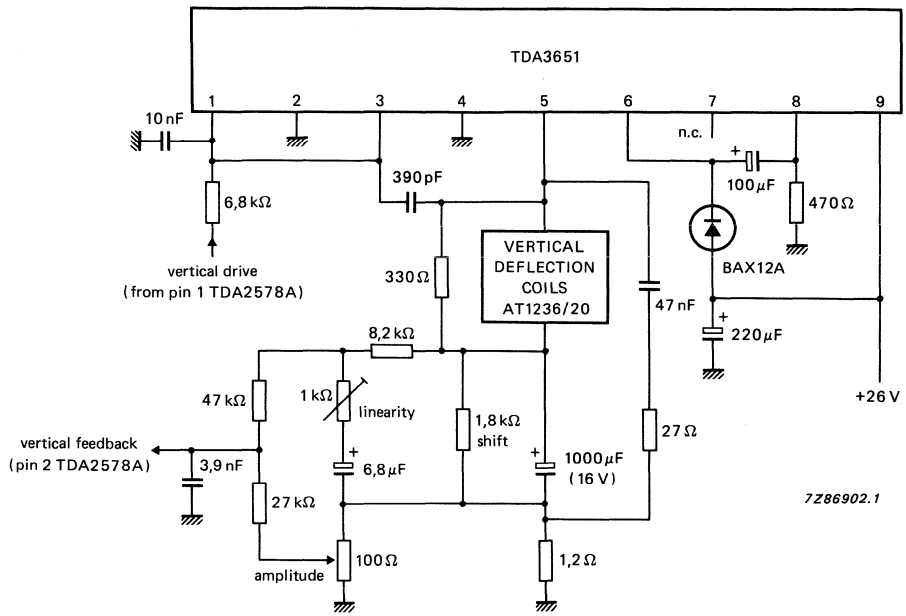


Fig. 8 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2578A, (90° application).

HORIZONTAL/VERTICAL SYNCHRONIZATION CIRCUIT

GENERAL DESCRIPTION

The TDA2579B generates and synchronizes horizontal and vertical signals. The device has a 3 level sandcastle output; a transmitter identification signal and also 50/60 Hz identification.

Features

- Horizontal phase detector, (sync to oscillator), sync separator and noise inverter
- Triple current source in the phase detector with automatic selection
- Second phase detector for storage compensation of the horizontal output
- Stabilized direct starting of the horizontal oscillator and output stage from mains supply
- Horizontal output pulse with constant duty cycle value of 29 μs
- Internal vertical sync separator, and two integration selection times
- Divider system with three different reset enable windows
- Synchronization is set to 628 divider ratio when no vertical sync pulses and no video transmitter is identified
- Vertical comparator with a low DC feedback signal
- 50/60 Hz identification output combined with mute function
- Automatic amplitude adjustment for 50 and 60 Hz and blanking pulse duration
- Automatic adaption of the burst-key pulsewidth

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply						
Minimum required current for starting horizontal oscillator and output stage		I_{16}	6.2	–	–	mA
Main supply voltage		V_{10}	–	12	–	V
Supply current		I_{10}	–	70	–	mA
Input signals						
Sync pulse input amplitude		$V_{5(p-p)}$	0.05	–	1.0	V
Horizontal flyback pulse input current		I_{12}	–	1	–	mA
Vertical comparator input signal						
Voltage AC		V_2	–	0.8	–	V
Voltage DC		V_2	–	1	–	V
Output signals						
Horizontal output (open collector) I_{11} = 25 mA		V_{11}	–	–	0.5	V
Vertical output stage driver (emitter follower) I_1 = 1.5 mA		V_1	5	–	–	V
Sandcastle output levels						
V_{17} burst-key		V_{17}	9.8	–	–	V
horizontal blanking		V_{17}	–	4.5	–	V
vertical blanking		V_{17}	–	2.5	–	V
Video transmitter identification output stage (open collector loaded with external resistor to positive supply). No sync. pulse present		V_{13}	–	–	0.5	V
		I_{13}	–	–	5	mA
Sync pulse present						
divider ratio > 576		V_{13}	–	V_{10}	–	V
divider ratio < 576		V_{13}	–	7.65	–	V

PACKAGE OUTLINE

18-lead dual in line; plastic (SOT102).

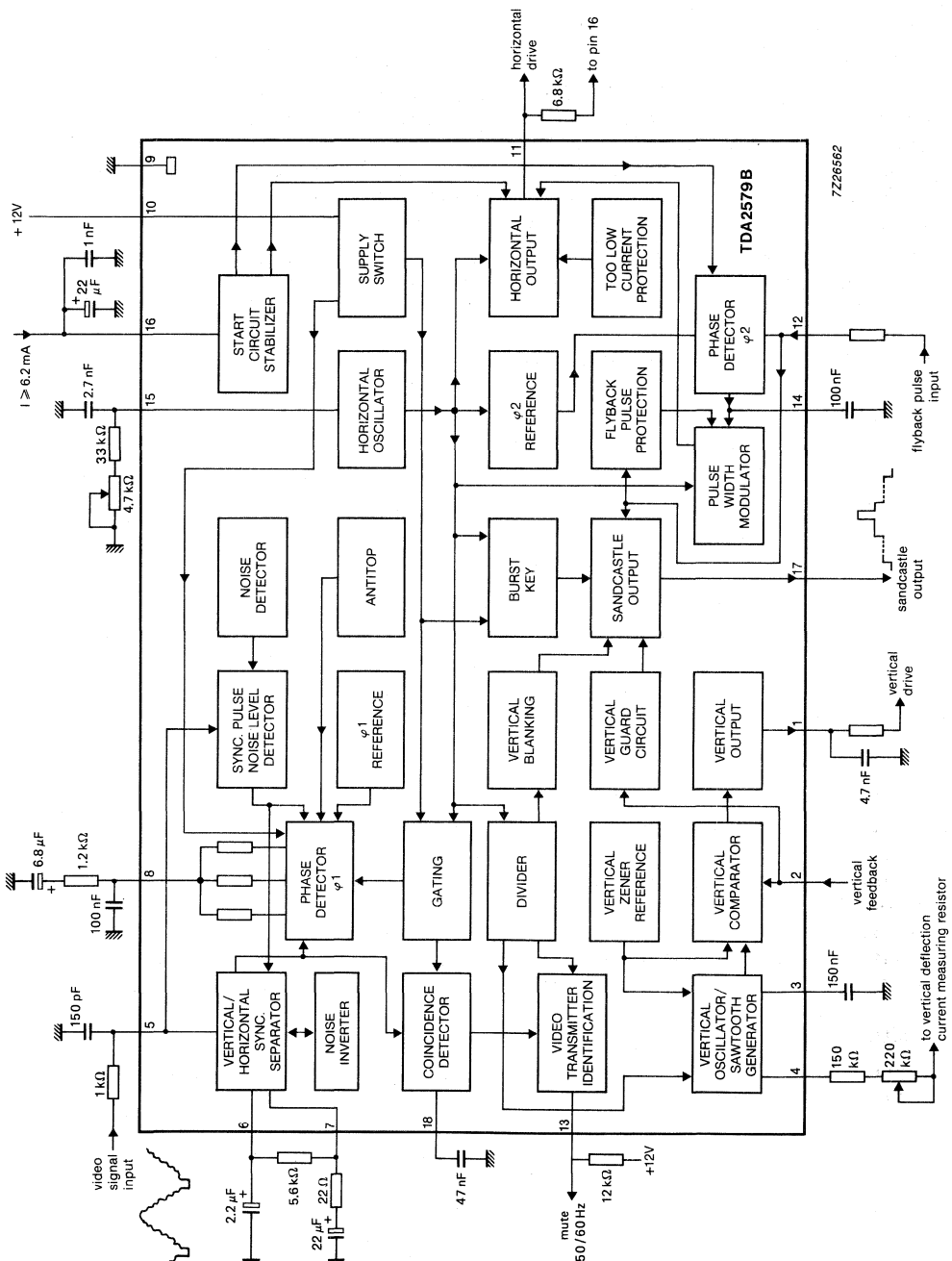


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Vertical part (pins 1,2,3,4)

The IC embodies a synchronized divider system for generating the vertical sawtooth at pin 3. The divider system has an internal frequency doubling circuit, so the horizontal oscillator is working at its normal line frequency and one line period equals 2 clock pulses. Due to the divider system no vertical frequency adjustment is needed. The divider has a discriminator window for automatically switching over from the 60 Hz to 50 Hz system. The divider system operates with 3 different divider reset windows for maximum interference/disturbance protection.

The windows are activated via an up/down counter. The counter increases its counter value by 1 for each time the separated vertical sync pulse is within the searched window. The count is decreased by 1 when the vertical sync pulse is not present.

Large (search) window: divider ratio between 488 and 722

This mode is valid for the following conditions:
1. Divider is looking for a new transmitter.
2. Divider ratio found, not within the narrow window limits.
3. Up/down counter value of the divider system operating in the narrow window mode decreases below count 1.
4. Externally setting. This can be reached by loading pin 18 with a resistor of 220 kΩ to earth or connecting a 3.6 V diode stabistor between pin 18 and ground.

Narrow window: divider ratio between 522-528 (60 Hz) or 622-628 (50 Hz).

The divider system switches over to this mode when the up/down counter has reached its maximum value of 12 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below count 1 the divider system switches over to the large window mode.

Standard TV-norm

When the up/down counter has reached its maximum value of 12 in the narrow window mode, the information applied to the up/down counter is changed such that the standard divider ratio value is tested. When the counter has reached a value of 14 the divider system is changed over to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing. A missed vertical sync pulse decreases the counter value by 1. When the counter reaches the value of 10 the divider system is switched over to the large window mode. The standard TV-norm condition gives maximum protection for video recorders playing tapes with anti-copy guards.

No-TV-transmitter found: (pin 18 $<$ 1.2 V)

In this condition, only noise is present, the divider is rest to count 628. In this way a stable picture display at normal height is achieved.

DEVELOPMENT DATA

Video tape recorders in feature mode

It should be noted that some VTRs operating in the feature modes, such as picture search, generate such distorted pictures that the no-TV-transmitter detection circuit can be activated as pin V_{18} drops below 1.2 V. This would imply a rolling picture (see Phase detector, sub paragraph d). In general VTR-machines use a re-inserted vertical sync pulse in the feature mode. Therefore the divider system has been made such that the automatic reset of the divider at count 628 when V_{18} is below 1.2 V is inhibited when a vertical sync pulse is detected.

The divider system also generates the anti-top-flutter pulse which inhibits the Phase 1 detector during the vertical sync. pulse. The width of this pulse depends on the divider mode. For the divider mode a the start is generated at the reset of the divider. In mode b and c the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 8 for 50 Hz and count 10 for 60 Hz. The vertical blanking pulse is also generated via the divider system. The start is at the reset of the divider while the blanking pulse ends at count 34 (17 lines) for 60 Hz, and at count 44 (22 lines) for 50 Hz systems. The vertical blanking pulse generated at the sandcastle output pin 17 is made by adding the anti-top-flutter pulse and the blanking pulse. In this way the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in the b or c mode. For generating a vertical linear sawtooth voltage a capacitor should be connected to pin 3. The recommended value is 150 nF to 330 nF (see Fig. 1).

The capacitor is charged via an internal current source starting at the reset of the divider system. The voltage on the capacitor is monitored by a comparator which is activated also at reset. When the capacitor has reached a voltage value of 5.85 V for the 50 Hz system or 4.85 V for the 60 Hz system the voltage is kept constant until the charging period ends. The charge period width is 26 clock pulses. At clock pulse 26 the comparator is switched off and the capacitor is discharged by an npn transistor current source, the value of which can be set by an external resistor between pin 4 and ground (pin 9). Pin 4 is connected to a pnp transistor current source which determines the current of the npn current source at pin 3. The pnp current source on pin 4 is connected to an internal zener diode reference voltage which has a typical voltage of $\approx$ 7.5 volts. The recommended operating current range is 10 to 75 μA. The resistance at pin R_4 should be 100 to 770 kΩ. By using a double current mirror concept the vertical sawtooth pre-correction can be set on the desired value by means of external components between pin 4 and pin 3, or by connecting the pin 4 resistor to the vertical current measuring resistor of the vertical output stage. The vertical amplitude is set by the current of pin 4. The vertical feedback voltage of the output stage has to be applied to pin 2. For the normal amplitude adjustment the values are DC = 1 V and AC = 0.8 V. Due to the automatic system adaptation both values are valid for 50 Hz and 60 Hz.

The low DC voltage value improves the picture bounce behaviour as less parabola compensation is necessary. Even a fully DC coupled feedback circuit is possible.

Vertical guard

The IC also contains a vertical guard circuit. This circuit monitors the vertical feedback signal on pin 2. When the level on pin 2 is below 0.35 V or higher than 1.85 V the guard circuit inserts a continuous level of 2.5 V in the sandcastle output signal of pin 17. This results in the blanking of the picture displayed, thus preventing a burnt-in horizontal line. The guard levels specified refer to the zener diode reference voltage source level.

Driver output

The driver output is at pin 1, it can deliver a drive current of 1.5 mA at 5 V output. The internal impedance is approximately 170 Ω. The output pin is also connected to an internal current source with a sink current of 0.25 mA.

Sync separator, phase detector and TV-station identification (pins 5,6,7,8 and 18)

The video input signal is connected to pin 5. The sync separator is designed such that the slicing level is independent of the amplitude of the sync pulse. The black level is measured and stored in the capacitor at pin 7. The slicing level value is stored in the capacitor at pin 6. The slicing level value can be chosen by the value of the external resistor between pins 6 and 7. The value is given by the formula:

$$P = \frac{R_S}{5.3 + R_S} \times 100 \quad (R_S \text{ value in } k\Omega)$$

Where R_S is the resistor between pins 6 and 7 and top sync level equals 100%. The recommended resistor value is 5.6 kΩ.

Black level detector

A gating signal is used for the black level detector. This signal is composed of an internal horizontal reference pulse with a duty factor of 50% and the flyback pulse at pin 12. In this way the TV-transmitter identification operates also for all DC conditions at input pin 5 (no video modulation, plain carrier only).
During the frame interval the slicing level detector is inhibited by a signal which starts with the anti-top flutter pulse and ends with the reset vertical divider circuit. In this way shift of the slicing level due to the vertical sync signal is reduced and separation of the vertical sync pulse is improved.

Noise level detector

An internal noise inverter is activated when the video level at pin 5 decreases below 0.7 V. The IC also embodies a built-in sync pulse noise level detection circuit. This circuit is directly connected to pin 5 and measures the noise level at the middle of the horizontal sync pulse. When a signal-to-noise level of 19 dB is detected a counter circuit is activated. A video input signal is processed as "acceptable noise free" when 12 out of 15 sync pulses have a noise level below 19 dB for two successive frame periods. The sync pulses are processed during a 15 line width gating period generated by the divider system. The measuring circuit has a built-in noise level hysteresis of approximately 3 dB.
When the "acceptable noise free" condition is found the phase detector of pin 8 is switched to not gated and normal time constant. When a higher sync pulse noise level is found the phase detector is switched over to slow time constant and gated sync pulse phase detection. At the same time the integration time of the vertical sync pulse separator is adapted.

$$S/N = 20 \text{ Log } \frac{\text{Video voltage (black to white } _{p\text{-}p})}{\text{Noise}_{rms}}$$

Phase detector

The phase detector circuit is connected to pin 8. This circuit consists of 3 separate phase detectors which are activated depending on the voltage of pin 18 and the state of the sync pulse noise detection circuit. For normal and fast time constants all three phase detectors are activated during the vertical blanking period, this with the exception of the anti-top-flutter pulse period, and the separated vertical sync-pulse time. As a result, phase jumps in the video signal related to the video head, take over of video recorders are quickly restored within the vertical blanking period. At the end of the blanking period the phase detector time constant is increased by 1.5 times. In this way there is no requirement for external VTR time constant switching, and so all station numbers are suitable for signals from VTR, video games or home computers.
For quick locking of a new TV station starting from a noise only signal condition (normal time constant) a special circuit is incorporated. A new TV station which is not locked to the horizontal oscillator will result in a voltage decrease below 0.1 V at pin 18. This will activate a frame period counter which switches the phase detector to fast for 3 frame periods during the vertical scan period.

The horizontal oscillator will now lock to the new TV-station and as a result, the voltage on pin 18 will increase to approximately 6.5 V. When pin 18 reaches a level of 1.8 V the mute output transistor of pin 13 is switched OFF and the divider is set to the large window. In general the mute signal is switched OFF within 5 ms (pin C_{18} = 47 nF) after reception of a new TV-signal. When the voltage on pin 18 reaches a level of 5 V, usually within 15 ms, the frame counter is switched OFF and the time constant is switched from fast to normal during the vertical scan period.

If the new TV station is weak, the sync-noise detector is activated. This will result in a change over of pin 18 voltage from 6.5 V to ≈ 10 V. When pin 18 exceeds the level of 7.8 V the phase detector is switched to slow time constant and gated sync pulse condition. The current is also reduced during the vertical blanking period by 1 mA. When desired, most conditions of the phase detector can also be set by external means in the following way:

a. Fast time constant TV transmitter identification circuit not active, connect pin 18 to earth (pin 9).
b. Fast time constant TV transmitter identification circuit active, connect a resistor of 220 kΩ between pin 18 and ground.
   This condition can also be set by using a 3.6 V stabistor diode instead of a resistor.
c. Slow time constant, (with exception of frame blanking period), connect pin 18 via a resistor of 10 kΩ to + 12 V, pin 10. In this condition the transmitter identification circuit is not active.
d. No switching to slow time constant desired (transmitter identification circuit active), connect a 6.8 V zener diode between pin 18 and ground.

Fig. 2 illustrates the operation of the 3 phase detector circuits.

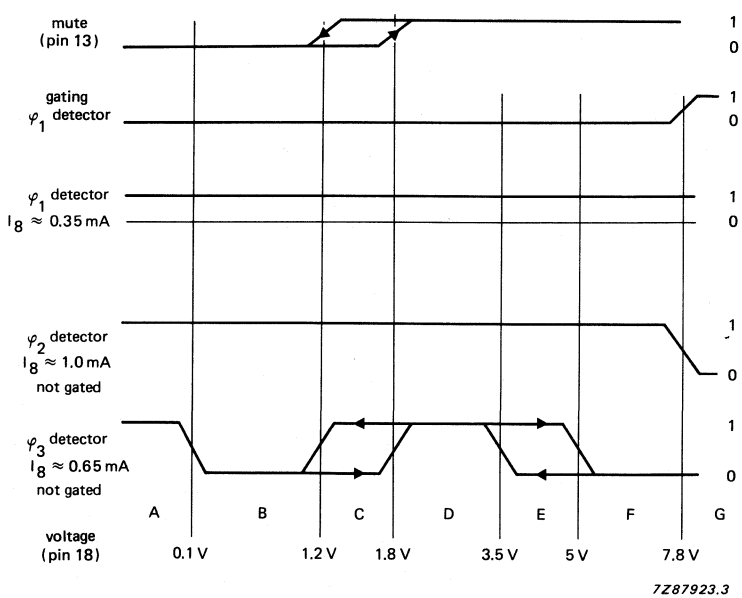


Fig. 2 Timing diagram, phase detectors.

Supply (pins 9, 10 and 16)

The IC has been designed such that the horizontal oscillator and output stage can start operating by application of a very low supply current into pin 16.

The horizontal oscillator starts at a supply current of approximately 4 mA. The horizontal output stage is forced into the non-conducting stage until the supply current has a typical value of 5 mA. The circuit has been designed so that after starting the horizontal output function a current drop of $\approx$ 1 mA is allowed. The starting circuit has the ability to derive the main supply (pin 10) from the horizontal output stage. The horizontal output signal can also be used as the oscillator signal for synchronized switched mode power supplies. The maximum allowed starting current is 9.7 mA (T_{amb} = 25 °C). The main supply should be connected to pin 10, and pin 9 should be used as ground. When the voltage on pin 10 increases from zero to its final value (typically 12 V) a part of the supply current of the starting circuit is taken from pin 10 via internal diodes, and the voltage on pin 16 will stabilize to a typical value of 9.4 V.

In a stabilized condition (pin $V_{10} > 10$ V) the minimum required supply current to pin 16 is $\approx$ 2.5 mA. All other IC functions are switched on via the main supply voltage on pin 10. When the voltage on pin 10 reaches a value of $\approx$ 7 V the horizontal phase detector circuit is activated and the vertical ramp on pin 3 is started. The second phase detector circuit and burst pulse circuit are started when the voltage on pin 10 reaches the stabilized voltage value of pin 16 which is typically 9.4 V.

To close the second phase detector loop, a flyback pulse must be applied to pin 12. When no flyback pulse is detected the duty factor of the horizontal output stage is 50%.

For remote switch-off pin 16 can be connected to ground (via a npn transistor with a series resistor of $\approx$ 500 Ω) which switches off the horizontal output.

Horizontal oscillator, horizontal output transistor, and second phase detector (pins 11, 12, 14 and 15)

The horizontal oscillator is connected to pin 15. The frequency is set by an external RC combination between pin 15 and ground, pin 9. The open collector horizontal output stage is connected to pin 11. An internal zener diode configuration limits the open voltage of pin 11 to $\approx$ 14.5 V.
The horizontal output transistor at pin 11 is blocked until the current into pin 16 reaches a value of $\approx$ 5 mA.
A higher current results in a horizontal output signal at pin 11, which starts with a duty factor of $\approx$ 40% HIGH.

The duty factor is set by an internal current-source-loaded npn emitter follower stage connected to pin 14 during starting. When pin 16 changes over to voltage stabilization the npn emitter follower and current source load at pin 14 are switched OFF and the second phase detector circuit is activated, provided a horizontal flyback pulse is present at pin 12. When no flyback pulse is detected at pin 12 the duty factor of the horizontal output stage is set to 50%.

The phase detector circuit at pin 14 compensates for storage time in the horizontal deflection output stage. The horizontal output pulse duration is 29 μs HIGH for storage times between 1 μs and 17 μs (flyback pulse of 12 μs). A higher storage time increases the HIGH time. Horizontal picture shift is possible by forcing an external charge or discharge current into the capacitor at pin 14.

Mute output and 50/60 Hz identification (pin 13)

The collector of an npn transistor is connected to pin 13. When the voltage on pin 18 drops below 1.2 V (no TV-transmitter) the npn transistor is switched ON.
When the voltage on pin 18 increases to a level of $\approx$ 1.8 V (new TV-transmitter found) the npn transistor is switched OFF.

Pin 13 has also the possibility for 50/60 Hz identification. This function is available when pin 13 is connected to pin 10 (+ 12 V) via an external pull-up resistor of 10 to 20 kΩ. When no TV-transmitter is identified the voltage on pin 13 will be LOW ($<$ 0.5 V). When a TV-transmitter with a divider ratio $>$ 576 (50 Hz) is detected the output voltage of pin 13 is HIGH (+ 12 V).
When a TV-transmitter with a divider ratio $<$ 576 (60 Hz) is found an internal pnp transistor with its emitter connected to pin 13 will force this pin output voltage down to $\approx$ 7.6 V.

Sandcastle output (pin 17)

The sandcastle output pulse generated at pin 17, has three different voltage levels. The highest level, (10.4 V), can be used for burst gating and black level clamping. The second level (4.5 V) is obtained from the horizontal flyback pulse at pin 12, and is used for horizontal blanking. The third level (2.5 V) is used for vertical blanking and is derived via the vertical divider system. For 50 Hz the blanking pulse duration is 44 clock pulses and for 60 Hz it is 34 clock pulses started from the vertical divider reset. For TV-signals which have a divider ratio between 622 and 628 or between 522 and 528 the pulse is started at the first equalizing pulse. With the 50/60 Hz information the burst-key pulse width is switched to improve the behaviour in multi-norm concepts.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Start current	I_{16}	–	9.7	mA
Supply voltage	V_{10}	–	13.2	V
Total power dissipation	P_{tot}	–	1.2	W
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−25	+ 70	°C

Thermal resistance

From junction to ambient in free air $R_{th\ j\text{-}a}$ 50 K/W

CHARACTERISTICS

T_{amb} = 25 °C; I_{16} = 6.2 mA; V_{10} = 12 V; unless otherwise specified
Voltage measurements are taken with respect to pin 9 (ground)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply current (pin 16)						
V_{10} = 0 V		I_{16}	6.2	–	9.7	mA
V_{10} = 10 V		I_{16}	2.5	–	9.7	mA
Stabilized voltage (pin 16)		V_{16}	8.8	9.3	9.7	V
Current consumption (pin 10)		I_{10}	–	70	85	mA
Supply voltage range (pin 10)		V_P	10	12	13.2	V
Video input (pin 5)						
Top sync level		V_5	1.5	3.1	3.75	V
Sync pulse amplitude (peak-to-peak value)	note 1	$V5_{(p\text{-}p)}$	0.05	0.6	1.0	V
Slicing level	note 2		35	50	65	%
Delay between video input and detector output (see also Fig. 3)			0.2	0.3	0.55	µs
Sync pulse noise level detector circuit active	note 3	S/N	–	19	–	dB
Sync pulse						
Noise level detector circuit hysteresis			–	3	–	dB
Noise gate (pin 5)						
Switching level		V_5	–	+ 0.7	+ 1	V
First control loop (pin 8) (horizontal oscillator to sync)						
Holding range		Δf	–	± 800		Hz
Catching range		Δf	± 700	± 800	± 1100	
Control sensitivity video with respect to burst-key and flyback-pulse						
Slow time constant			–	2	–	kHz/µs
Normal time constant			–	5	–	kHz/µs
Fast time constant			–	3	–	kHz/µs
Phase modulation due to hum on the supply line (pin 10)	note 4		–	0.2	–	µs/Vtt
Phase modulation due to hum on input current (pin 16)	note 4		–	0.08	–	µs/Vtt

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Second control loop (pin 14) (horizontal flyback to horizontal oscillator)						
Control sensitivity	t_d = 10 µs	$\Delta t_d/\Delta t_o$	200	300	600	µs
Control range		t_d	1	–	>45	µs
Control range for constant duty factor horizontal output		t_d	1	29 (–t flyback pulse)		µs
Controlled edge of horizontal output signal (pin 11)				positive		
Phase adjustment (pin 14) (via second control loop)						
Control sensitivity	t_d = 10 µs		–	25	–	µA/µs
Maximum allowed control current		I_{14}	–	–	± 60	µA
Horizontal oscillator (pin 15)	C = 2.7 nF; R_{osc} = 34.8 kΩ					
Frequency (no sync)		f	–	15625	–	Hz
Spread (fixed external component, no sync)		Δf	–	–	± 4	%
Frequency deviation between starting point output signal and stabilized condition		Δf	–	+ 5	+ 8	%
Temperature coefficient		T_C	–	-1.10^{-4}	–	/K
Horizontal output (pin 11) (Open collector)						
Output voltage high		V_{11}	–	–	13.2	V
Start voltage protection (internal zener diode)		V_{11}	13	–	15.8	V
Low input current (pin 16) protection output enabled		I_{16}	–	5.0	6.2	mA
Output voltage low start condition	I_{11} = 10 mA	V_{11}	–	0.1	0.5	V
Duty factor output current during starting	I_{16} = 6.2 mA		50	60	70	%
Output voltage low normal condition	I_{11} = 25 mA	V_{11}	–	0.3	0.5	V
Duty factor output current without flyback pulse (pin 12)			45	50	55	%
Duration of the output pulse HIGH	t_d = 10 µs		27	29	31	µs
Controlled edge			positive			
Temperature coefficient horizontal output pulse			–	-5.10^{-2}	–	µs/°C
Influence of delay time on pulse width of the horizontal output signal		$\Delta H_W/t_d$	–	0.16	–	µs/µs

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle output signal (pin 17)	I_L = 1 mA					
Output voltage during:						
burst-key		V_{17}	9.8	10.4	–	V
horizontal blanking		V_{17}	4.1	4.5	4.9	V
vertical blanking	I_L = 0.3 mA	V_{17}	2.1	2.5	2.9	V
Zero level output voltage	I_{sink} = 0.5 mA	V_{17}	–	–	0.7	V
Pulse width:						
burst-key (50 Hz)		t_p	3.85	4.15	4.6	μs
burst-key (60 Hz)		t_p	3.40	3.65	4.0	μs
Horizontal blanking		V_{12}	–	1.0	–	V
Vertical blanking	note 5					
Phase position burstkey time between middle sync pulse at pin 5 and start of burst pulse at pin 17			2.3	2.7	3.1	μs
Time between start sync pulse and end of burst pulse at pin 17						
(50 Hz)			–	9.3	9.7	μs
(60 Hz)			–	8.8	9.2	μs
Coincidence detector, video transmitter identification circuit and time constant switching levels (see also Fig. 1)						
Detector output current		I_{18}	–	0.25	–	mA
Voltage level for in sync condition (φ_1 normal)		V_{18}	5.8	6.5	7.0	V
Voltage for noisy sync pulse (φ_1 slow and gated)		V_{18}	9	10	–	V
Voltage level for noise only	note 6	V_{18}	–	0.3	–	V
Switching level normal to fast		V_{18}	<3.2	3.5	3.8	V
Switching level mute output active and fast to normal		V_{18}	<1.0	1.2	1.4	V
Switching level frame period counter (3 periods fast)		V_{18}	<0.08	0.12	0.16	V
Switching level: normal to fast (locking) mute output inactive		V_{18}	>1.5	1.75	2.0	V
Switching level fast to normal (locking)		V_{18}	>4.7	5.0	5.3	V
Switching level normal to slow (gated sync pulse)		V_{18}	7.4	7.8	8.2	V

parameter	conditions	symbol	min.	typ.	max.	unit
Video transmitter identification output (pin 13)						
Output voltage active (no sync)	I_{13} = 1 mA	V_{13}	–	0.15	0.32	V
Sink current active (no sync)	$V_{13} < 1$ V	I_{13}	–	–	5	mA
Output current inactive (sync 50 Hz)		I_{13}	–	–	1	μA
50/60 Hz identification (pin 13) (R_{13} positive supply 12 kΩ)						
Emitter follower, pnp:						
60 Hz: $\frac{2 \times f_H}{f_V} < 576$ voltage		V_{13}	7.2	7.65	8.1	V
50 Hz: $\frac{2 \times f_H}{f_V} > 576$ voltage		V_{13}	–	V_{10}	–	V
Flyback input pulse (pin 12)						
Switching level		V_{12}	–	+1	–	V
Input current		I_{12}	+0.2	–	+3	mA
Input pulse		V_{12}	–	–	12	V_P
Input resistance			–	3.5	–	kΩ
Phase position without shift time between the middle of the sync pulse at pin 5 and the middle of the horizontal blanking pulse at pin 17		t_d	2.1	2.5	2.9	μs
Vertical ramp generator (pin 3)						
Pulse width charge current		–	–	26	–	clock pulses
Charge current		I_3	–	3	–	mA
Top level ramp signal voltage						
Divider in 50 Hz mode	note 7	V_3	5.5	5.85	6.3	V
Divider in 60 Hz mode	note 7	V_3	4.55	4.85	5.25	V
Ramp amplitude	C_3 = 150 nF,					
R_4 = 330 kΩ 50 Hz	note 7		–	3.1	–	V_P
R_4 = 330 kΩ 60 Hz	note 7		–	2.5	–	V_P
Temperature coefficient	I_4 = 30 μA	I_3	–	+ 100	–	10^{-6}/K

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Current source (pin 4)						
Output voltage	$I_4 = 20\ \mu A$	V_4	7.0	7.5	7.9	V
Allowed current range		I_4	10	–	75	μA
Temperature coefficient output voltage	$I_4 = 30\ \mu A$	TC	–	+ 50	–	$10^{-6}/K$
Comparator (pin 2)	$C_3 = 150$ nF; $R_4 = 330\ k\Omega$					
Input voltage						
DC level	note 7	V_2	0.97	1.07	1.17	V
AC level		V_2	–	0.8	–	V_P
Deviation amplitude 50/60 Hz			–	1.75	2.5	%
Vertical output stage (pin 1) (npn emitter follower)						
Output voltage	I_o pin 1 = +1.5 mA note 7	V_1	5.0	5.5	6.3	V
R_S, sync separator resistor			–	170	–	Ω
Continuous sink current			–	0.25	–	mA
Vertical guard circuit (pin 2)						
Active ($V_{17} = 2.5$ V)						
Switching level LOW	note 7	V_2	> 1.7	1.85	2.0	V
Switching level HIGH	note 7	V_2	< 0.25	0.35	0.45	V

Notes to the characteristics

1. Up to 1 V peak-to-peak the slicing level is constant, at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. The slicing level is fixed by the formula:

$$P = \frac{R_S}{5.3 + R_S} \times 100\% \quad (R_S \text{ value in } k\Omega)$$

3. $$S/N = 20 \log \frac{\text{video voltage black to white (p-p)}}{\text{noise (rms)}}$$

   measured with 1 $V_{p\text{-}p}$ video input
4. Measured between pin 5 and sandcastle output pin 17.
5. Divider in search (large) mode:
   start: reset divider = start vertical sync plus 1 clock pulse
   stop:

$$n = \frac{2 \times f_H}{f_V} > 576 \text{ clock pulse } 44$$

$$n = \frac{2 \times f_H}{f_V} < 576 \text{ clock pulse } 34$$

   Divider in small window mode:
   start: clock pulse 517 (60 Hz) clock pulse 618 (50 Hz)
   stop: clock pulse 34 (60 Hz) clock pulse 44 (50 Hz)
6. Depends on DC level of pin 5, given value is valid for $V_5 \approx 5$ V.
7. Value related to internal zener diode reference voltage source spread includes the complete spread of reference voltage.

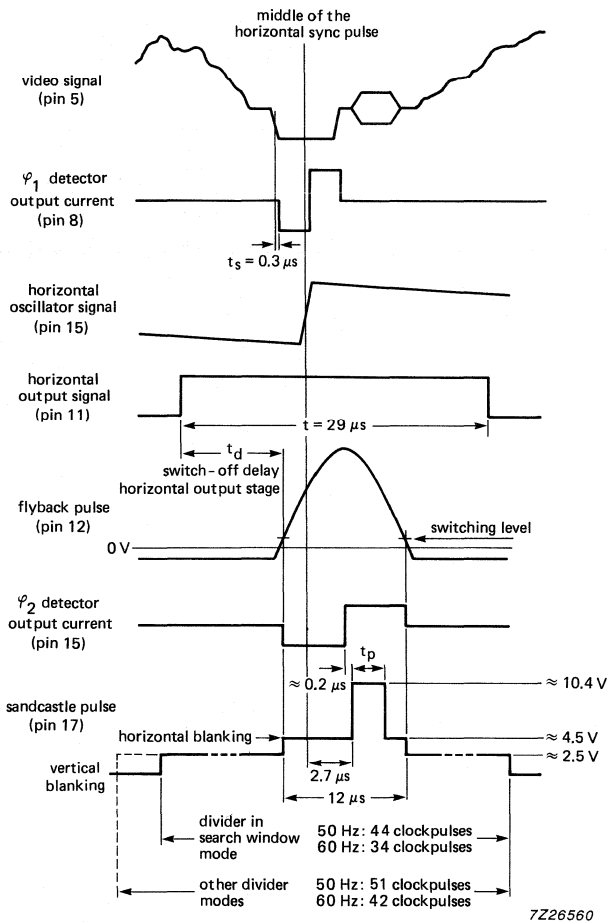


Fig.3 Timing diagram of the TDA2579B.

APPLICATION INFORMATION

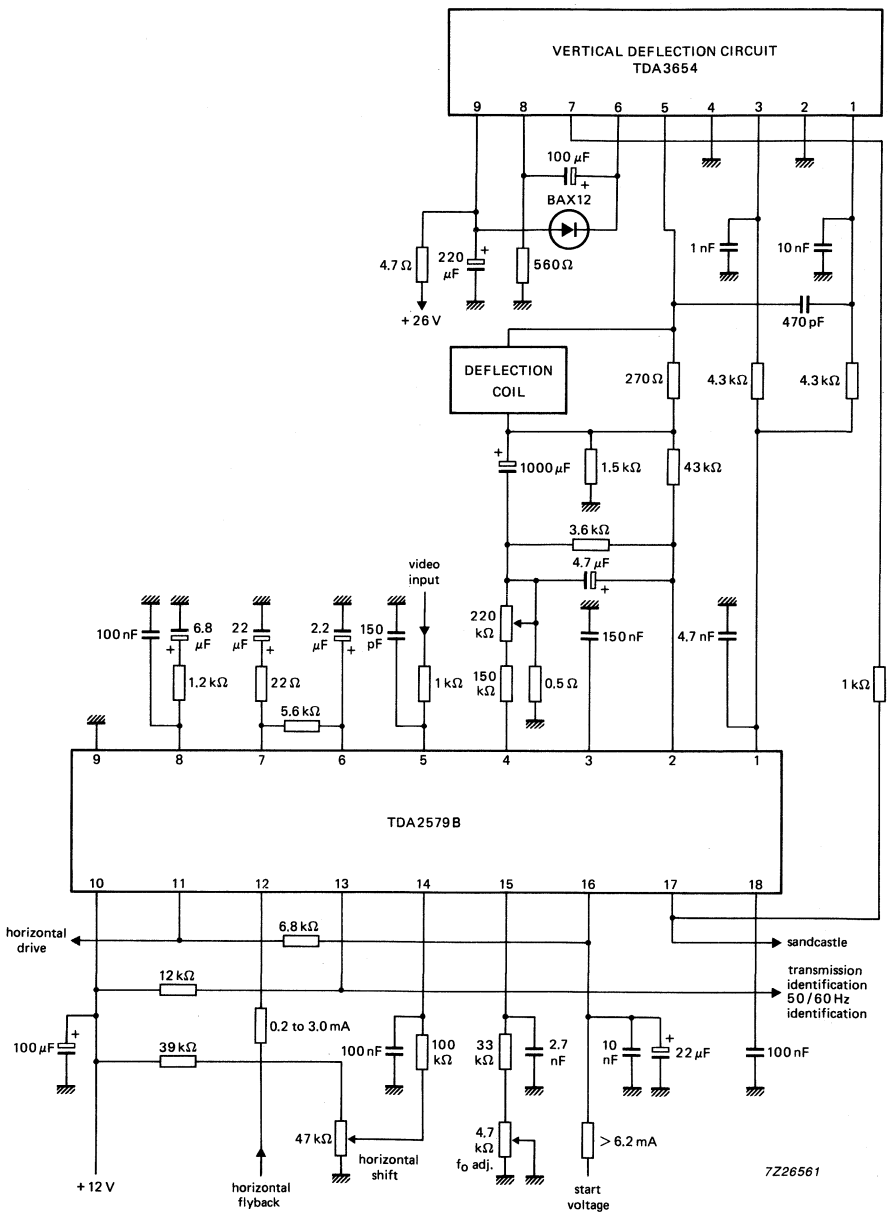


Fig.4 TDA2579B 110° application circuit (45AX).

CONTROL CIRCUIT FOR POWER SUPPLIES

The TDA2582 is a monolithic integrated circuit for controlling power supplies which are provided with the drive for the horizontal deflection stage.
The circuit features the following:

- Voltage controlled horizontal oscillator.
- Phase detector.
- Duty factor control for the negative-going transient of the output signal.
- Duty factor increases from zero to its normal operation value.
- Adjustable maximum duty factor.
- Over-voltage and over-current protection with automatic re-start after switch-off.
- Counting circuit for permanent switch-off when n-times over-current or over-voltage is sensed.
- Protection for open-reference voltage.
- Protection for too low supply voltage.
- Protection against loop faults.
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1,5 V.
- Normal and 'smooth' remote ON/OFF possibility.

QUICK REFERENCE DATA

Supply voltage	$V_{9\text{-}16}$	typ.	12 V
Supply current	I_9	typ.	14 mA
Input signals			
Horizontal drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$		5 to 11 V
Flyback pulse (differentiated deflection current); peak-to-peak value	$V_{2\text{-}16(p\text{-}p)}$		1 to 5 V
External reference voltage	$V_{10\text{-}16}$	typ.	6,1 V
Output signals			
Duty factor of output pulse	δ	$>$ $<$	0 % 98 ± 0,8 %
Output voltage at $I_o < 20$ mA (peak value)	$V_{11\text{-}16M}$	typ.	11,8 V
Output current (peak value)	I_{11M}	$<$	40 mA

PACKAGE OUTLINES

TDA2582 : 16-lead DIL; plastic (SOT38).
TDA2582Q: 16-lead QIL; plastic (SOT58).

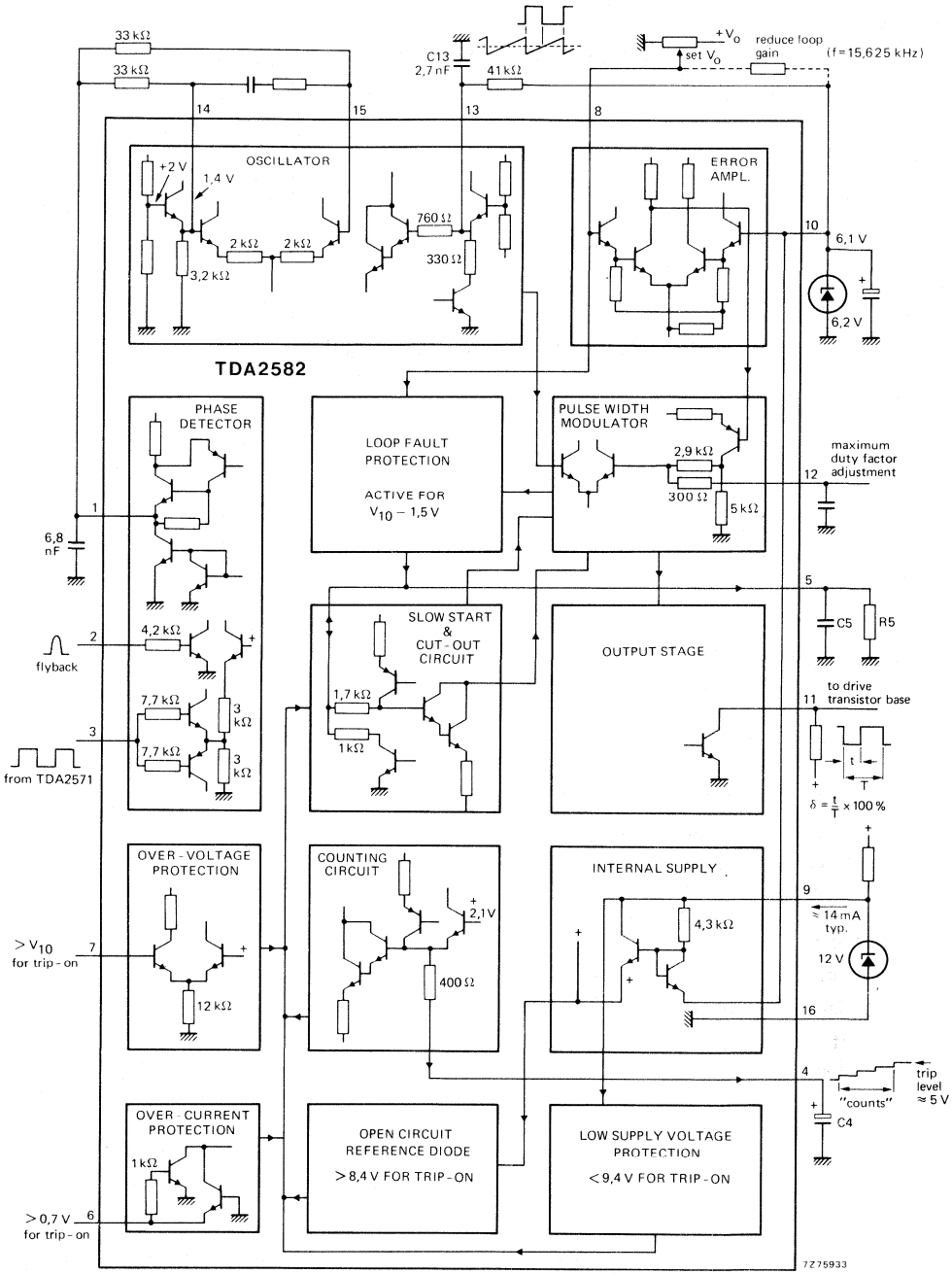


Fig. 1 Block diagram.

Note: trip levels are nominal values.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage at pin 9	V_{9-16}	max. 14	V
Voltage at pin 11	V_{11-16}	0 to 14	V
Output current (peak value)	I_{11M}	max. 40	mA
Total power dissipation	P_{tot}	max. 280	mW
Storage temperature	T_{stg}	−25 to + 125	°C
Operating ambient temperature	T_{amb}	−25 to + 80	°C

CHARACTERISTICS

V_{9-16} = 12 V; V_{10-16} = 6,1 V; T_{amb} = 25 °C; measured in Fig. 4

Supply voltage range	V_{9-16}	typ. 12 10 to 14	V V
Protection voltage too low supply voltage	V_{9-16}	typ. 9,4 8,6 to 9,9	V V
Supply current at δ = 50%	I_9	typ. 14	mA
Supply current during protection	I_9	typ. 14	mA
Minimum required supply current (note 1)	I_9	< 17	mA
Power consumption	P	typ. 170	mW
Required input signals			
Reference voltage (note 2)	V_{10-16}	typ. 6,1 5,6 to 6,6	V V
Feedback input impedance	$\lvert Z_{8-16} \rvert$	typ. 200	kΩ
High reference voltage protection: threshold voltage	V_{10-16}	typ. 8,4 7,9 to 8,9	V V
Horizontal reference signal (square-wave or differentiated; negative transient is reference)			
Voltage driven (peak-to-peak value)	$V_{3-16(p-p)}$	5 to 12	V
Current driven (peak value)	I_{3M}	−1 to + 1,5	mA
Switching level current	$\pm I_3$	< 100	μA
Flyback pulse or differential deflection current	V_{2-16}	1 to 5	V
Flyback pulse current (peak value)	I_{2M}	< 1,5	mA
Over-current protection: (note 3) threshold voltage	$-V_{6-16}$	typ. 640 600 to 695	mV mV
	$+V_{6-16}$	typ. 680 640 to 735	mV mV

Notes

1. This value refers to the minimum required supply current that will start all devices under the following conditions: V_{9-16} = 10 V; V_{10-16} = 6,2 V; δ = 50%.
2. Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.
3. This spread is inclusive temperature rise of the IC due to warming up. For other ambient temperatures the values must be corrected by using a temperature coefficient of typical −1,85 mV/°C.

CHARACTERISTICS (continued)

Over-voltage protection: ($V_{ref} = V_{10\text{-}16}$) threshold voltage	$V_{7\text{-}16}$	typ.	V_{ref}–60 mV
			V_{ref}–130 to V_{ref}–0 mV
Remote control voltage; switch-off (note 1)	$V_{4\text{-}16}$	>	5,6 V
Remote control voltage; switch-on	$V_{4\text{-}16}$	<	4,5 V
'Smooth' remote control; switch-off (note 2)	$V_{5\text{-}16}$	>	4,5 V
'Smooth' remote control; switch-on	$V_{5\text{-}16}$	<	3 V
Remote control switch-off current	I_4	<	1 mA
Delivered output signals			
Horizontal drive pulse (loaded with a resistor of 560 Ω to + 12 V peak-to-peak value	$V_{11\text{-}16(p\text{-}p)}$	>	11,6 V
Output current; peak value	I_{11M}	<	40 mA
Saturation voltage of output transistor at I_{11} = 20 mA	V_{CEsat}	typ.	200 mV
		<	400 mV
at I_{11} = 40 mA	V_{CEsat}	<	525 mV
Duty factor of output pulse (note 3)	δ	>	0 %
		<	98 ± 0,8 %
Charge current for capacitor on pin 4	I_4	typ.	110 μA
Charge current for capacitor on pin 5	I_5	typ.	120 μA
Supply current for reference	I_{10}	typ.	1 mA
			0,6 to 1,45 mA
Oscillator			
Temperature coefficient		typ.	0,0003 $^oC^{-1}$
		<	0,0004 $^oC^{-1}$
Relative frequency deviation for $V_{10\text{-}16}$ changing from 5,6 to 6,6 V		typ.	–1,4 %
		<	–2 %
Oscillator frequency spread (with fixed external components)		<	3 %
Frequency control sensitivity at pin 15 f_{nom} = 15,625 kHz		typ.	5 kHz/V

Notes

1. See application information pin 4.
2. See application information pin 5.
3. The duty factor is specified as follows: $\delta = \frac{t_p}{T} \times 100\%$ (see Fig. 2). After switch-on the duty factor rises gradually from 0% to the steady value. The relationship between $V_{8\text{-}16}$ and the duty factor is given in Fig. 7 and the relationship between $V_{12\text{-}16}$ and the duty factor is shown in Fig. 9.

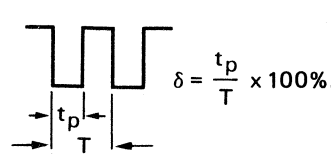


Fig. 2.

Phase control loop

Loop gain of APC-system (automatic phase control) *		typ.	5	kHz/μs
Catching range (f_{nom} = 15,625 kHz)	Δf	>	1300	Hz
		<	2100	Hz
Phase relation between negative transient of sync pulse and middle of flyback	t	typ.	1	μs
Tolerance of phase relation	Δt	⩽	± 0,4	μs

PINNING

1. Phase detector output
2. Flyback pulse position input
3. Reference frequency input
4. Re-start count capacitor/remote control input
5. Slow start and transfer characteristic for low feedback voltages
6. Over-current protection input
7. Over-voltage protection input
8. Feedback voltage input
9. Positive supply
10. Reference input
11. Output
12. Maximum duty factor adjustment/smoothing
13. Oscillator timing network
14. Reactance stage reference voltage
15. Reactance stage input
16. Negative supply (ground)

* For component values see Fig. 1.

APPLICATION INFORMATION

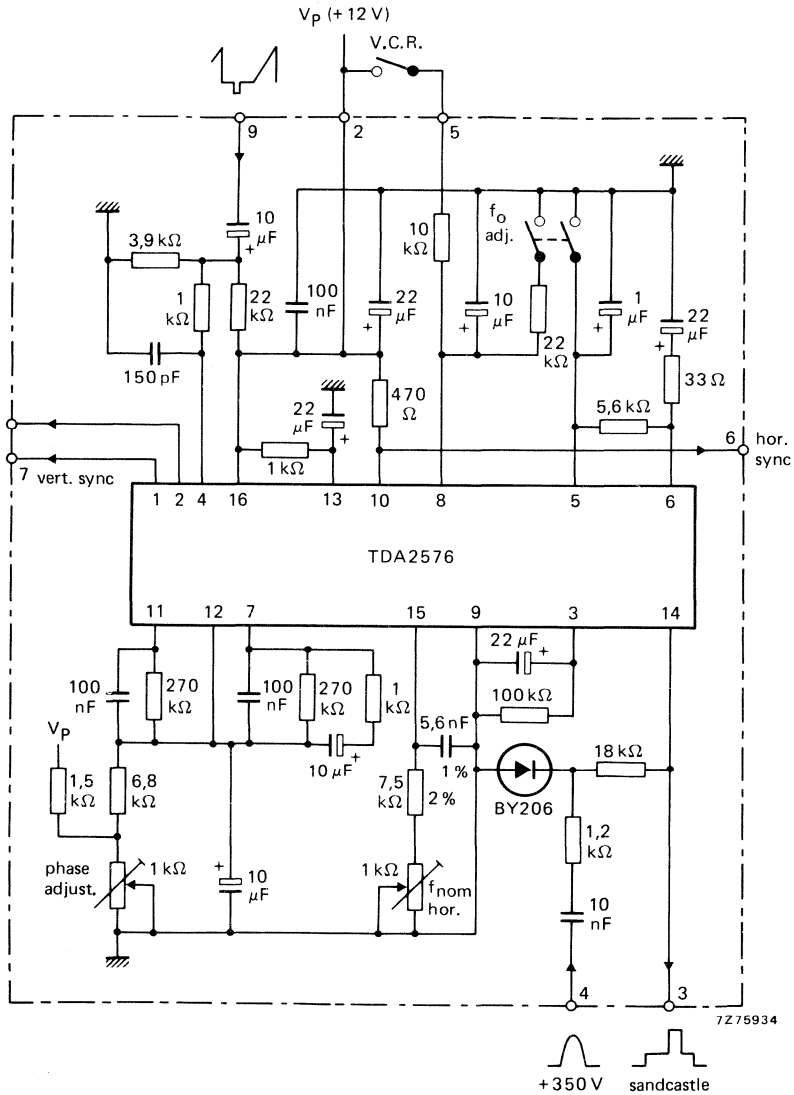


Fig. 3a.

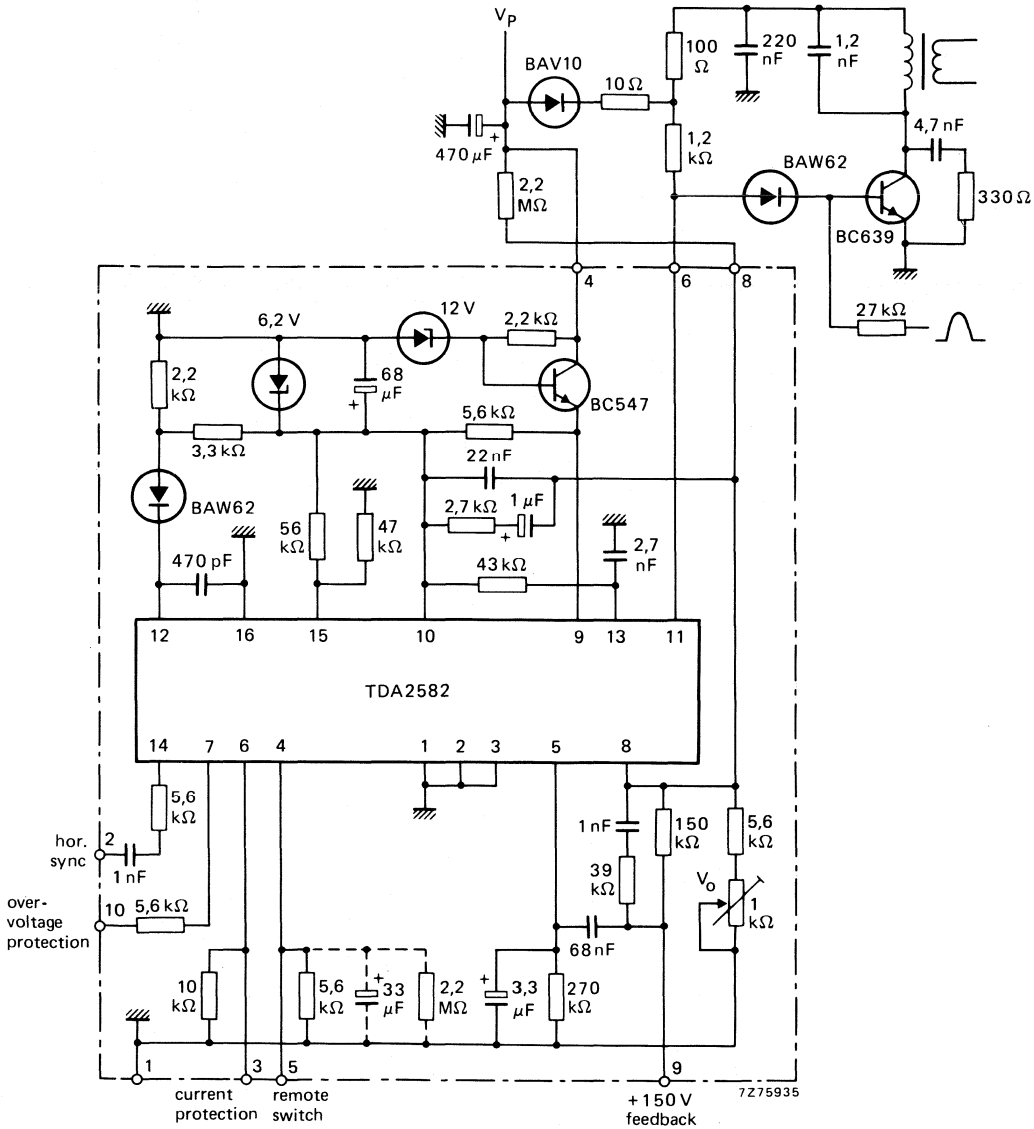


Fig. 3b.

Lead 6 (pin 10) of circuit TDA2576 connected to lead 2 (pin 14) of circuit TDA2582.

APPLICATION INFORMATION

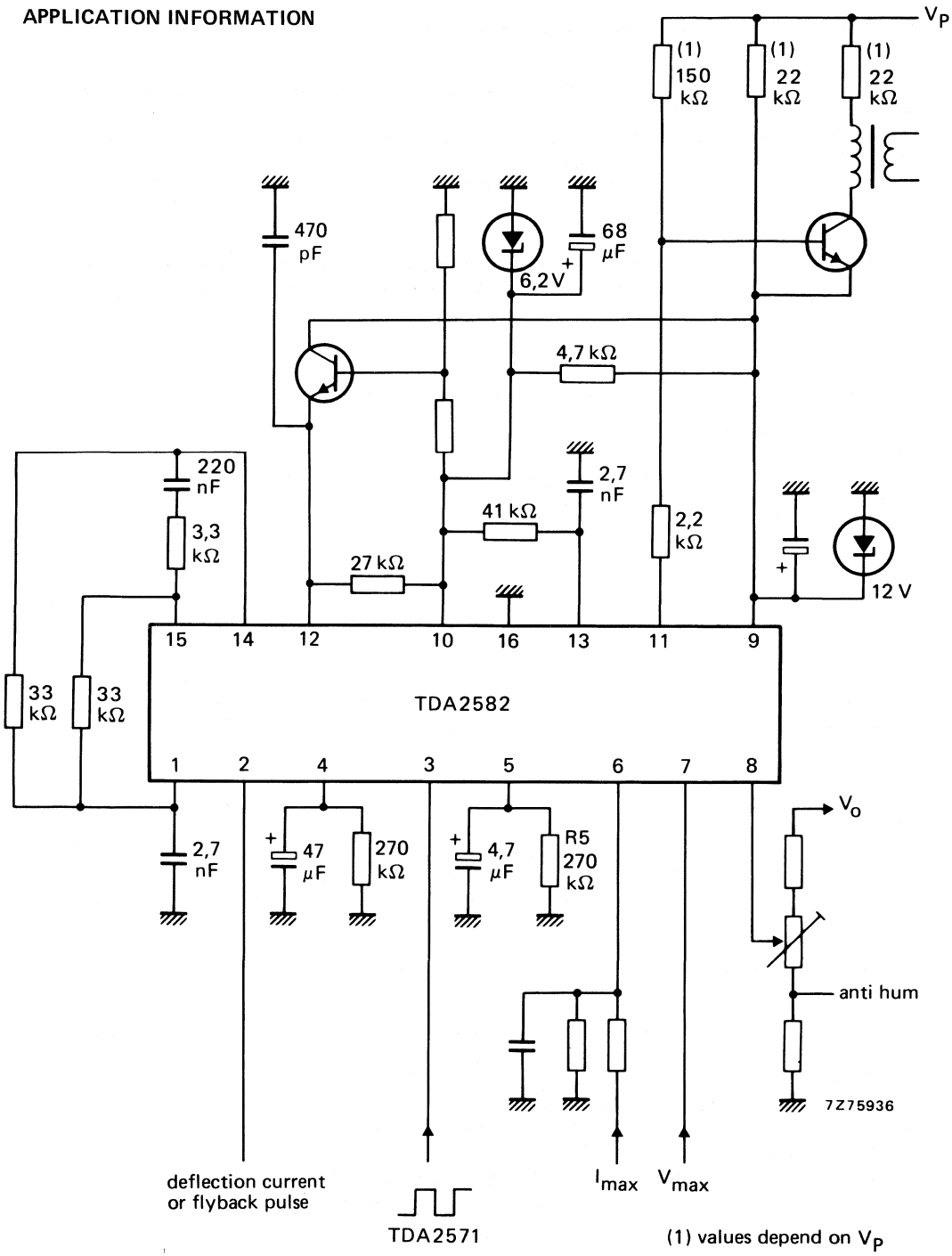


Fig. 4 Circuit diagram.

The function is described against the corresponding pin number

1. Phase detector output

The output circuit consists of a bidirectional current source which is active for the time that the signal on pin 2 exceeds 1 V.
The current values are chosen such that the correct phase relation is obtained when the output signal of the TDA2571 is applied to pin 3.
With a resistor of 2 x 33 kΩ and a capacitor of 2,7 nF the control steepness is 0,55 V/μs (Fig. 4).

2. Flyback pulse input

The signal applied to pin 2 is normally a flyback pulse with a duration of about 12 μs. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3 μs).

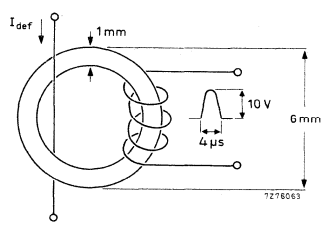


Fig. 5a.

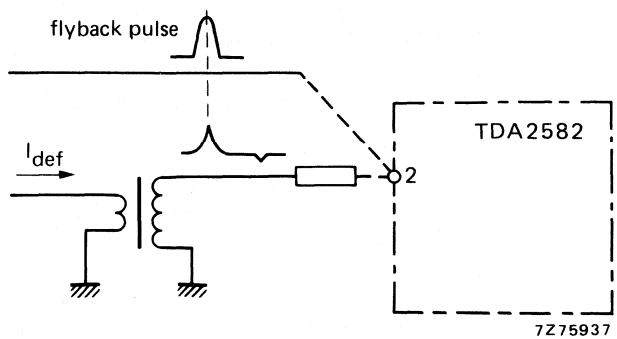


Fig. 5b.

The toroidal transformer in Fig. 5a is for obtaining a pulse representing the mid-flyback from the deflection current. The connection of the picture phase information is shown in Fig. 5b.

3. Reference frequency input

The input circuit can be driven directly by the square-wave output voltage from pin 8 of the TDA2571.
The negative-going transient switches the current source connected to pin 1 from positive to negative.
The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables mains isolation). The input circuit switching level is about 3 V and the input impedance is about 8 kΩ.

4. Re-start count capacitor/remote control input

Counting

An external capacitor (C4 = 47 μF) is connected between pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.
If the protection circuits are required to operate, e.g. over-current at pin 6, the duty factor will be set to zero thus turning off the power supply.
After a short interval (determined by the time constant on pin 5) the power supply will be restarted via the slow start circuit.
If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

The number of times this action is repeated (n) for a persisting fault condition is now determined by: n = C4/C5.

APPLICATION INFORMATION (continued)

Remote control input

For this application the capacitor on pin 4 has to be replaced by a resistor with a value between 4,7 and 18 kΩ. When the externally applied voltage $V_{4\text{-}16} > 5{,}6$ V, the circuit switches off; switching on occurs when $V_{4\text{-}16} < 4{,}5$ V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1,5 V.

5. Slow start and transfer characteristics for low feedback voltages

Slow start

An external shunt capacitor (C5 = 4,7 μF) and resistor (R5 = 270 kΩ) are connected between pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

Transfer characteristic for low feedback voltages

The duty factor transfer characteristic for low feedback voltages can be influenced by R5. The transfer for three different resistor values is given in Fig. 7.

'Smooth' remote ON/OFF

The ON/OFF information should be applied to pin 5 via a high ohmic resistor, a high OFF-level gives a slow rising voltage at pin 5, which results in a slowly decreasing duty factor.

6. Over-current protection input

A voltage proportional to the current in the power switching device is applied to the integrated circuit between pins 6 and 16. The circuit trips on both positive and negative polarity. When the tripping level is reached, the output pulse is immediately blocked and the starting circuit is activated again.

7. Over-voltage protection input

When the voltage applied to this pin exceeds the threshold level the protection circuit will operate. The tripping level is about the same as the reference voltage on pin 10.

8. Feedback voltage input

The control loop input is applied to pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 10.
Under normal operating conditions, the voltage on pin 8 will be about equal to the reference voltage on pin 10. For further information refer to the Figs 7 and 8.

9. 12 V positive supply

The maximum voltage that may be applied is 14 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 9 and 16 to ensure that the maximum voltage does not exceed 14 V. When the voltage on this pin falls below a minimum of 8,6 V (typically 9,4 V), the protection circuit will switch-off the power supply.

10. Reference input

An external reference diode must be connected between this pin and pin 16.
The reference voltage must be between 5,6 and 6,6 V. The IC delivers about 1 mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between pins 9 and 10. A higher reference voltage value up to 7,5 V is allowed when use is made of a duty factor limiting resistor < 27 kΩ between pins 12 and 16.

11. Output

An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an n-p-n transistor with 3 series-connected clamping diodes to the internal 12 V supply rail. This provides a low impedance in the "ON" state, that is with the drive transistor turned-off.

12. Maximum duty factor adjustment/smoothing

Maximum duty factor adjustment

Pin 12 is connected to the output voltage of the amplitude comparator ($V_{10\text{-}8}$). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A high voltage on pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting pin 12 to the emitter of an n-p-n transistor used as a voltage source.
Fig. 9 plots the maximum duty factor as a function of the voltage applied to pin 12. If some spread is acceptable the maximum duty factor can also be limited by connecting a resistor from pin 12 to pin 16. A resistor of 12 kΩ limits the maximum duty factor to about 50%. This application also reduces the total IC gain.

Smoothing

Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470 pF between pins 12 and 16.

13. Oscillator timing network

The timing network comprises a capacitor between pins 13 and 16, and a resistor between pin 13 and the reference voltage on pin 10.
The charging current for the capacitor (C13) is derived from the voltage reference diode connected to pin 10 and discharged via an internal resistor of about 330 Ω.

14. Reactance stage reference voltage

This pin is connected to an emitter follower which determines the nominal reference voltage for the reactance stage (1,4 V for reference voltage $V_{10\text{-}16} = 6{,}1$ V). Free-running frequency is obtained when pins 14 and 15 are short-circuited.

15. Reactance stage input

The output voltage of the phase detector (pin 1) is connected to pin 15 via a resistor. The voltage applied to pin 15 shifts the upper level of the voltage sensor of the oscillator thus changing the oscillator frequency and phase. The time constant network is connected between 14 and 15. Control sensitivity is typically 5 kHz/V.

16. Negative supply (ground)

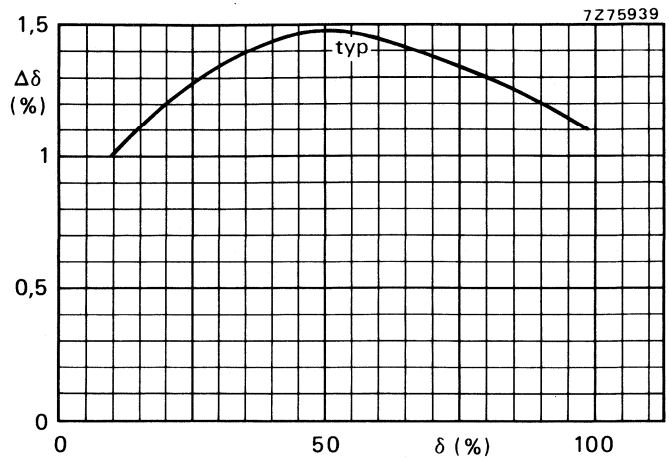


Fig. 6 Duty factor change as a function of initial duty factor; at 1 mV error amplifier input change; $\Delta V_{8\text{-}10(p\text{-}p)}$ = 1 mV.

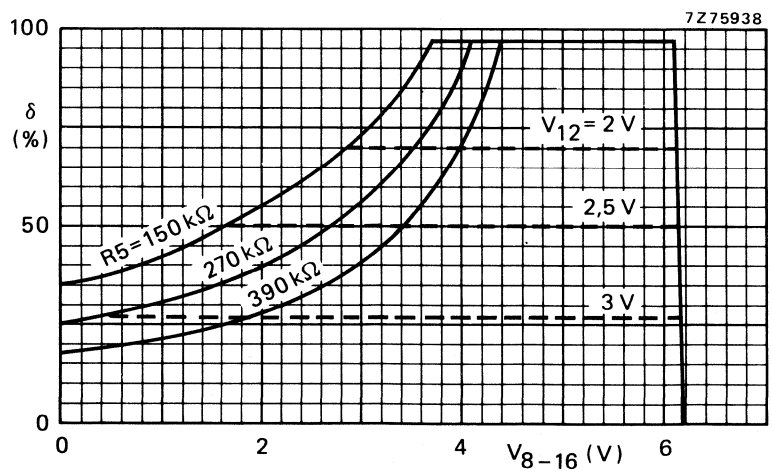


Fig. 7 Duty factor of output pulses as a function of feedback input voltage ($V_{8\text{-}16}$) with R5 as a parameter and $V_{12\text{-}16}$ as a limiting value; $V_{10\text{-}16}$ = 6,1 V.

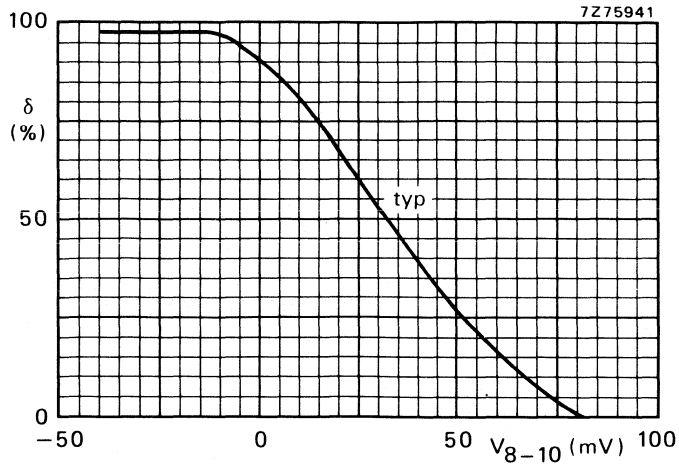


Fig. 8 Duty factor of output pulses as a function of error amplifier input ($V_{8\text{-}10}$); $V_{10\text{-}16}$ = 6,1 V.

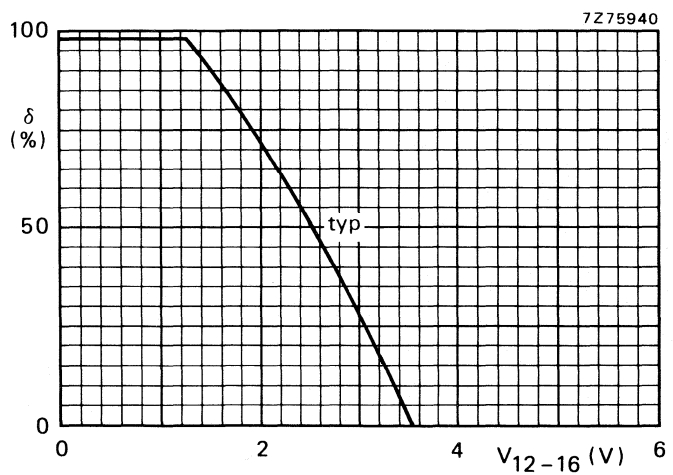


Fig. 9 Maximum duty factor limitation as a function of the voltage applied to pin 12; $V_{10\text{-}16}$ = 6,1 V.

HORIZONTAL COMBINATION

The TDA2593 is a monolithic integrated circuit intended for use in colour television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3500, TDA3510 and TDA3520. The circuit incorporates the following functions:

- horizontal oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage (φ_1)
- internal key pulse for phase detector (φ_1) (additional noise limiting)
- phase comparison between line flyback pulse and oscillator voltage (φ_2)
- larger catching range obtained by coincidence detector (φ_3; between sync and key pulse)
- switch for changing the filter characteristic and the gate circuit (VCR-operation)
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage with separate supply voltage for direct drive of thyristor deflection circuits
- low supply voltage protection

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}16}$	typ.	12 V
Supply current	I_1	typ.	30 mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$		3 to 4 V
Noise separator input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		3 to 4 V
Pulse duration switch input voltage			
at t = 7 μs (thyristor driving)	$V_{4\text{-}16}$		9,4 to $V_{1\text{-}16}$ V
at t = 14 μs + t_d (transistor driving)	$V_{4\text{-}16}$		0 to 3,5 V
at t = 0 (input 4 open or $V_{3\text{-}16}$ = 0)	$V_{4\text{-}16}$		5,4 to 6,6 V
Output signals			
Vertical sync output pulse (peak-to peak value)	$V_{8\text{-}16(p\text{-}p)}$	typ.	11 V
Burst gating output pulse (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	11 V
Line drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

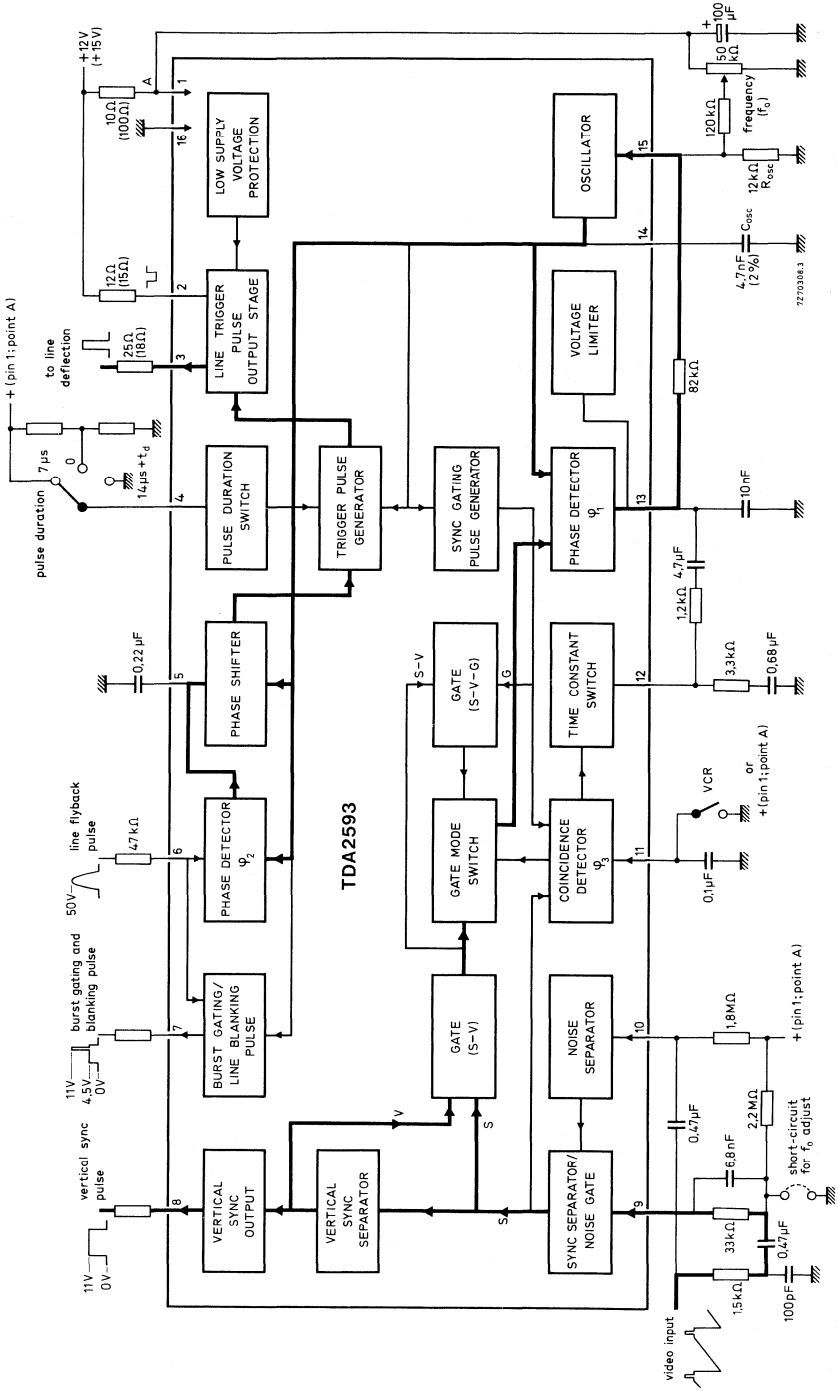


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
at pin 1 (voltage source)	V_{1-16}	max.	13,2 V
at pin 2	V_{2-16}	max.	18 V
Voltages			
Pin 4	V_{4-16}	max.	13,2 V
Pin 9	$\pm V_{9-16}$	max.	6 V
Pin 10	$\pm V_{10-16}$	max.	6 V
Pin 11	V_{11-16}	max.	13,2 V
Currents			
Pins 2 and 3 (thyristor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	650 mA
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400 mA
Pin 4	I_4	max.	1 mA
Pin 6	$\pm I_6$	max.	10 mA
Pin 7	$-I_7$	max.	10 mA
Pin 11	I_{11}	max.	2 mA
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature	T_{stg}		−25 to + 125 °C
Operating ambient temperature	T_{amb}		0 to + 70 °C

CHARACTERISTICS at V_{1-16} = 12 V; T_{amb} = 25 °C; measured in Fig. 1

Sync separator

Input switching voltage	V_{9-16}	typ.	0,8 V
Input keying current	I_9		5 to 100 μA
Input leakage current at V_{9-16} = −5 V	I_9	<	1 μA
Input switching current	I_9	⩽	5 μA
Switch off current	I_9	>	100 μA
		typ.	150 μA
Input signal (peak-to-peak value)	$V_{9-16(p-p)}$		3 to 4 V*

* Permissible range 1 to 7 V.

Noise separator				
Input switching voltage	V_{10-16}	typ.	1,4	V
Input keying current	I_{10}		5 to 100	μA
Input switching current	I_{10}	>	100	μA
		typ.	150	μA
Input leakage current at $V_{10-16} = -5$ V	I_{10}	<	1	μA
Input signal (peak-to-peak value)	$V_{10-16(p-p)}$		3 to 4	V *
Permissible superimposed noise signal (peak-to-peak value)	$V_{10-16(p-p)}$	<	7	V
Line flyback pulse				
Input current	I_6	typ.	1	mA
			0,02 to 2	mA
Input switching voltage	V_{6-16}	typ.	1,4	V
Input limiting voltage	V_{6-16}		−0,7 to + 1,4	V
Switching on VCR				
Input voltage	V_{11-16}		0 to 2,5	V
	V_{11-16}		9 to V_{1-16}	V
Input current	$-I_{11}$	<	200	μA
	I_{11}	<	2	mA
Pulse duration switch				
For t = 7 μs (thyristor driving)				
Input voltage	V_{4-16}		9,4 to V_{1-16}	V
Input current	I_4	>	200	μA
For t = 14 μs + t_d (transistor driving)				
Input voltage	V_{4-16}		0 to 3,5	V
Input current	$-I_4$	>	200	μA
For t = 0; $V_{3-16} = 0$ or input pin 4 open				
Input voltage	V_{4-16}		5,4 to 6,6	V
Input current	I_4	typ.	0	μA

* Permissible range 1 to 7 V.

Vertical sync pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{8\text{-}16(p\text{-}p)}$	>	10	V
		typ.	11	V
Output resistance	R_8	typ.	2	kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15	μs
Delay between trailing edge of input and output signal	t_{off}	typ.	t_{on}	μs
Burst gating pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	>	10	V
		typ.	11	V
Output resistance	R_7	typ.	70	Ω
Pulse duration; $V_{7\text{-}16}$ = 7 V	t_p	typ.	4	μs
			3,7 to 4,3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; $V_{7\text{-}16}$ = 7 V	t	typ.	2,65	μs
			2,15 to 3,15	μs
Output trailing edge current	I_7	typ.	2	mA
Line flyback-blanking pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$		4 to 5	V
Output resistance	R_7	typ.	70	Ω
Output trailing edge current	I_7	typ.	2	mA
Line drive pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5	V
Output resistance				
for leading edge of line pulse	R_3	typ.	2,5	Ω
for trailing edge of line pulse	R_3	typ.	20	Ω
Pulse duration (thyristor driving)				
$V_{4\text{-}16}$ = 9,4 to $V_{1\text{-}16}$ V	t_p	typ.	7	μs
			5,5 to 8,5	μs
Pulse duration (transistor driving)				
$V_{4\text{-}16}$ = 0 to 4 V; t_{fp} = 12 μs	t_p		$14 + t_d$	μs*
Supply voltage for switching off the output pulse	$V_{1\text{-}16}$	typ.	4	V
Overall phase relation				
Phase relation between middle of sync pulse and the middle of the flyback pulse	t	typ.	2,6	μs**
Tolerance of phase relation	$\lvert \Delta t \rvert$	<	0,7	μs

* t_d = switch-off delay of line output stage.
** Line flyback pulse duration t_{fp} = 12 μs.

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2. If additional adjustment is applied it can be arranged by current supply at pin 5 such that	$\Delta I_5/\Delta t$	typ.	30	$\mu A/\mu s$
Oscillator				
Threshold voltage low level	V_{14-16}	typ.	4,4	V
Threshold voltage high level	V_{14-16}	typ.	7,6	V
Discharge current	$\pm I_{14}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4,7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15,625	kHz
Spread of frequency	$\Delta f_o/f_o$	<	± 5	%*
Frequency control sensitivity	$\Delta f_o/\Delta I_{15}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	$\Delta f_o/f_o$	typ.	± 10	%
Influence of supply voltage on frequency	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	<	± 0,05	%*
Change of frequency when V_{1-16} drops to 5 V	Δf_o	<	± 10	%*
Temperature coefficient of oscillator frequency		<	$\pm 10^{-4}$	Hz/K*
Phase comparison φ_1				
Control voltage range	V_{13-16}		3,8 to 8,2	V
Control current (peak value)	$\pm I_{13M}$		1,9 to 2,3	mA
Output leakage current at V_{13-16} = 4 to 8 V	I_{13}	<	1	μA
Output resistance at V_{13-16} = 4 to 8 V	R_{13}	high ohmic		**
at V_{13-16} < 3,8 V or > 8,2 V	R_{13}	low ohmic		▲
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ beteeen pins 13 and 15)	Δf	typ.	± 780	Hz
Spread of catching and holding range	$\Delta(\Delta f)$	typ.	± 10	%*

* Excluding external component tolerances.
** Current source.
▲ Emitter follower.

Phase comparison φ_2 and phase shifter			
Control voltage range	$V_{5\text{-}16}$	5,4 to 7,6	V
Control current (peak value)	$\pm I_{5M}$	typ. 1	mA
Output resistance			
at $V_{5\text{-}16}$ = 5,4 to 7,6 V		high ohmic	*
at $V_{5\text{-}16}$ < 5,4 V or > 7,6 V	R_5	typ. 8	kΩ
Input leakage current			
$V_{5\text{-}16}$ = 5,4 to 7,6 V	I_5	< 5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	< 15	μs
Static control error	$\Delta t/\Delta t_d$	< 0,2	%
Coincidence detector φ_3			
Output voltage	$V_{11\text{-}16}$	0,5 to 6	V
Output current (peak value)			
without coincidence	I_{11M}	typ. 0,1	mA
with coincidence	$-I_{11M}$	typ. 0,5	mA
Time constant switch			
Output voltage	$V_{12\text{-}16}$	typ. 6	V
Output current (limited)	$\pm I_{12}$	< 1	mA
Output resistance			
at $V_{11\text{-}16}$ = 2,5 to 7 V	R_{12}	typ. 0,1	kΩ
at $V_{11\text{-}16}$ < 1,5 V or > 9 V	R_{12}	typ. 60	kΩ
Internal gating pulse			
Pulse duration	t_p	typ. 7,5	μs

* Current source.

HORIZONTAL COMBINATION

GENERAL DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in colour television receivers.

Features

- Positive video input; capacitively coupled (source impedance $< 200\ \Omega$)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- φ_1 phase control between horizontal sync and oscillator
- Coincidence detector φ_3 for automatic time-constant switching; overruled by the VCR switch
- Time-constant switch between two external time-constants or loop-gain; both controlled by the coincidence detector φ_3
- φ_1 gating pulse controlled by coincidence detector φ_3
- Mute circuit depending on TV transmitter identification
- φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4 V or higher than 8 V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot-suppressor controlled by the line flyback control

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_{15\text{-}5} = V_P$	typ.	12 V
Sync pulse amplitude (positive video)	$V_{i(p\text{-}p)}$	min.	50 mV
Horizontal output current	I_4	typ.	50 mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

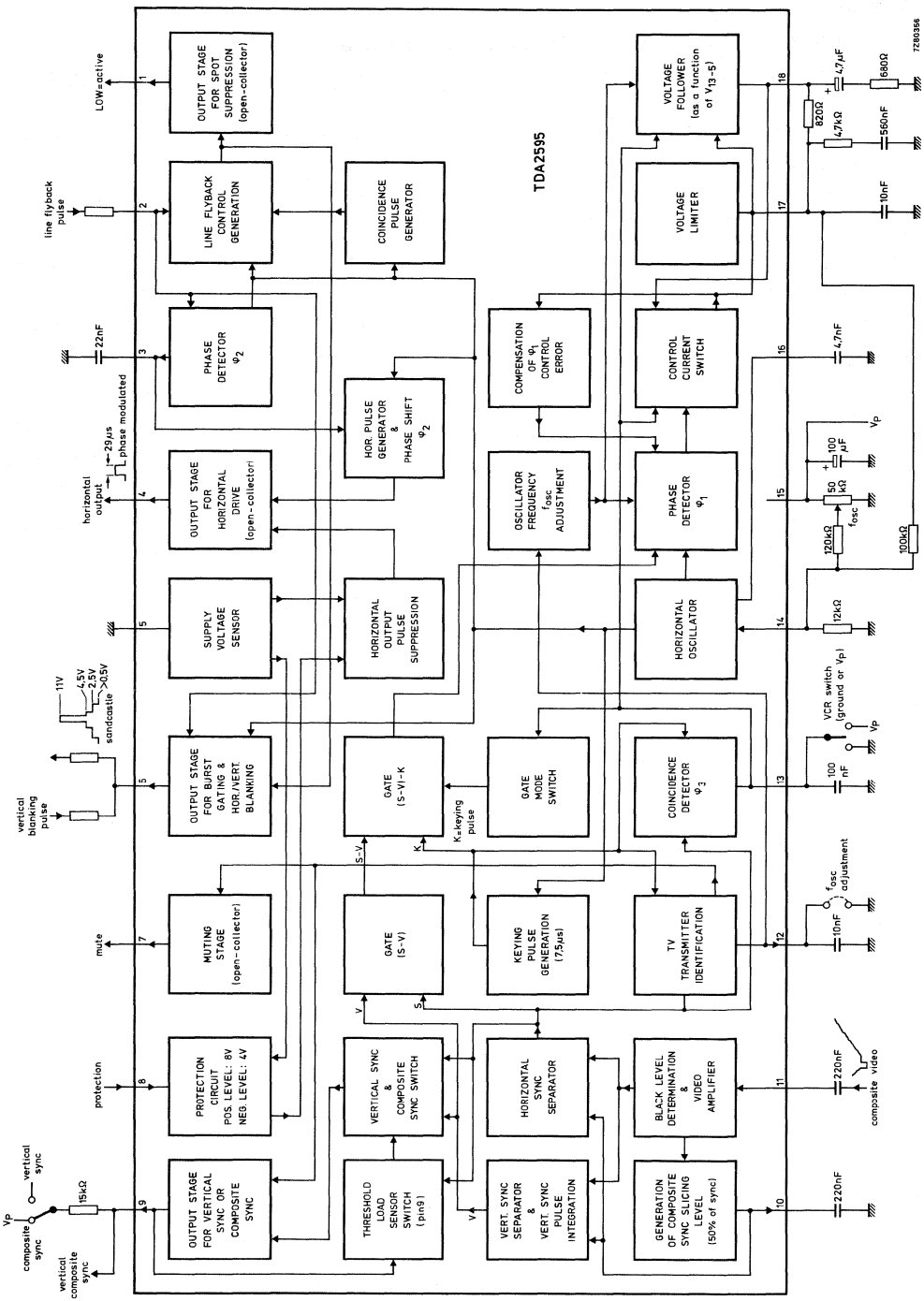


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_{15-5} = V_P$	max.	13,2	V
Voltages at:				
pins 1, 4 and 7	$V_{1;4;7-5}$	max.	18	V
pins 8, 13 and 18	$V_{8;13;18-5}$	max.	V_P	V
pin 11 (range)	V_{11-5}		−0,5 to + 6	V
Currents at:				
pin 1	I_1	max.	10	mA
pin 2 (peak value)	$\pm I_{2M}$	max.	10	mA
pin 4	I_4	max.	100	mA
pin 6 (peak value)	$\pm I_{6M}$	max.	6	mA
pin 7	I_7	max.	10	mA
pin 8 (range)	I_8		−5 to + 1	mA
pin 9 (range)	I_9		−10 to + 3	mA
pin 18	$\pm I_{18}$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−25 to + 125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Composite video input and sync separator (pin 11) (internal black level determination)					
Input signal (positive video; standard signal; peak-to-peak value)	$V_{11\text{-}5(p\text{-}p)}$	0,2	1	3	V
Sync pulse amplitude (independent of video content)	$V_{11\text{-}5(p\text{-}p)}$	50	–	–	mV
Generator resistance	R_G	–	–	200	Ω
Input current during:					
video	I_{11}	–	5	–	μA
sync pulse	$-I_{11}$	–	40	–	μA
black level	$-I_{11}$	–	25	–	μA
Composite sync generation (pin 10) horizontal slicing level at 50% of the sync pulse amplitude for $V_{11\text{-}5(p\text{-}p)} < 1{,}5$ V					
Capacitor current during:					
video	I_{10}	–	16	–	μA
sync pulse	$-I_{10}$	–	170	–	μA
Vertical sync pulse generation slicing level at 30% (60% between black level and horizontal slicing level); pin 9					
Output voltage	$V_{9\text{-}5}$	10	–	–	V
Pulse duration	t_p	–	190	–	μs
Delay with respect to the vertical sync pulse (leading edge)	t_d	–	45	–	μs
Pulse-mode control					
output current for vertical sync pulse (dual integrated)		no current applied at pin 9			
output current for horizontal and vertical sync pulse (non-integrated separated signal)		current applied via a resistor of 15 kΩ from V_P to pin 9			

parameter	symbol	min.	typ.	max.	unit
Horizontal oscillator (pins 14 and 16)					
Frequency; free running	f_{osc}	–	15 625	–	Hz
Reference voltage for f_{osc}	V_{14-5}	–	6	–	V
Frequency control sensitivity	$\Delta f_{osc}/\Delta I_{14}$	–	31	–	Hz/μA
Adjustment range of circuit Fig. 1	Δf_{osc}	–	± 10	–	%
Spread of frequency	Δf_{osc}	–	–	5	%
Frequency dependency (excluding tolerance of external components)					
with supply voltage (V_P = 12 V)	$\frac{\Delta f_{osc}/f_{osc}}{\Delta V_{15-5}/V_{15-5}}$	–	± 0,05	–	
with supply voltage drop of 5 V	Δf_{osc}	–	–	10	%
with temperature	TC	–	–	$\pm 10^{-4}$	K^{-1}
Capacitor current during:					
discharging	$+I_{16}$	–	1024	–	μA
charging	$-I_{16}$	–	313	–	μA
Sawtooth voltage timing (pin 14)					
rise time	t_r	–	49	–	μs
fall time	t_f	–	15	–	μs
Horizontal output pulse (pin 4)					
Output voltage LOW at I_4 = 50 mA	V_{4-5}	–	–	0,5	V
Pulse duration (HIGH)	t_p	–	29 ± 1,5	–	μs
Supply voltage for switching off the output pulse (pin 15)	V_P	–	4	–	V
Hysteresis for switching on the output pulse	ΔV_P	–	250	–	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_1 (pin 17)					
Control voltage range	$V_{17\text{-}5}$	3,55	–	8,3	V
Leakage current at $V_{17\text{-}5}$ = 3,55 to 8,3 V	I_{17}	–	–	1	μA
Control current for external time-constant switch	$\pm I_{17}$	1,8	2	2,2	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5} < 2$ V or $V_{13\text{-}5} > 9,5$ V	$\pm I_{17}$	–	8	–	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5}$ = 2 to 9,5 V	$\pm I_{17}$	1,8	2	2,2	mA
Horizontal oscillator control					
control sensitivity	S_φ	6	–	–	kHz/μs
catching and holding range	$\pm\Delta f_{osc}$	–	680	–	Hz
spread of catching and holding range	$\pm\Delta f_{osc}$	–	10	–	%
Internal keying pulse at $V_{13\text{-}5}$ = 2,9 to 9,5 V	t_p	–	7,5	–	μs
Time-constant switch					
slow time-constant at	$V_{13\text{-}5}$	9,5	–	2	V
fast time-constant at	$V_{13\text{-}5}$	2	–	9,5	V
Impedance converter offset voltage (slow time-constant)	$\pm V_{17\text{-}18}$	–	–	3	mV
Output resistance					
slow time-constant	$R_{18\text{-}5}$	–	–	10	Ω
fast time-constant	$R_{18\text{-}5}$	high impedance			
Leakage current	I_{18}	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Coincidence detector φ_3 (pin 13)					
Output voltage					
without coincidence with composite video signal	V_{13-5}	–	–	1	V
without coincidence without composite video signal (noise)	V_{13-5}	–	–	2	V
with coincidence with composite video signal	V_{13-5}	–	6	–	V
Output current					
without coincidence with composite video signal	I_{13}	–	50	–	μA
with coincidence with composite video signal	$-I_{13}$	–	300	–	μA
Switching current					
at $V_{13-5} = V_P - 0{,}5$ V	I_{13}	–	–	100	μA
at $V_{13-5} = 0{,}5$ V (average value)	$I_{13(av)}$	–	–	100	μA
Phase comparison φ_2 (pins 2 and 3) (see note 1)					
Input for line flyback pulse (pin 2)					
Switching level for φ_2 comparison and flyback control	V_{2-5}	–	3	–	V
Switching level for horizontal blanking	V_{2-5}	–	0,3	–	V
Input voltage limiting	V_{2-5}	–	–0,7	–	V
	or:	–	+4,5	–	V
Switching current					
at horizontal flyback	I_2	0,01	1	–	mA
at horizontal scan	I_2	–	–	2	μA
Maximum negative input current	$-I_2$	–	–	500	μA
Phase detector output (pin 3)					
Control current for φ_2	$\pm I_3$	–	1	–	mA
Control range	$\Delta t_{\varphi 2}$	–	19	–	μs
Static control error	$\Delta t/\Delta t_d$	–	–	0,2	%
Leakage current	I_3	–	–	5	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_2 (pins 2 and 3) (continued)					
Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at t_{fp} = 12 μs (note 2)	Δt	–	2,6 ± 0,7	–	μs
If additional adjustment is required, it can be arranged by applying a current at pin 3	$\Delta I/\Delta t$	–	30	–	μA/μs
Burst gating pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	10	11	–	V
Pulse duration	t_p	3,7	4	4,3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at V_{6-5} = 7 V	$t_{\varphi 6}$	2,15	2,65	3,15	μs
Output trailing edge current	I_6	–	2	–	mA
Horizontal blanking pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	4,1	4,5	4,9	V
Output trailing edge current	I_6	–	2	–	mA
Saturation voltage at horizontal scan	V_{6-5sat}	–	–	0,5	V
Clamping circuit for vertical blanking pulse (pin 6) (note 3)					
Output voltage at I_6 = 2,8 mA	V_{6-5}	2,15	2,5	3	V
Minimum output current at $V_{6-5} > 2,15$ V	I_{6min}	–	2,3	–	mA
Maximum output current at $V_{6-5} < 3$ V	I_{6max}	–	3,3	–	mA
TV-transmitter identification (pin 12) (note 4)					
Output voltage					
no TV transmitter	V_{12-5}	–	–	1	V
TV transmitter identified	V_{12-5}	7	–	–	V

parameter	symbol	min.	typ.	max.	unit
Mute output (pin 7)					
Output voltage at I_7 = 3 mA no TV transmitter	V_{7-5}	–	–	0,5	V
Output resistance at I_7 = 3 mA no TV transmitter	R_{7-5}	–	–	100	Ω
Output leakage current at $V_{12-5} > 3$ V TV transmitter identified	I_7	–	–	5	μA
Protection circuit (beam-current/ EHT voltage protection) (pin 8)					
No-load voltage for $I_8 = 0$ (operative condition)	V_{8-5}	–	6	–	V
Threshold at positive-going voltage	V_{8-5}	–	8 ± 0,8	–	V
Threshold at negative-going voltage	V_{8-5}	–	4 ± 0,4	–	V
Current limiting for V_{8-5} = 1 to 8,5 V	$\pm I_8$	–	60	–	μA
Input resistance for $V_{8-5} > 8,5$ V	R_{8-5}	–	3	–	kΩ
Internal response delay of threshold switch	t_d	–	10	–	μs
Control output of line flyback pulse control (pin 1)					
Saturation voltage at standard operation; I_1 = 3 mA	V_{1-5sat}	–	–	0,5	V
Output leakage current in case of disturbance of line flyback pulse	I_1	–	–	5	μA

Notes to the characteristics

1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase modulated (φ_2) horizontal output pulse with constant duration.
2. t_{fp} is the line flyback pulse duration.
3. Three-level sandcastle pulse.
4. If pin 12 is connected to V_P the vertical output is active independent of synchronization state.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P	6 to 35	V
Repetitive peak output current	I_{ORM}	< 1,5	A
Output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	typ. 4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ. 5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ. 0,3	%
Input impedance	$\|Z_i\|$	typ. 45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ. 25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ. 55	mV
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

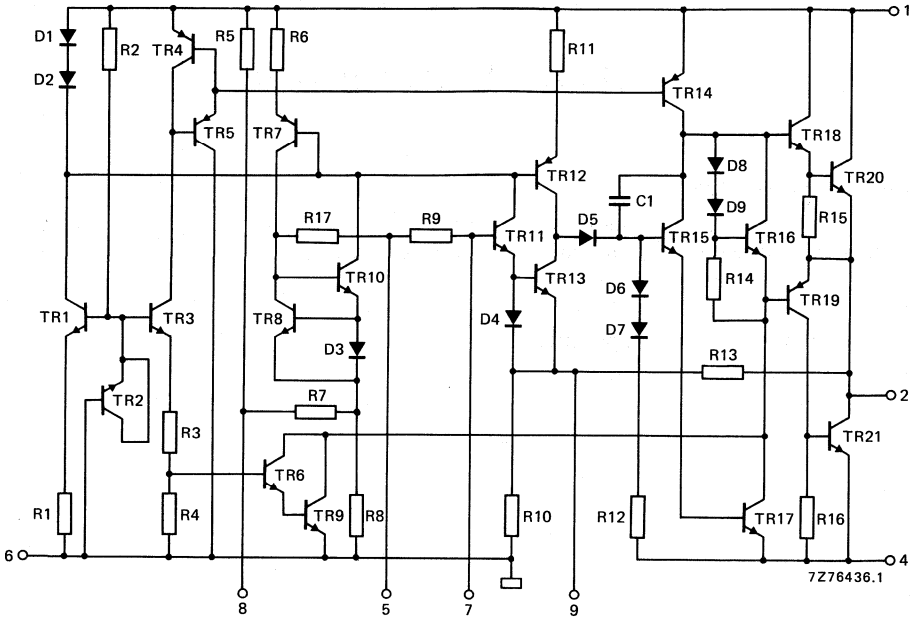


Fig. 1 Circuit diagram; pin 3 not connected.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA2613 is a hi-fi audio power amplifier encapsulated in a 9-lead SIL plastic power package. The device is especially designed for mains fed applications (e.g. tv and radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 40 V
Output power at THD = 0,5%, V_P = 24 V	P_O	typ.	6 W
Voltage gain	G_V	typ.	30 dB
Supply voltage ripple rejection	SVRR	typ.	60 dB
Noise output voltage	$V_{no(rms)}$	typ.	70 μV

PACKAGE OUTLINE

TDA2613: 9-lead SIL; plastic power (SOT110B).

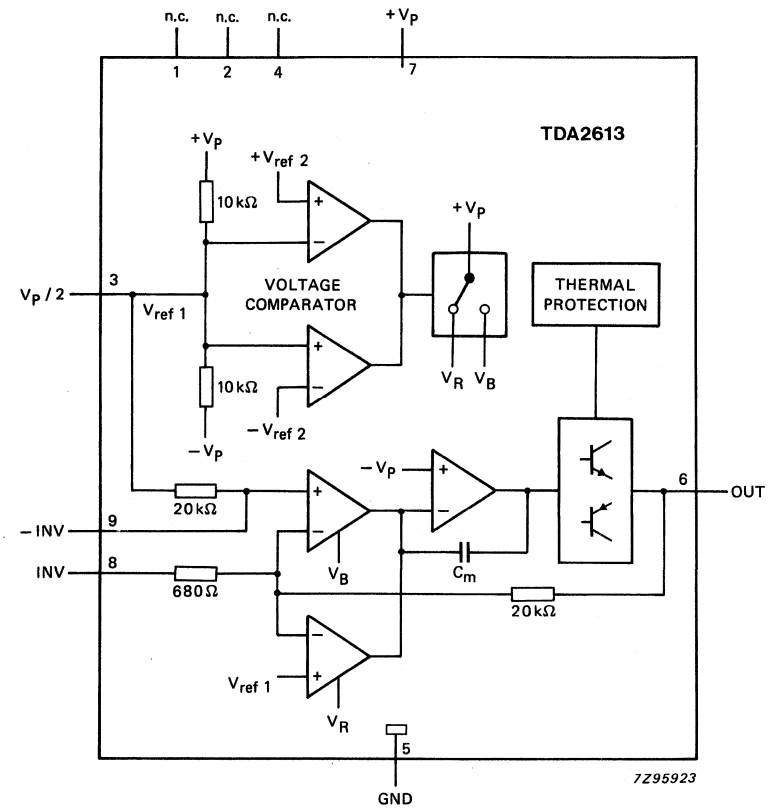


Fig. 1 Block diagram.

PINNING

1.	n.c.	not connected	5.	GND	ground (asymmetrical) / negative supply (symmetrical)
2.	n.c.	not connected	6.	OUT	output
3.	$V_P/2$	½ V_P (asymmetrical) / ground (symmetrical)	7.	+V_P	positive supply
4.	n.c.	not connected	8.	INV	inverting input
			9.	−INV	non-inverting input

VERTICAL DEFLECTION CIRCUIT

The TDA2653A is a monolithic integrated circuit for vertical deflection in large screen colour television receivers.

The circuit incorporates the following functions:

- Oscillator; switch capability for 50 Hz/60 Hz operation
- Synchronization circuit
- Blanking pulse generator with guard circuit
- Sawtooth generator with buffer stage
- Preamplifier with fed-out inputs
- Output stage with thermal and short-circuit protection
- Flyback generator
- Voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9-8} = V_S$	typ.	26	V
Supply current (pin 5 + pin 9)*	$I_5 + I_9 = I_S$	typ.	325	mA
Output current (peak-to-peak value)*	$I_{6(p-p)}$	typ.	1,7	A
Maximum output current (peak-to-peak value)	$I_{6(p-p)}$	max.	2,6	A
Picture frequency	f		50 Hz/60	Hz
Sync input pulse (peak-to-peak value)	$V_{2-8(p-p)}$	$\geqslant$	1	V
Thermal resistance from junction to mounting base	$R_{th\ j-mb}$	$\leqslant$	5	K/W

* for 45 AX systems

PACKAGE OUTLINE

13-lead SIL; plastic power (SOT141RGA).

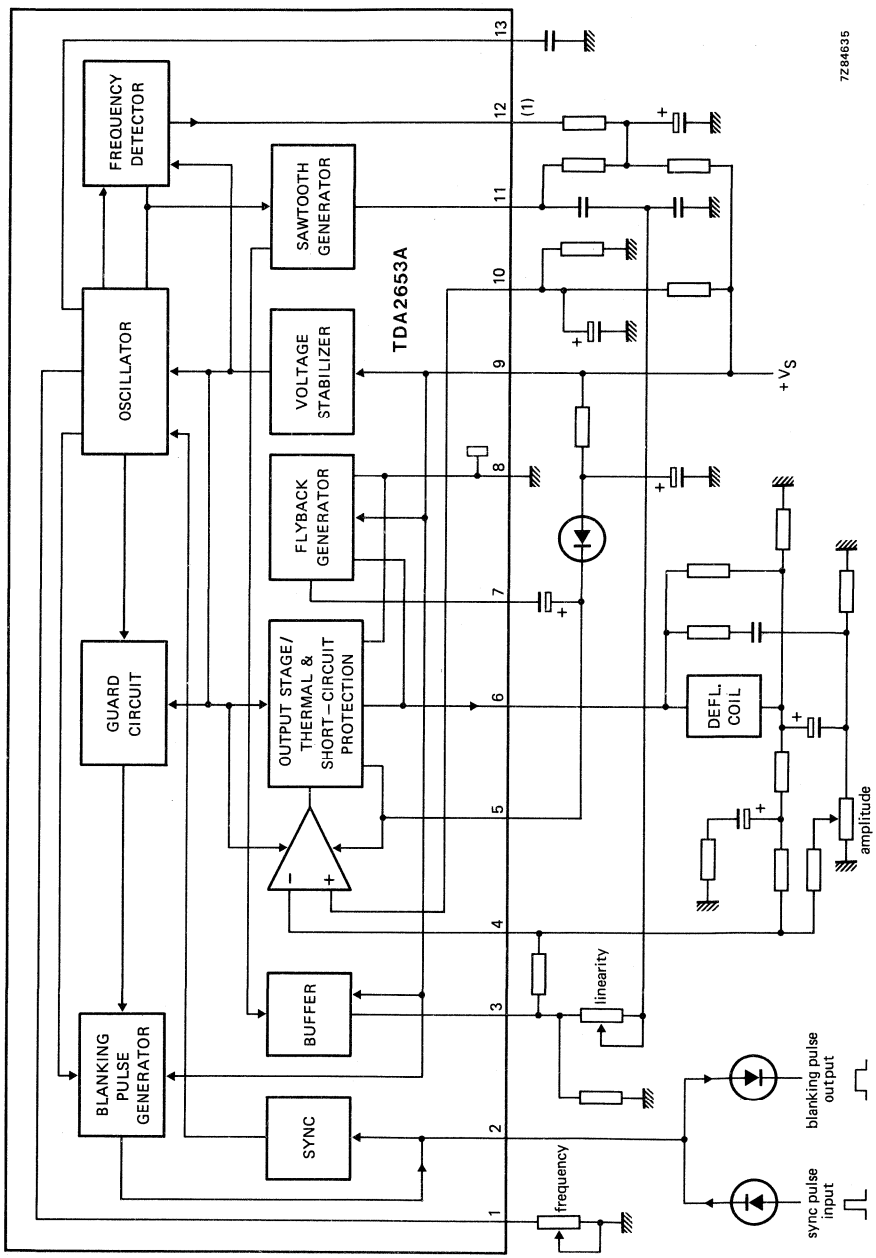


Fig. 1 Block diagram.

(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_{9-8} = V_S$	max.	40 V
Supply voltage output stage (pin 5)	V_{5-8}	max.	60 V
Voltages			
Pin 3	V_{3-11}	max.	7 V
Pin 13	V_{13-8}	max.	7 V
Pins 4 and 10	$V_{4;10-8}$	max.	24 V
Pin 6	V_{6-8}	max.	60 V
	$-V_{6-8}$	max.	0 V
Pins 7 and 11	$V_{7;11-8}$	max.	40 V
Currents			
Pin 1	I_1	max.	0 mA
	$-I_1$	max.	1 mA
Pin 2	$\pm I_2$	max.	10 mA
Pin 3	I_3	max.	0 mA
	$-I_3$	max.	5 mA
Pin 7	I_7	max.	1,3 A
	$-I_7$	max.	1,5 A
Pin 11	I_{11}	max.	50 mA
	$-I_{11}$	max.	1 mA
Pin 12	I_{12}	max.	3 mA
	$-I_{12}$	max.	0 mA

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

Storage temperature range	T_{stg}	−25 to + 150 °C
Operating ambient temperature range	T_{amb}	0 °C to limiting value

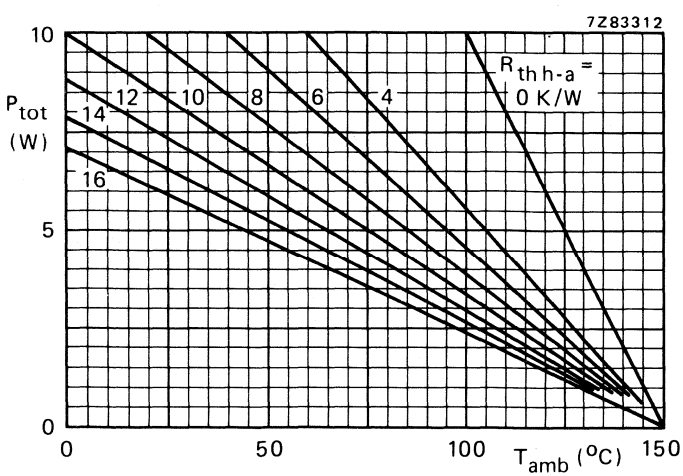


Fig. 2 Total power dissipation. $R_{th\ h-a}$ includes $R_{th\ mb-h}$ which is expected when heat-sink compound is used. $R_{th\ j-mb} \leqslant 5$ K/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

Supply voltage/output stage			
Supply voltage	$V_{9-8} = V_S$		9 to 30 V
Output voltage			
at $-I_6$ = 1,1 A	V_{6-8}	⩾	$V_{5-8} - 2,2$ V
		typ.	$V_{5-8} - 1,9$ V
at I_6 = 1,1 A	V_{6-8}	typ.	1,3 V
		⩽	1,6 V
Flyback generator output voltage at $-I_7$ = 1,1 A	V_{7-8}	typ.	$V_S - 2,2$ V
Peak output current	$\pm I_6$	⩽	1,3 A
Flyback generator peak current	$\pm I_7$	⩽	1,3 A
Feedback			
Input quiescent current	$-I_{4;10}$	typ.	0,1 μA
Synchronization			
Sync input pulse	V_{2-8}		1 to 12 V
Tracking range		typ.	28 %
Oscillator/sawtooth generator			
Oscillator frequency control input voltage	V_{1-8}		6 to 9 V
Sawtooth generator output voltage	V_{3-8}		0 to $V_S - 1$ V
	V_{11-8}		0 to $V_S - 2$ V
Sawtooth generator output current	$-I_3$		0 to 4 mA
	I_{11}	⩾	−2 μA
		⩽	+30 mA
Oscillator temperature dependency			
T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	typ.	10^{-4} K^{-1}
Oscillator voltage dependency			
V_S = 10 to 30 V	$(\Delta f/f)/\Delta V_S$	typ.	4×10^{-4} V^{-1}
Blanking pulse generator			
Output voltage			
at V_S = 24 V; I_2 = 1 mA	V_{2-8}	typ.	18,5 V
Output current	$-I_2$	⩽	3 mA
Output resistance	R_{2-8}	typ.	410 Ω
Blanking pulse duration at 50 Hz sync	t_b	typ.	1,4 ± 0,07 ms
50 Hz/60 Hz switch capability			
Saturation voltage; LOW voltage level	V_{12-8}	typ.	1 V
Output leakage current	I_{12}	typ.	1 μA

Thermal resistance/junction temperature

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	5 K/W
Junction temperature; switching point thermal protection	T_j	typ.	150 ± 8 °C

PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply (V_S)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

APPLICATION INFORMATION

The function is described against the corresponding pin number

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA.

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The DC voltage is proportional to the output voltage (DC feedback). The AC voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (AC feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

APPLICATION INFORMATION (continued)

10. Reference voltage of preamplifier

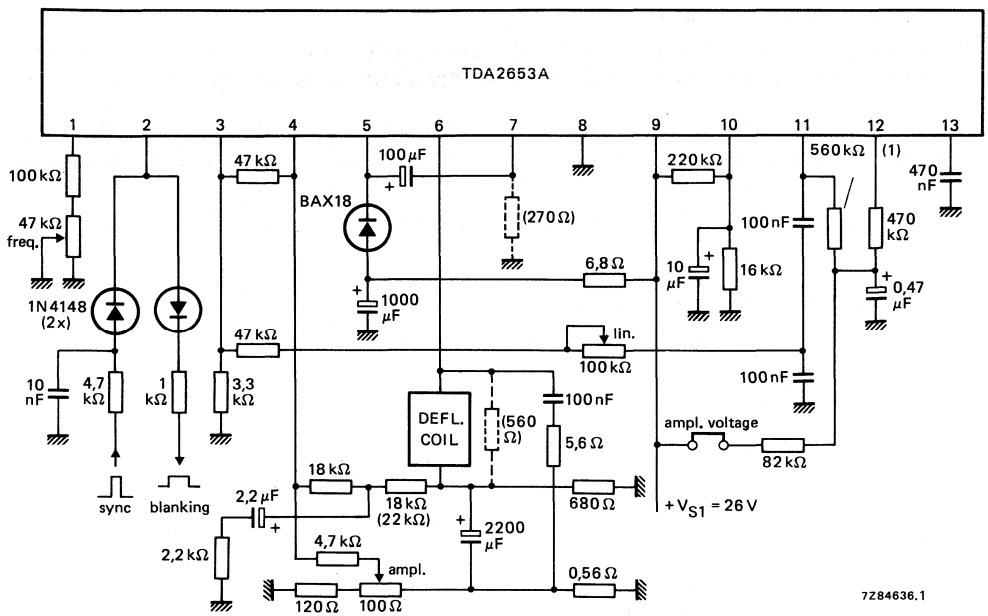
    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

    This sawtooth capacitor has been split to realize linearity control.

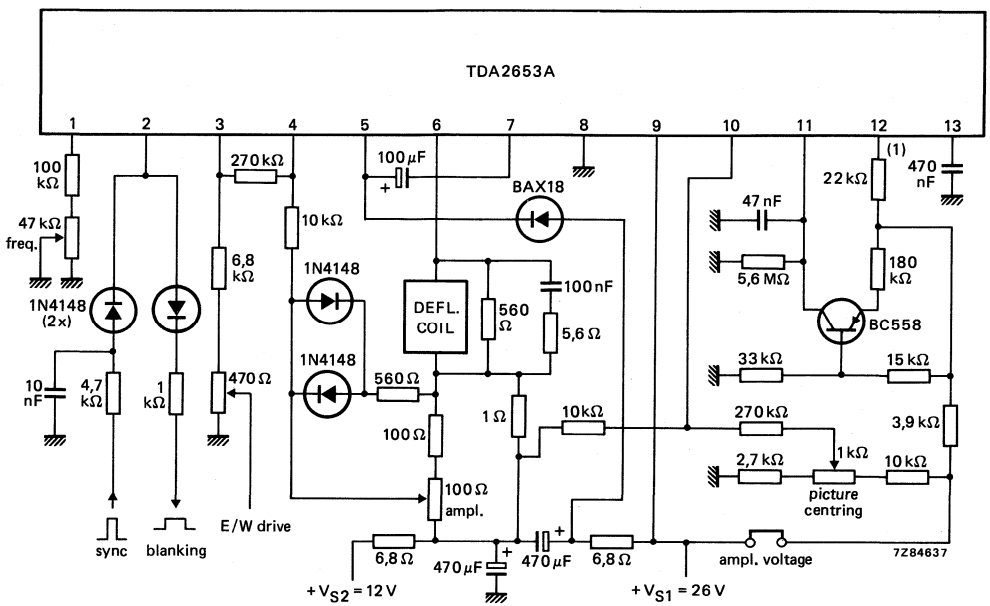
12. 50 Hz/60 Hz switching level

    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit for 45AX system (26 V).



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 4 Typical vertical deflection circuit for 45 AX system (V_{S1} = 26 V, V_{S2} = 12 V) in quasi-bridge connection.

VERTICAL DEFLECTION CIRCUIT

The TDA2654 is a monolithic integrated circuit for vertical deflection in monochrome and tiny-vision colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Sawtooth generator
- S-correction and linearity circuit
- Comparator and drive circuit
- Output stage
- Flyback dissipation limiting circuit
- Supply for pre-stages via internal voltage divider
- Thermal protection circuit
- Controlled switch-on

QUICK REFERENCE DATA

Supply voltage range (ref. to tab = ground)	V_P		10 to 35	V
Output current (peak-to-peak value)	$I_{9(p-p)}$	max.	2	A
Total power dissipation	P_{tot}	max.	5	W
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to tab	$R_{th\ j\text{-}tab}$	=	12	°C/W

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

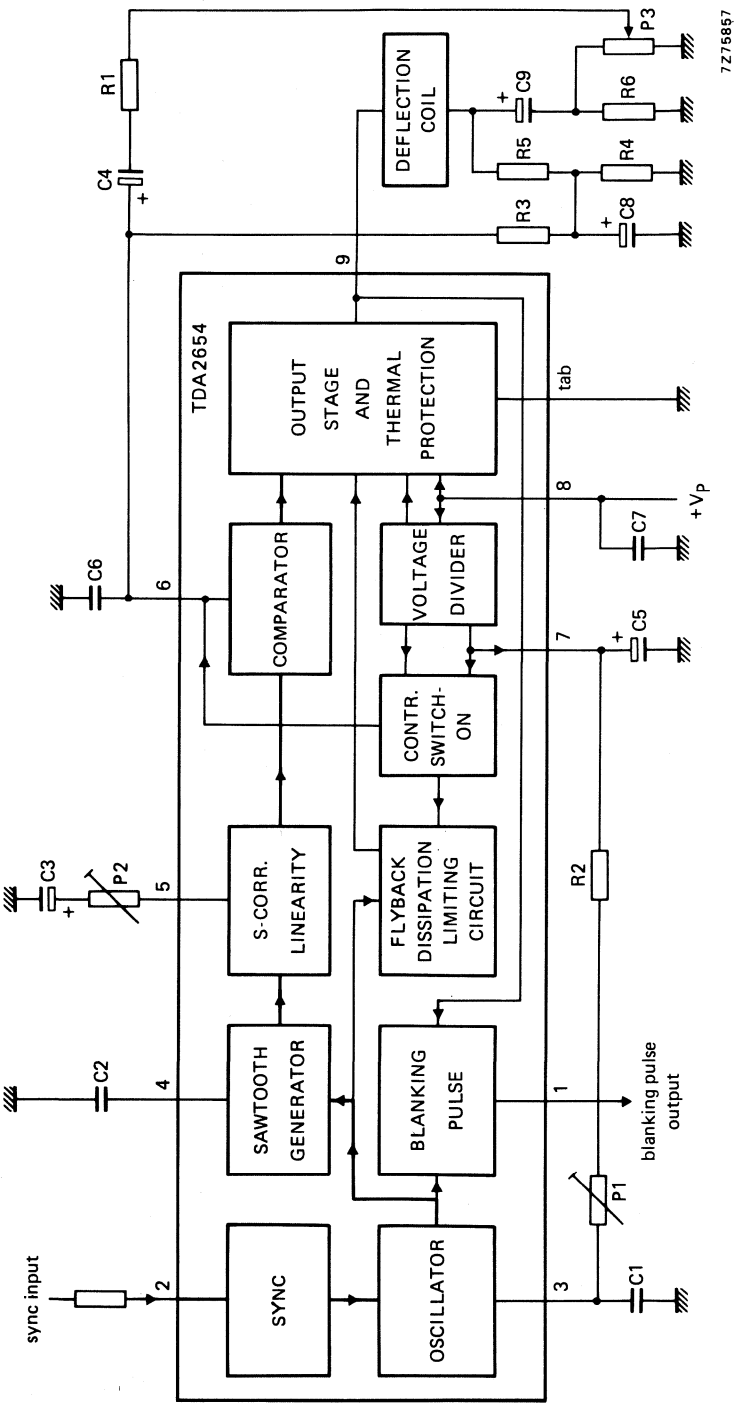


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

All voltages and currents refer to the tab (ground) connection.

Voltages			
Pin 2	V_2	max.	5 V
Pin 3	V_3	max.	17 V
Pin 4	V_4	max.	17 V
Pin 5	V_5	max.	6 V
Pin 6	V_6	max.	13 V
Pin 7	V_7	max.	18 V
Pin 8	V_8 (V_P)	max.	35 V
Currents			
Pin 1	$+I_1$	max.	1 mA
	$-I_1$	max.	5 mA
Pin 2	I_2	max.	2,5 mA
Pin 3	I_3	max.	30 mA
Pin 4	I_4	max.	30 mA
Pin 5	$\pm I_5$	max.	1 mA
Pin 6	$\pm I_6$	max.	3 mA
Pin 9 (repetitive)	$\pm I_9$	max.	1 A
Pin 9 (non-repetitive)	$\pm I_9$	max.	1,5 A
Total power dissipation (see also Fig. 2)	P_{tot}	max.	5 W
Storage temperature	T_{stg}	−25 to + 150	°C
Operating junction temperature	T_j	max.	150 °C

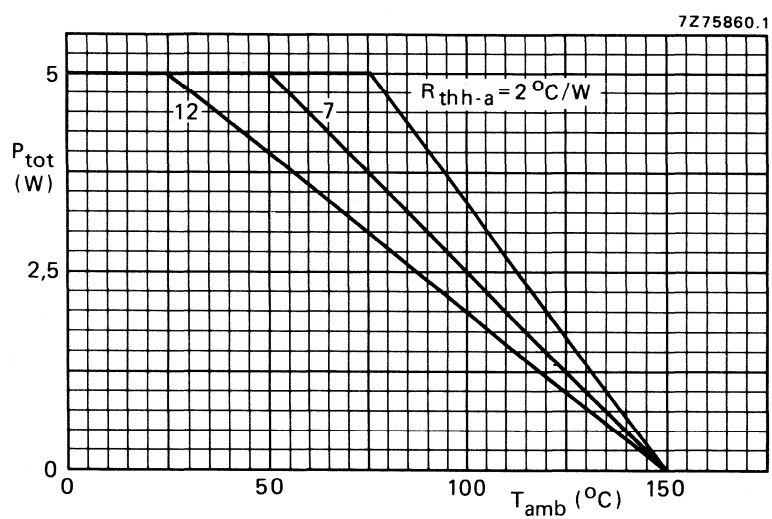


Fig. 2 Total power dissipation. The graph takes into account an $R_{th\ tab\text{-}h}$ = 1 °C/W which is to be expected when the tab is connected to a heatsink with one 3 mm bolt, without using heatsink compound. $R_{th\ j\text{-}tab}$ = 12 °C/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified; voltages and currents ref. to tab (ground)

			monochrome (Fig. 3)	tiny-vision colour (Fig. 4)	
Supply voltage (pin 8)	V_P	typ.	25	31	V
Supply current (pin 8)	I_P	typ.	165	150	mA
Total power dissipation	P_{tot}	typ.	3,1	3,5	W
Output voltage (peak-to-peak value)	$V_{9\,(p\text{-}p)}$	typ.	22	28	V
Blanking pulse; I_1 = 1 mA	V_1	typ.	11,5	14,5	V
Blanking pulse duration	t_p	typ.	1,3	1,4	ms
D.C. input voltage (pin 6)	V_6	typ.	3,4	4,4	V
Deflection current (peak-to-peak value)	$I_{9\,(p\text{-}p)}$	typ.	1,1	0,92	A
Flyback time	t	typ.	1,3	1,32	ms
Free running oscillator frequency	f_{osc}	typ.	46	46	Hz
Oscillator thermal drift		typ.	−0,01	−0,01	Hz/°C
Oscillator voltage shift		typ.	−0,13	−0,12	Hz/V
Tracking range oscillator		typ.	18	18	%
Synchronization input voltage	V_2	>	1	1	V
Voltage divider ratio	V_7/V_8	typ.	0,52	0,52	
Input resistance pin 7	R_7	typ.	2,8	2,8	kΩ
Recommended thermal resistance of heatsink for T_{amb} up to 70 °C	$R_{th\ h\text{-}a}$	<	13	10	°C/W

PINNING

1. Blanking pulse output
2. Synchronization input
3. Oscillator timing network
4. Sawtooth generator
5. S-correction and linearity control
6. Feedback input
7. Voltage divider
8. Positive supply
9. Output

Tab. Negative supply (ground)

APPLICATION INFORMATION (see also Fig. 1)

The function is described against the corresponding pin number

1. Blanking pulse output

When the IC is adjusted on a free running frequency of 46 Hz the internal blanking pulse generator delivers a blanking pulse with a duration between 1,2 ms and 1,5 ms. The circuit is, however, made such that when the flyback time of the deflection current is longer, the blanking pulse corresponds to the flyback time. The output voltage is also high when the voltage at pin 9 is lower than nominal 5 V. An external blanking circuit is recommended when tiny-vision receivers are operated from a car-battery.

2. Synchronization input

The oscillator has to be synchronized by a positive-going pulse. The circuit is made such that synchronization is inhibited during the flyback time.

APPLICATION INFORMATION (continued)

3. Oscillator

The oscillator frequency is set by the potentiometer P1 and resistor R2 between pins 3 and 7 and capacitor C1 between pin 3 and ground. For 50 Hz systems the free running frequency is preferably adjusted to 46 Hz.

4. Sawtooth generator

This pin supplies the charging and discharging currents of the capacitor between pin 4 and ground (C2).

5. S-correction and linearity control

The amount of S-correction can be set by the value of C3. For 110° deflection coils, e.g. AT1040/15, a capacitor of 15 μF will give the right value for S-correction. For 90° deflection systems (e.g. AT1235/00) a nearly linear deflection current is required, this can be achieved by increasing C3 to 100 μF. The linearity can be adjusted by potentiometer P2.

6. Output current feedback

To this pin is applied a part of the output current measured across R6 and superimposed on a d.c. voltage derived from the voltage across the output coupling capacitor. This signal is compared with the internal reference sawtooth. The internal reference sawtooth has an amplitude of about 0,6 V peak to peak and a d.c. level of about 3,4 V, for a supply voltage of 25 V at pin 8.

7. Internal voltage divider decoupling

The voltage on this pin is about half the supply voltage at pin 8 and is applied to the bases of emitter followers supplying the pre-stages of the IC. This voltage controls the amplitude of the internal reference sawtooth. In this way tracking with the line deflection system is achieved when the supply voltage at pin 8 is derived from the line output transformer.

8. Positive supply

The value depends on the deflection coil.

9. Output

The deflection coil is connected to ground via coupling capacitor C9 and current sensing resistor R6. The line frequency superimposed on the output voltage may be too high due to the current feedback system. The line frequency ripple can be decreased by connecting a resistor across the deflection coil. The flyback time can be influenced by the resistor divider (R4, R5) for the d.c. feedback to pin 6. It should be noted that the output voltage shows a negative swing of about 1 V during the first (positive current) part of the flyback.

Tab

The tab is used as negative supply (ground) connection. Therefore, the tab should be well connected to the negative side of the power supply.

Controlled switch-on

This feature is achieved by charging the a.c. coupling capacitor (C4; connected to pin 6) from an internal current source of about 2 mA (voltage limited to maximum 15 V) for a short period after switch-on. The charging time can be influenced by the value of C5 (connected to pin 7). Discharging of C4 results in a slowly increasing deflection current after a delay of about 1 second. The blanking voltage at pin 1 is high during this delay.

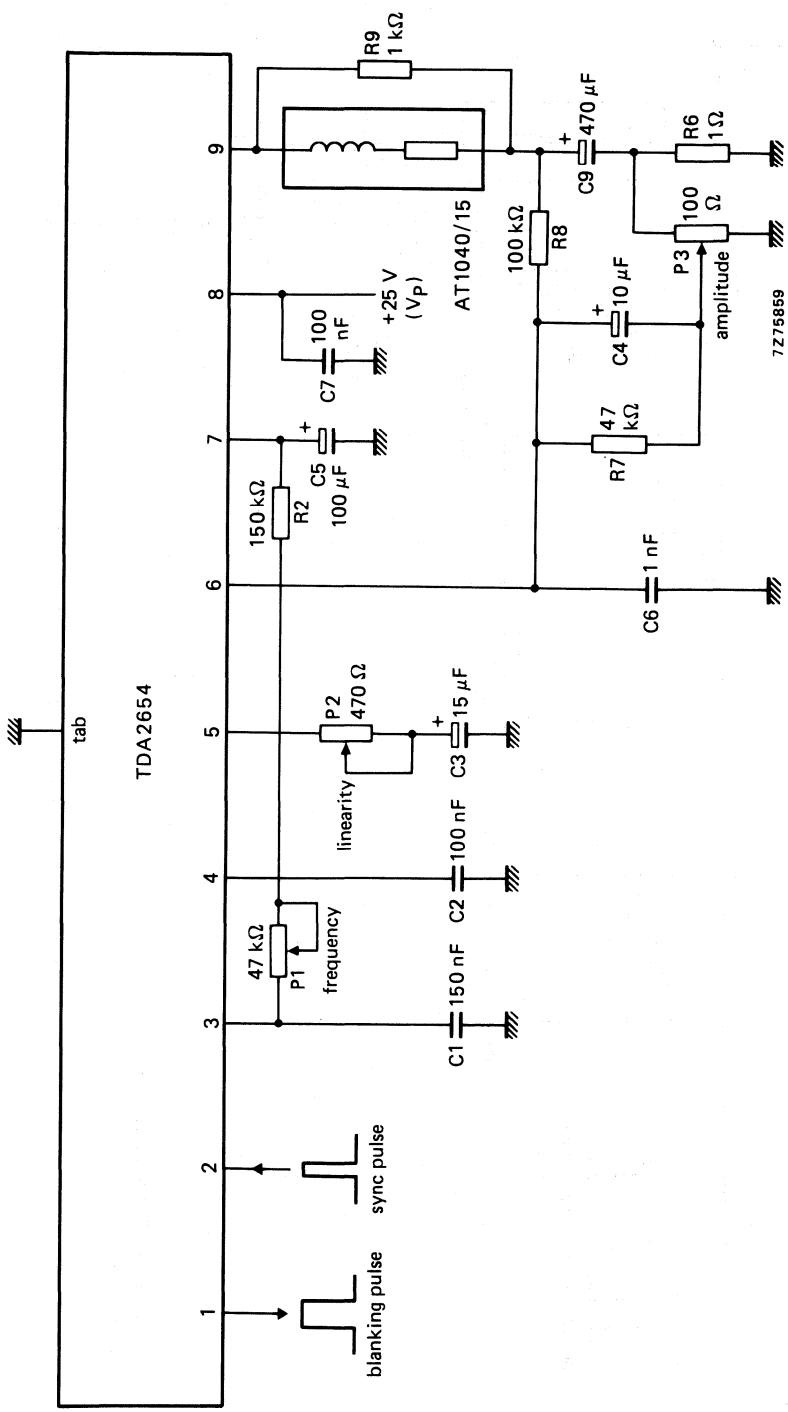


Fig. 3 Monochrome 110° vertical deflection system.

APPLICATION INFORMATION (continued)

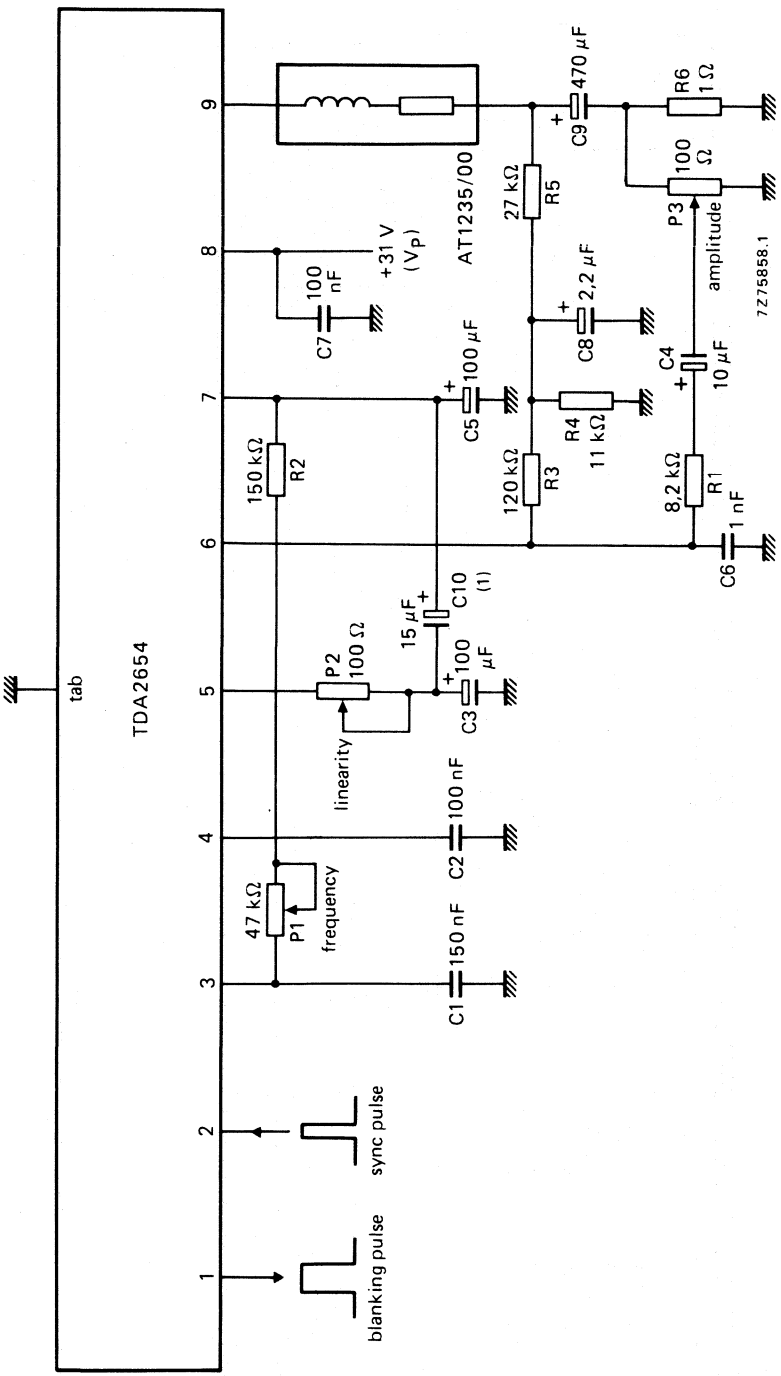


Fig. 4 Colour 90° vertical deflection system.

(1) Only required when rapid variations in the supply voltage are expected.

VERTICAL DEFLECTION CIRCUIT

The TDA2658 is a monolithic integrated circuit for vertical deflection in small screen colour television receivers and monitors.

The circuit incorporates the following functions:

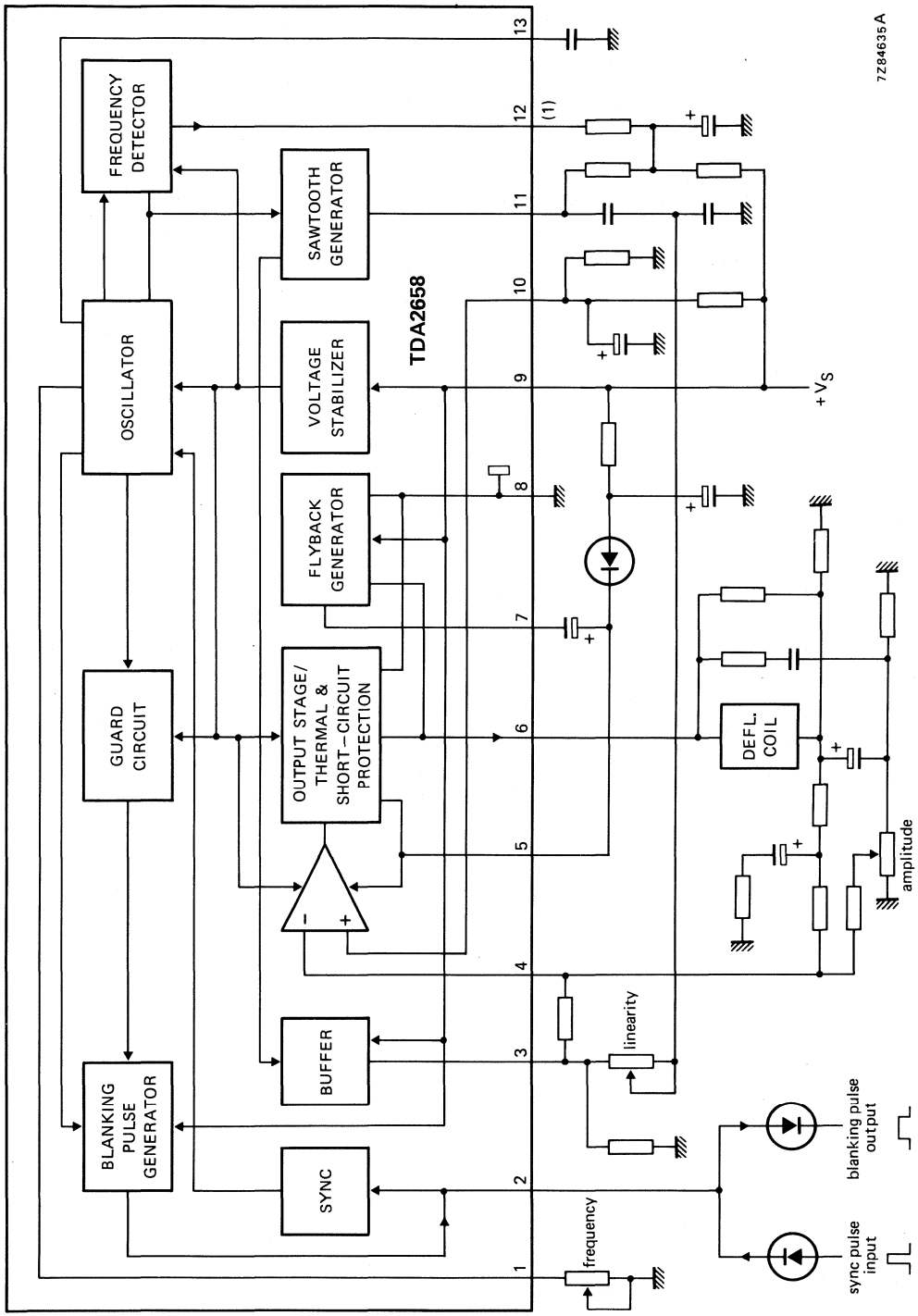
- Oscillator; switch capability for 50 Hz/60 Hz operation.
- Synchronization circuit.
- Blanking pulse generator with guard circuit.
- Sawtooth generator with buffer stage.
- Preamplifier with fed-out inputs.
- Output stage with thermal and short-circuit protection.
- Flyback generator.
- Voltage stabilizer.

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9-8} = V_S$	typ.	26	V
Supply current (pin 5 + pin 9)	$I_5 + I_9 = I_S$	typ.	250	mA
Output current (peak-to-peak value)	$I_{6(p-p)}$	typ.	1,6	A
Picture frequency	f		50 Hz/60	Hz
Sync input pulse (peak-to-peak value)	$V_{2-8(p-p)}$	$\geqslant$	1	V
Thermal resistance from junction to mounting base	$R_{th\ j-mb}$	$\leqslant$	5	K/W

PACKAGE OUTLINE

13-lead SIL; plastic power (SOT141B).



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_{9-8} = V_S$	max.	40 V
Supply voltage output stage (pin 5)	V_{5-8}	max.	58 V
Voltages			
Pin 3	V_{3-11}	max.	7 V
Pin 13	V_{13-8}	max.	7 V
Pins 4 and 10	$V_{4;10-8}$	max.	24 V
Pin 6	V_{6-8}	max.	58 V
	$-V_{6-8}$	max.	0 V
Pins 7 and 11	$V_{7;11-8}$	max.	40 V
Currents			
Pin 1	I_1	max.	0 mA
	$-I_1$	max.	1 mA
Pin 2	$\pm I_2$	max.	10 mA
Pin 3	I_3	max.	0 mA
	$-I_3$	max.	5 mA
Pin 7	I_7	max.	0,9 A
	$-I_7$	max.	1,1 A
Pin 11	I_{11}	max.	50 mA
	$-I_{11}$	max.	1 mA
Pin 12	I_{12}	max.	3 mA
	$-I_{12}$	max.	0 mA

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

Storage temperature range	T_{stg}	−25 to + 150 °C
Operating ambient temperature range	T_{amb}	0 °C to limiting value

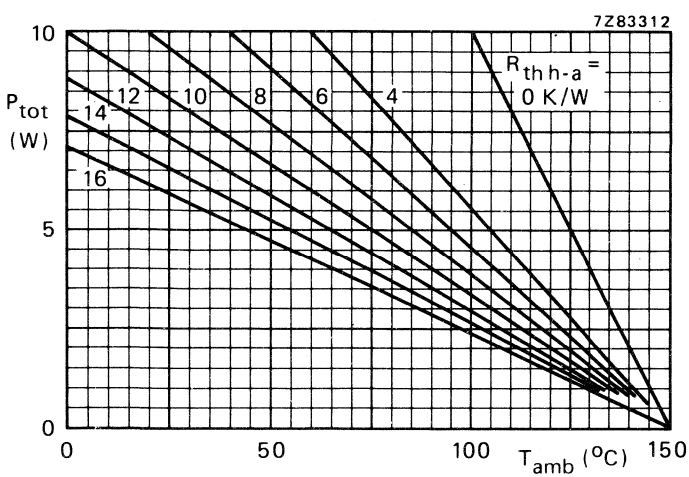


Fig. 2 Total power dissipation. $R_{th\ h-a}$ includes $R_{th\ mb-h}$ which is expected when heat-sink compound is used. $R_{th\ j-mb} \leqslant 5$ K/W.

CHARACTERISTICS

T_{amb} = 25 °C; V_S = 26 V; unless otherwise specified.

Supply voltage/output stage			
Supply voltage	$V_{9-8} = V_S$		9 to 30 V
Output voltage			
at $-I_6$ = 0,75 A	V_{6-8}	⩾	$V_{5-8} - 2{,}2$ V
		typ.	$V_{5-8} - 1{,}9$ V
at I_6 = 0,75 A	V_{6-8}	typ.	1,3 V
		⩽	1,6 V
Flyback generator output voltage at $-I_6$ = 0,75 A	V_{7-8}	typ.	$V_S - 2{,}2$ V
Peak output current	$\pm I_6$	⩽	0,9 A
Flyback generator peak current	$\pm I_7$	⩽	0,9 A
Feedback			
Input quiescent current	$-I_{4;10}$	typ.	0,1 μA
Synchronization			
Sync input pulse	V_{2-8}		1 to 12 V
Tracking range		typ.	28 %
Oscillator/sawtooth generator			
Oscillator frequency control input voltage	V_{1-8}		6 to 9 V
Sawtooth generator output voltage	V_{3-8}		0 to $V_S - 1{,}5$ V
	V_{11-8}		0 to $V_S - 1{,}5$ V
Sawtooth generator output current	$-I_3$		0 to 4 mA
	I_{11}	⩾	−2 μA
		⩽	+30 mA
Oscillator temperature dependency			
T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	typ.	10^{-4} K^{-1}
Oscillator voltage dependency			
V_S = 10 to 30 V	$(\Delta f/f)/\Delta V_S$	typ.	4×10^{-4} V^{-1}
Blanking pulse generator			
Output voltage			
at V_S = 24 V; I_2 = 1 mA	V_{2-8}	typ.	18,5 V
Output current	$-I_2$	⩽	3 mA
Output resistance	R_{2-8}	typ.	410 Ω
Blanking pulse duration at 50 Hz sync	t_b	typ.	1,4 ± 0,07 ms
50 Hz/60 Hz switch capability			
Saturation voltage; LOW voltage level	V_{12-8}	typ.	1 V
Output leakage current	I_{12}	typ.	1 μA

Thermal resistance/junction temperature

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	5 K/W
Junction temperature; switching point thermal protection	T_j	typ.	150 ± 8 °C

PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply (V_S)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

APPLICATION INFORMATION

The function is described against the corresponding pin number

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA (V_S = 26 V).

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

APPLICATION INFORMATION (continued)

10. Reference voltage of preamplifier

    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

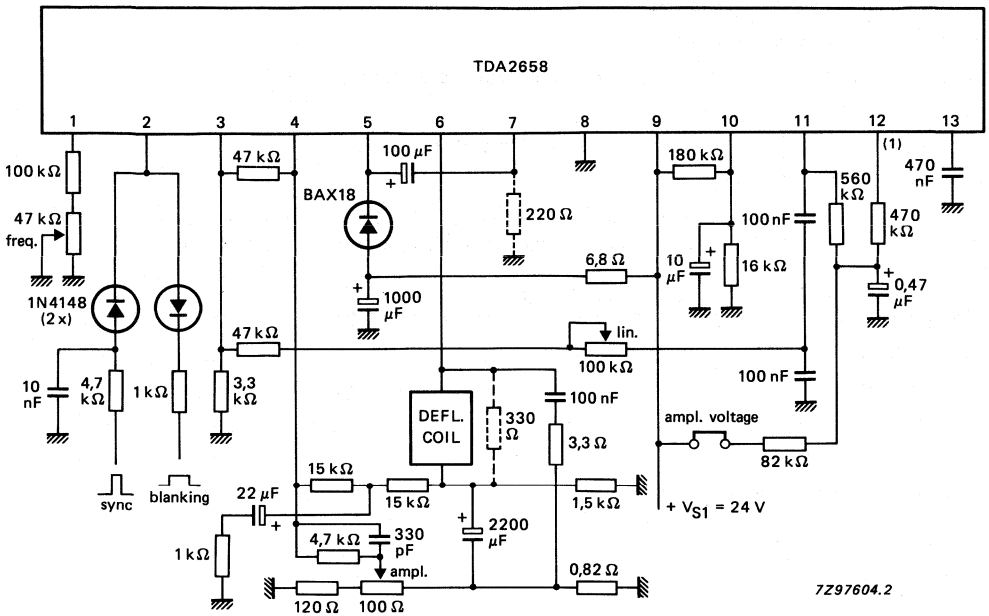
    This sawtooth capacitor has been split to realize linearity control.

12. 50 Hz/60 Hz switching level

    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.

The following application data are measured in Fig. 3

System supply voltages	V_{S1}	typ.	24	V
System supply currents	I_{S1}	typ.	145	mA
Output voltage	V_{6-8}	typ.	14	V
Output voltage (peak value)	V_{6-8}	typ.	44	V
Deflection current (peak-to-peak value)	$I_{6(p-p)}$	typ.	1	A
Flyback time	t_{fl}	typ.	1	ms
Total power dissipation per package	P_{tot}	typ. max.	1,7 2,2	W W
Oscillator frequency unsynchronized	f	typ.	46,5	Hz



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit.

INFRARED RECEIVER

The TDA3047 is for infrared reception with low power consumption.
The difference between the TDA3047 and TDA3048 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8-16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2-15(p-p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	4,5 V

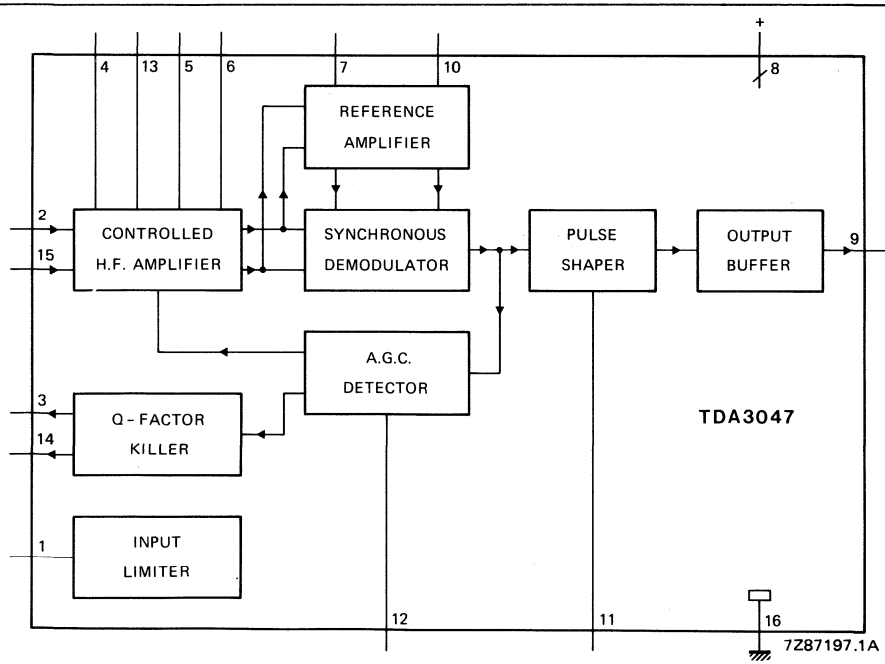


Fig. 1 Block diagram of TDA3047.

PACKAGE OUTLINES

TDA3047P: 16-lead DIL; plastic (SOT38).
TDA3047T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *high.*

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	V_{2-15}	max.	4,5 V
pins 4 and 13	V_{4-13}	max.	4,5 V
pins 5 and 6	V_{5-6}	max.	4,5 V
pins 7 and 10	V_{7-10}	max.	4,5 V
pins 9 and 11	V_{9-11}	max.	4,5 V
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range			see Fig. 2		
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *high*					
at V_{9-16} = 4,5 V	$-I_9$	75	120	–	μA
at V_{9-16} = 3,0 V	$-I_9$	75	130	–	μA
at V_{9-16} = 1,0 V	$-I_9$	75	140	–	μA
Output current; output voltage *low*					
at V_{9-16} = 0,5 V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *high*; $-I_9 = 75$ μA.
2. Voltage pin 9 remains *low*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*)	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*)	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12-16} = 2$ V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at $V_{12-16} = 2$ V	$-I_{14}$	2,5	7,5	20	μA

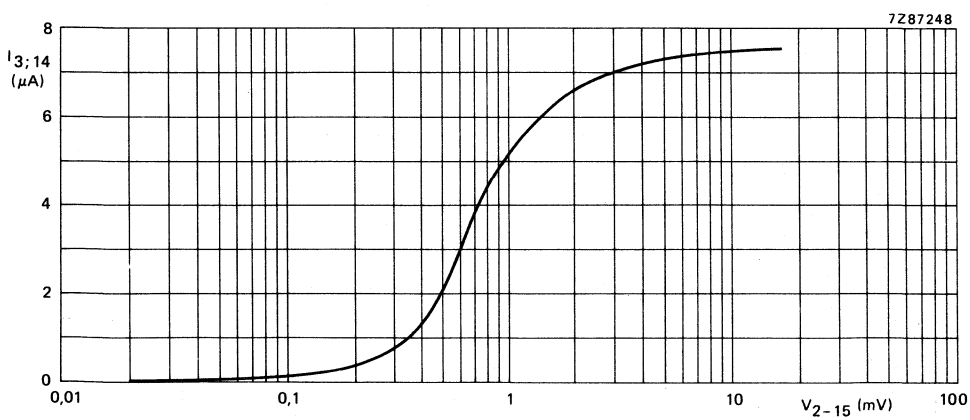
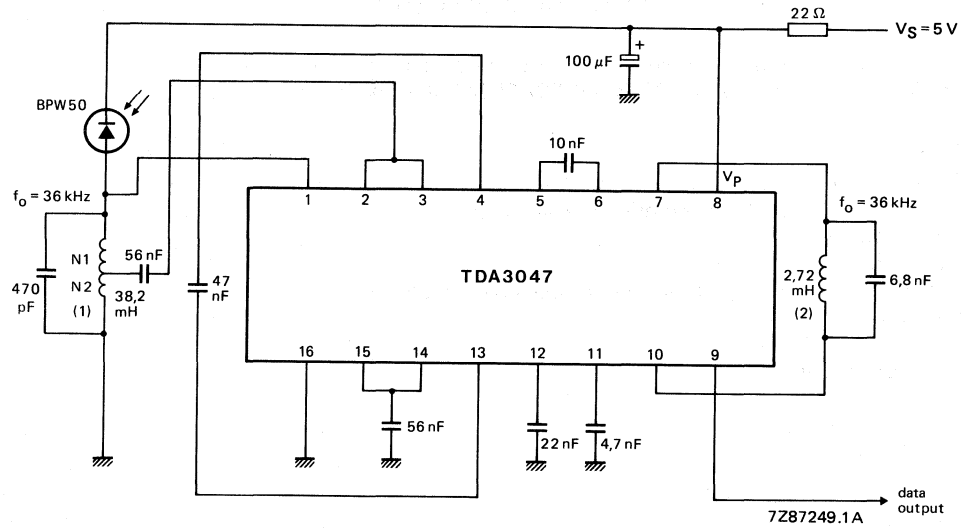


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3047.

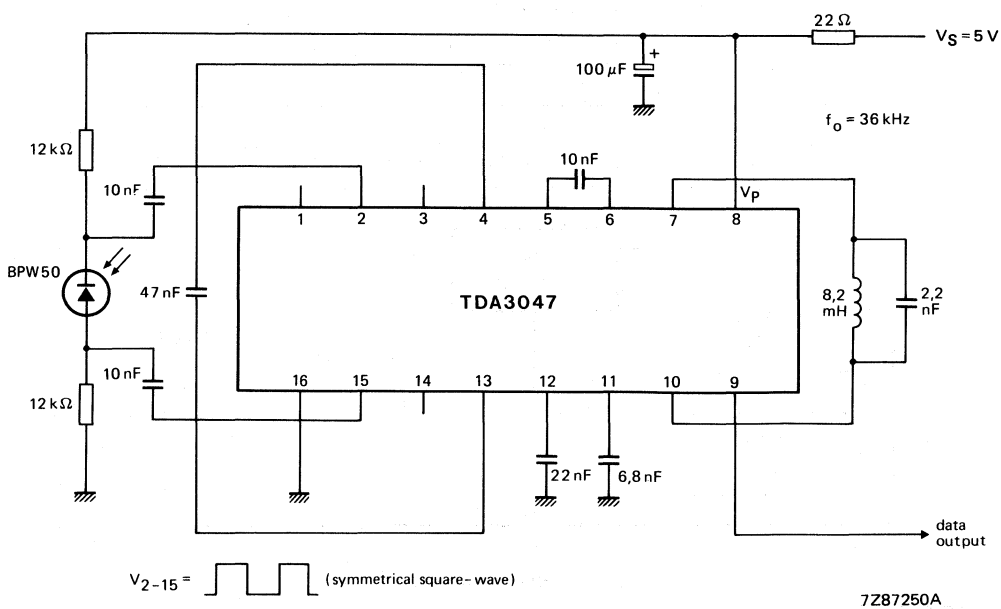


Fig. 4 Wide-band receiver with TDA3047.

For better sensitivity both 12 kΩ resistors may have a higher value.

INFRARED RECEIVER

The TDA3048 is for infrared reception with low power consumption.
The difference between the TDA3048 and TDA3047 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8-16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2-15(p-p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	4,5 V

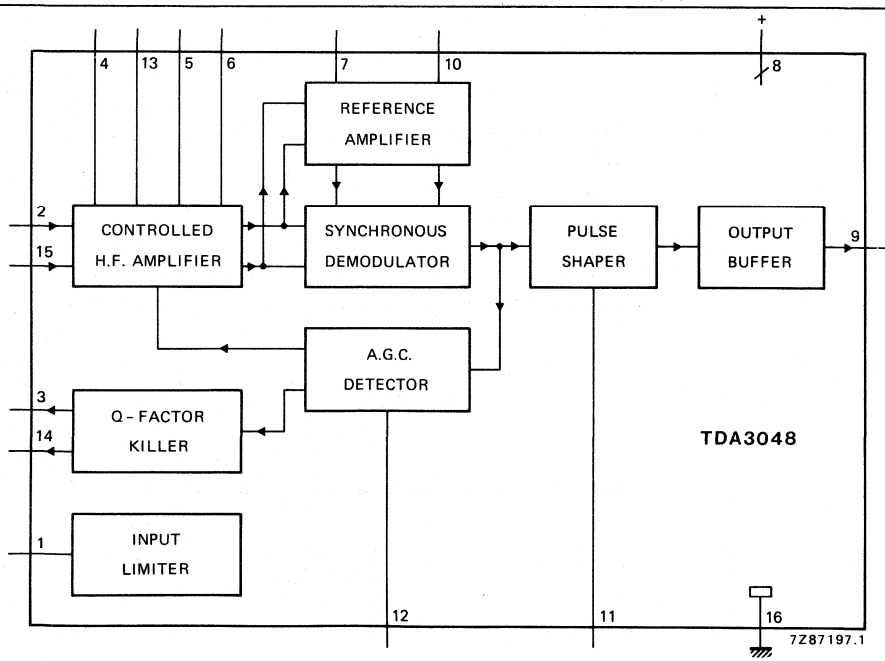


Fig. 1 Block diagram of TDA3048.

PACKAGE OUTLINES

TDA3048P: 16-lead DIL; plastic (SOT38).
TDA3048T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *low.*

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2	V
Output current pulse shaper (pin 11)	I_{11}	max.	10	mA
Voltages between pins*				
pins 2 and 15	V_{2-15}	max.	4,5	V
pins 4 and 13	V_{4-13}	max.	4,5	V
pins 5 and 6	V_{5-6}	max.	4,5	V
pins 7 and 10	V_{7-10}	max.	4,5	V
pins 9 and 11	V_{9-11}	max.	4,5	V
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 125	°C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range		see Fig. 2			
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *low*					
$-V_{9-8} = 4{,}5$ V	I_9	75	120	–	μA
$-V_{9-8} = 3{,}0$ V	I_9	75	130	–	μA
$-V_{9-8} = 1{,}0$ V	I_9	75	140	–	μA
Output current; output voltage *high*					
$-V_{9-8} = 0{,}5$ V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *low*; $I_9 = 75$ μA.
2. Voltage pin 9 remains *high*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12-16} = 2$ V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at $V_{12-16} = 2$ V	$-I_{14}$	2,5	7,5	20	μA

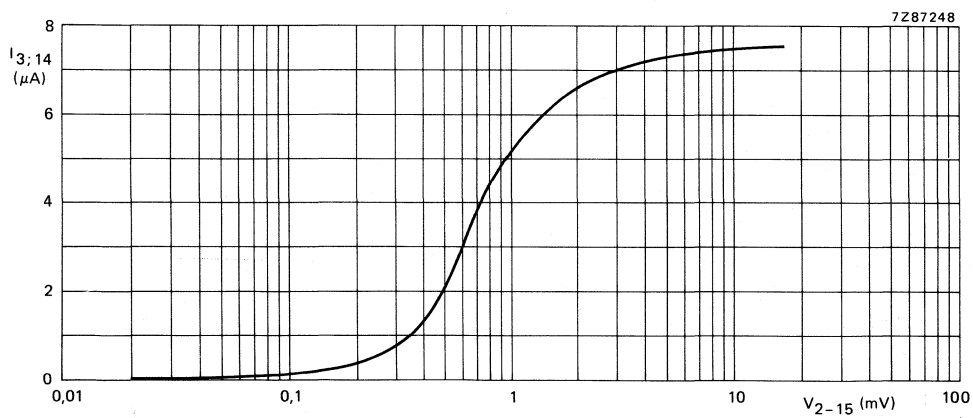
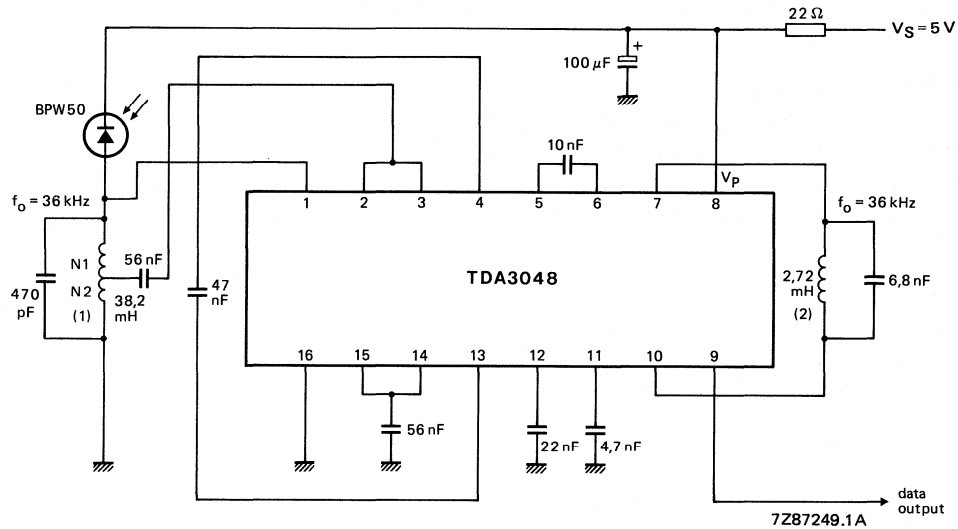


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3048.

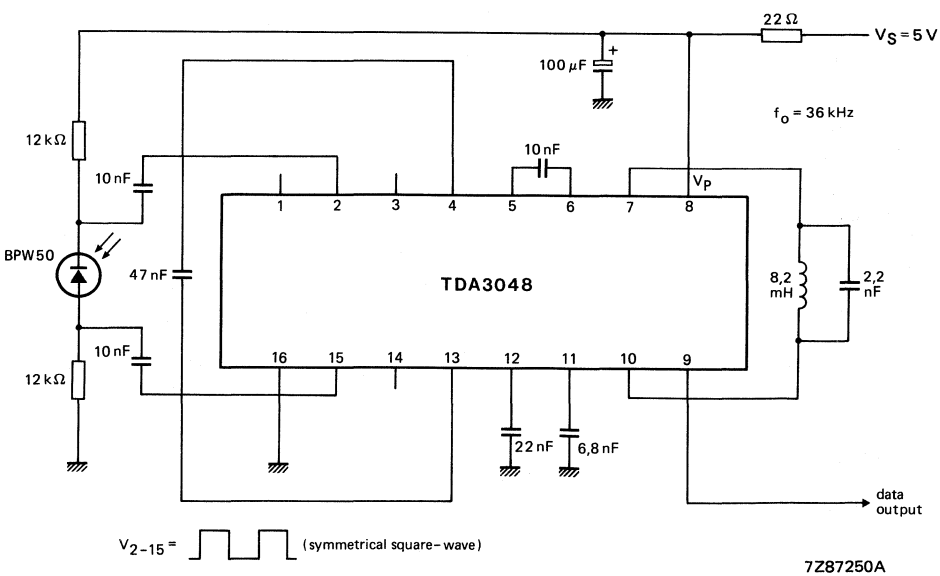


Fig. 4 Wide-band receiver with TDA3048.
For better sensitivity both 12 kΩ resistors may have a higher value.

VIDEO CONTROL COMBINATION CIRCUIT

GENERAL DESCRIPTION

The TDA3504 is an integrated circuit which performs video control functions in a PAL/SECAM decoder for negative colour difference signals −(R-Y) and −(B-Y).

The required input signals are: luminance and colour difference and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages.

Features

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G-Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- Emitter-follower outputs for driving the RGB output stages

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 2)		$V_P = V_{2\text{-}18}$	–	12	–	V
Supply current		$I_P = I_2$	–	95	–	mA
CVBS input signal (peak-to-peak value)		$V_{11\text{-}18(p\text{-}p)}$	–	0.45	–	V
Colour difference input signals (peak-to-peak value)						
−(B-Y)		$V_{15\text{-}18(p\text{-}p)}$	–	1.33	–	V
−(R-Y)		$V_{14\text{-}18(p\text{-}p)}$	–	1.05	–	V
Inserted RGB signals (black-to-white value)		$V_{10,9,8\text{-}18}$	–	1.0	–	V
Three-level sandcastle pulse		$V_{6\text{-}18}$	–	2.5	–	V
			–	4.5	–	V
			–	8.0	–	V
Control voltage ranges						
brightness		$V_{17\text{-}18}$	1.0	–	3.0	V
contrast		$V_{16\text{-}18}$	2.0	–	4.2	V
saturation		$V_{12\text{-}18}$	2.0	–	4.2	V

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

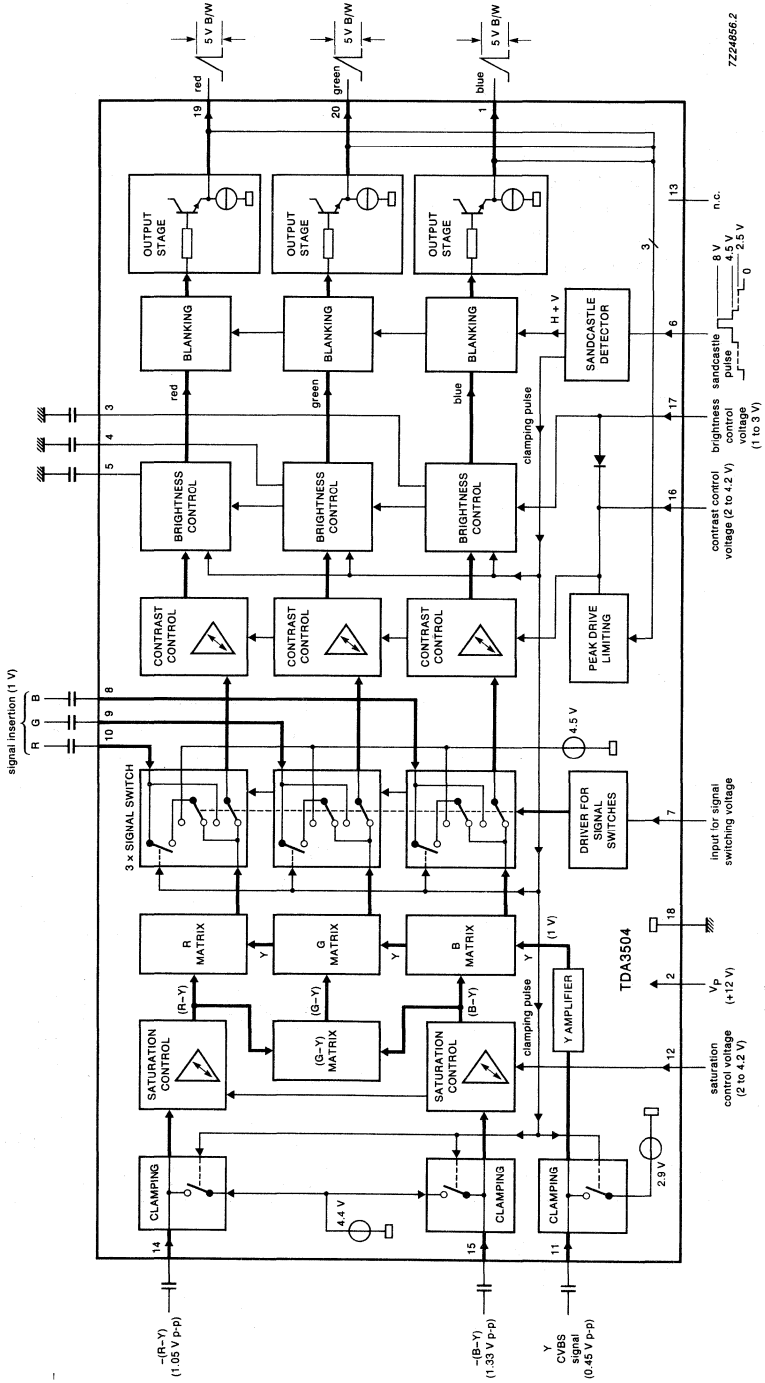


Fig.1 Block diagram.

PINNING

pin	description
1	blue output
2	positive supply voltage (+ 12 V)
3	blue storage for brightness
4	green storage for brightness
5	red storage for brightness
6	sandcastle pulse input
7	fast switch for RGB inputs
8	blue input (external signal)
9	green input (external signal)
10	red input (external signal)
11	luminance input
12	saturation control input
13	not connected
14	colour difference input −(R-Y)
15	colour difference input −(B-Y)
16	contrast control input
17	brightness control input
18	ground (0 V)
19	red output
20	green output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 2)	$V_P = V_{2-18}$	0	13.2	V
Voltage ranges				
at pin 6	V_{6-18}	0	V_P	V
at pin 7	V_{7-18}	−0.5	3.0	V
at pins 12, 16 and 17	$V_{12, 16, 17-18}$	0	$0.5V_P$	V
at pins 1, 3, 4, 5, 8, 9, 10, 11, 14, 15, 19 and 20	no external DC voltage			
Currents				
at pins 1, 19 and 20 (average)	$-I_{1, 19, 20}$	–	3	mA
at pins 1, 19 and 20 (peak)	$-I_{1, 19, 20}$	–	10	mA
at pin 16 (average)	I_{16}	–	10	mA
at pin 17	I_{17}	–	5	mA
Total power dissipation	P_{tot}	–	1.7	W
Storage temperature range	T_{stg}	−25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

CHARACTERISTICS

$V_P = V_{2\text{-}18} = 12.0$ V; $V_{8,\ 9,\ 10\text{-}18(p\text{-}p)} = 1.0$ V; $V_{11\text{-}18(p\text{-}p)} = 0.45$ V; $V_{14\text{-}18(p\text{-}p)} = 1.05$ V; $V_{15\text{-}18(p\text{-}p)} = 1.33$ V; $T_{amb} = 25\ ^{o}C$; measured in Fig.2; nominal settings of brightness, contrast and saturation; all voltages are referred to pin 18; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 2)						
Supply voltage		$V_P = V_2$	10.8	12.0	13.2	V
Supply current		$I_P = I_2$	–	95	125*	mA
Colour difference inputs (pins 14 and 15)						
–(R-Y) input signal (pin 14) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{14(p\text{-}p)}$	–	1.05	1.48	V
–(B-Y) input signal (pin 15) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{15(p\text{-}p)}$	–	1.33	1.88	V
Input current during scanning		$I_{14,\ 15}$	–	–	0.2	μA
Input resistance		$R_{14,\ 15\text{-}18}$	1.0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{14,\ 15}$	3.8	4.4	4.8	V
Saturation control (pin 12)						
Control voltage for maximum saturation	note 1	V_{12}	4.0	4.2	4.4	V
Control voltage for nominal saturation	note 1; 6 dB below max.	V_{12}	2.9	3.1	3.3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{12}	1.9	2.1	2.3	V
Minimum saturation	$V_{12} = 1.8$ V	d	46	50	–	dB
Input current		I_{12}	–	–	20	μA
(G-Y) matrix						
Matrixed according to the equation $V_{(G\text{-}Y)} = -0.51\ V_{(R\text{-}Y)} - 0.19\ V_{(B\text{-}Y)}$						
Luminance input (pin 11)						
CVBS input signal (peak-to-peak value)		$V_{11(p\text{-}p)}$	–	450	630	mV
Input resistance		$R_{11\text{-}18}$	1	–	–	MΩ

* < 110 mA after warm-up.

parameter	conditions	symbol	min.	typ.	max.	unit
Input current during scanning		I_{11}	–	–	0.4	μA
Linearity	nominal settings	m	0.85	–	–	
Internal DC voltage due to clamping	note 1	V_{11}	2.5	2.9	3.3	V
RGB channels						
Signal switching input (pin 7)						
Normal state; no insertion		V_7	0	–	0.4	V
Level for insertion-on		V_7	0.9	–	3.0	V
Input capacitance		$C_{7\text{-}18}$	–	–	10	pF
Input current	V_7 = 0 to 3 V	I_7	−100	–	+ 450	μA
Signal insertion R: pin 10 G: pin 9 B: pin 8						
External RGB input signals (black-to-white value)		$V_{8, 9, 10}$	–	1.0	1.4	V
Input current during scanning		$I_{8, 9, 10}$	–	–	0.4	μA
Internal DC voltage due to clamping	notes 1 and 2	$V_{8, 9, 10}$	4.0	4.5	5.0	V
Contrast control (pin 16)	note 1					
Control voltage for maximum contrast		V_{16}	4.0	4.2	4.4	V
Control voltage for nominal contrast	3 dB below max.	V_{16}	3.4	3.6	3.8	V
Control voltage for −10 dB below max.		V_{16}	2.6	2.8	3.0	V
Minimum contrast referred to max.	V_{16} = 2 V	d	18	21	29	dB
Difference between RGB channels	contrast −10 dB below max.		–	–	0.6	dB

CHARACTERISTICS (continued)

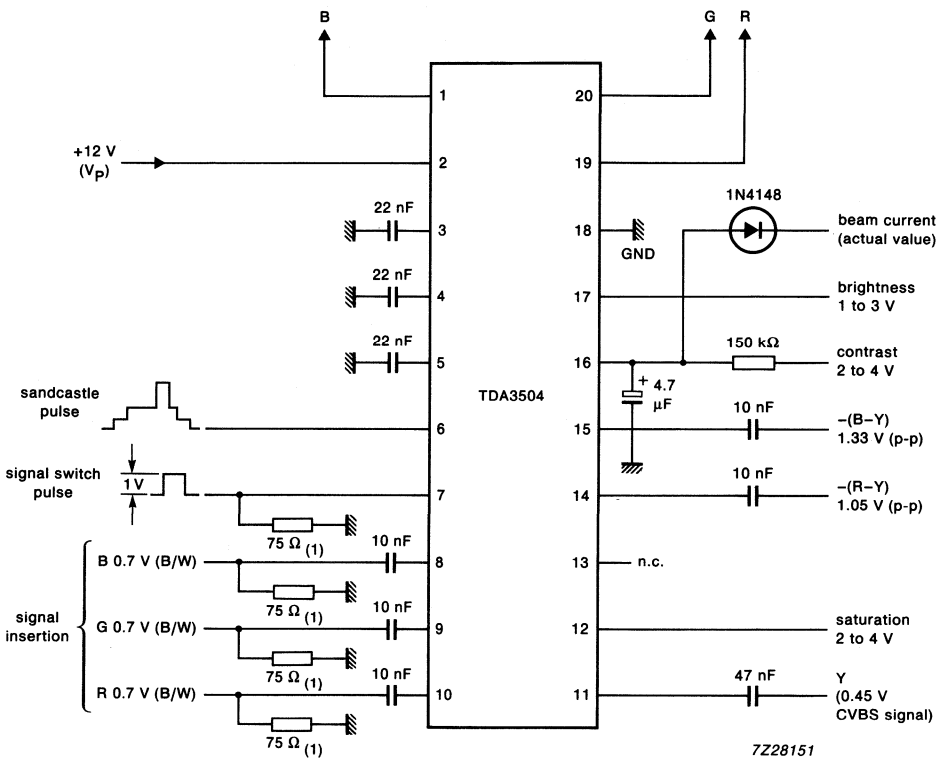
parameter	conditions	symbol	min.	typ.	max.	unit
Peak drive limiting						
Threshold voltage	note 1	V_{th}	8.7	9.0	9.3	V
Input current at contrast control input	$V_{1, 19, 20} = \geqslant V_{th}$	I_{16}	10	20	30	mA
Brightness control (pin 17)	note 1					
Control voltage range		V_{17}	1	–	3	V
Control voltage for nominal brightness		V_{17}	–	2.0	–	V
Input current		$-I_{17}$	–	–	10	μA
Shift of black level in the control range related to the luminance signal (black/white)	$\Delta V_{17} = 1$ V		–	± 40	–	%
Tracking			95	–	–	%
RGB outputs (emitter follower) (pins 19, 20 and 1)						
Output voltage; black-to-white positive		$V_{19, 20, 1}$	4.0	5.0	6.5	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{19, 20, 1}$	–	–	10	mV
Internal current source		$I_{19, 20, 1}$	2.0	3.0	–	mA
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 11)		$G_{19, 20, 1\text{-}11}$	22	24	26	dB
Frequency response of luminance path	0 to 5 MHz	$d_{19, 20, 1\text{-}11}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 14 and 15)		$G_{1\text{-}15}$ $G_{19\text{-}14}$	11	14	17	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency response of colour difference paths	0 to 2 MHz	$d_{1\text{-}15}$ $d_{19\text{-}14}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{19\text{-}10}$ $G_{20\text{-}9}$ $G_{1\text{-}8}$	12	14	16	dB
Frequency response of inserted signal paths	0 to 10 MHz	$d_{19\text{-}10}$ $d_{20\text{-}9}$ $d_{1\text{-}8}$	–	–	3	dB
Difference in transit times between R, G and B channels		$\Delta t_{19,\,20,\,1}$	–	0	15	ns
Delay time between signal switching and signal insertion		t_d	–25	–	+ 25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{19,\,20,\,1}$	–	–	10	%
Sandcastle pulse detector (pin 6)	note 3					
The following amplitudes are required for separating the various pulses:						
horizontal and vertical blanking pulses	note 4	V_6	2.1	2.5	2.9	V
horizontal pulses		V_6	4.1	4.5	5.0	V
clamping pulses	note 5	V_6	7.6	8.0	12.0	V
no keying		V_6	–	–	1.0	V
Input current		$-I_6$	–	–	110	μA
Delay of leading edge of clamping pulse		t_d	–	0.5	–	μs

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{7\text{-}18} < 0.4$ V during clamping time – the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
   When $V_{7\text{-}18} > 0.9$ V during clamping time – the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) and the given levels separate the various pulses.
4. Blanked to ultra-black (–25%).
5. Pulse duration $\geqslant 3.5$ μs.

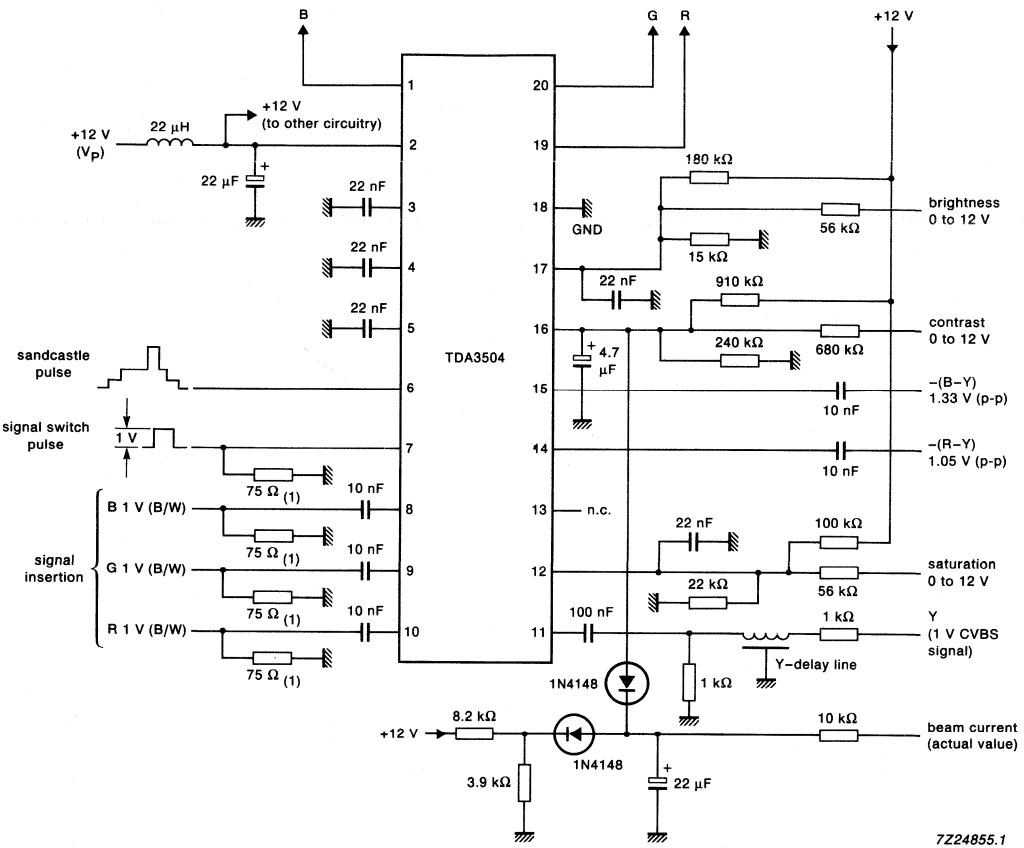
APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.

Fig.2(a) Basic application circuit diagram.

DEVELOPMENT DATA



(1) When applied via a 75 Ω line.

Fig.2(b) Typical application circuit diagram.

VIDEO CONTROL COMBINATION CIRCUIT

WITH AUTOMATIC CUT-OFF CONTROL

GENERAL DESCRIPTION

The TDA3505 and TDA3506 are monolithic integrated circuits which perform video control functions in a PAL/SECAM decoder. The TDA3505 is for negative colour difference signals −(R-Y), −(B-Y) and the TDA3506 is for positive colour difference signals +(R-Y), +(B-Y).

The required input signals are: luminance and colour difference (negative or positive) and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. The circuits provide automatic cut-off control of the picture tube.

Features

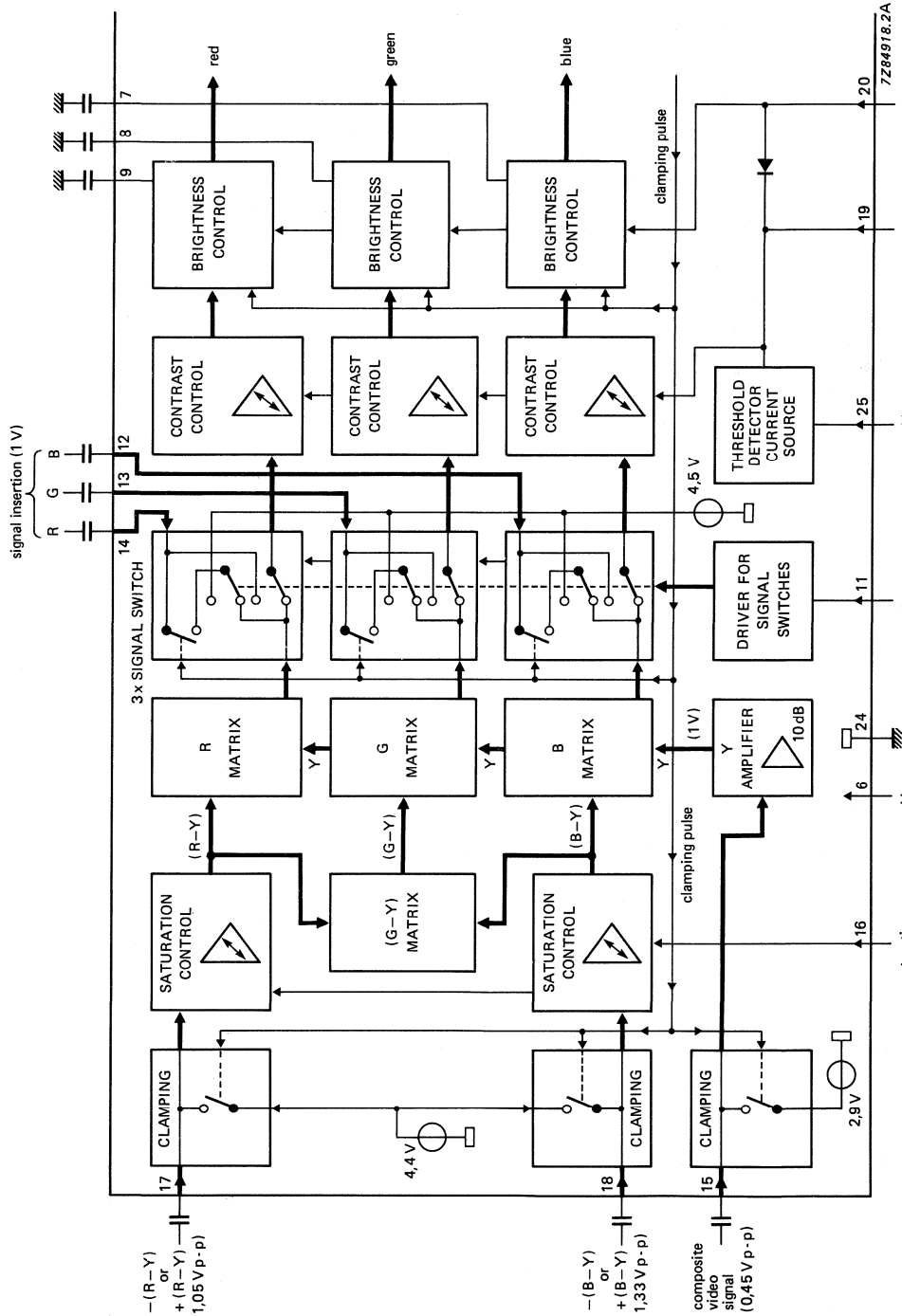
- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G-Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	95	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0,45	–	V
Colour difference input signals (peak-to-peak value)						
−(B-Y) or +(B-Y) respectively		$V_{18-24(p-p)}$	–	1,33	–	V
−(R-Y) or +(R-Y) respectively		$V_{17-24(p-p)}$	–	1,05	–	V
Inserted RGB signals (black-to-white value)		$V_{12, 13, 14-24}$	–	1,0	–	V
Three-level sandcastle pulse		V_{10-24}	–	2,5	–	V
			–	4,5	–	V
			–	8,0	–	V
Control voltage ranges						
brightness		V_{20-24}	1,0	–	3,0	V
contrast		V_{19-24}	2,0	–	4,3	V
saturation		V_{16-24}	2,0	–	4,3	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).



Note Colour difference inputs are negative for TDA3505 or positive for TDA3506.

Fig. 1a Part of block diagram; continued in Fig. 1b.

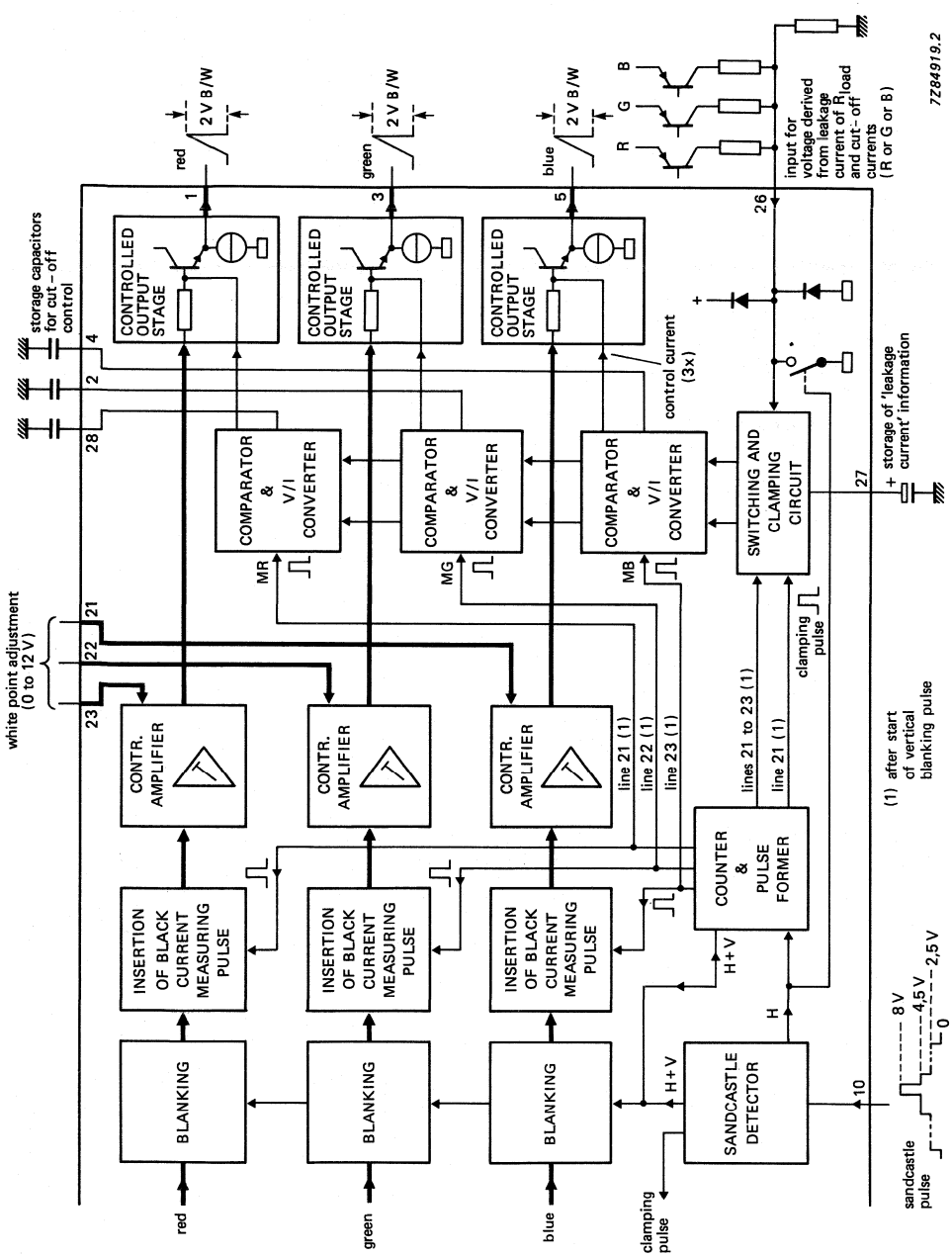


Fig. 1b Part of block diagram; continued from Fig. 1a.

PINNING

pin	description
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	colour difference input –(R-Y) or +(R-Y) respectively
18	colour difference input –(B-Y) or +(B-Y) respectively
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6)	$V_P = V_{6-24}$	–	13,2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	–0,5	3,0	V
at pins 16, 19, 20	$V_{16, 19, 20-24}$	0	$0{,}5V_P$	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1, 3, 5}$	–	3	mA
at pin 19	I_{19}	–	10	mA
at pin 20	I_{20}	–	5	mA
at pin 25	$-I_{25}$	–	5	mA
Total power dissipation	P_{tot}	–	1,7	W
Storage temperature range	T_{stg}	–25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

CHARACTERISTICS

$V_P = V_{6-24} = 12{,}0$ V; $V_{12, 13, 14(p-p)} = 1{,}0$ V; $V_{15-24(p-p)} = 0{,}45$ V; $V_{17-24(p-p)} = 1{,}05$ V; $V_{18-24(p-p)} = 1{,}33$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 2; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10,8	12,0	13,2	V
Supply current		I_P	–	95	125*	mA
Colour difference inputs (pins 17, 18)						
(R-Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	–	1,05	1,48	V
(B-Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	–	1,33	1,88	V
Input current during scanning		$I_{17, 18}$	–	–	1,0	μA
Input resistance		$R_{17, 18-24}$	1,0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{17, 18}$	3,8	4,4	4,8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 1	V_{16}	4,0	4,2	4,4	V
Control voltage for nominal saturation	6 dB below max. note 1	V_{16}	2,9	3,1	3,3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{16}	1,9	2,1	2,3	V
Minimum saturation	$V_{16} = 1{,}8$ V	d	46	50	–	dB
Input current		I_{16}	–	–	20	μA
(G-Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$						
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	–	450	630	mV
Input resistance		R_{15-24}	100	–	–	kΩ

* < 110 mA after warm-up.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance input (continued)						
Input capacitance		$C_{15\text{-}24}$	–	–	5	pF
Input current during scanning		I_{15}	–	–	1	μA
Linearity	nominal settings	m	0,85	–	–	
Internal DC voltage due to clamping	note 1	V_{15}	2,5	2,9	3,3	V
RGB channels						
Signal switching input (pin 11)						
Normal state; no insertion		V_{11}	0	–	0,4	V
Level for insertion-on		V_{11}	0,9	–	3,0	V
Input capacitance		$C_{11\text{-}24}$	–	–	10	pF
Input current	V_{11} = 0 to 3 V	I_{11}	−100	–	+450	μA
Signal insertion (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12, 13, 14}$	–	1,0	1,4	V
Input current during scanning		$I_{12, 13, 14}$	–	–	1,0	μA
Internal DC voltage due to clamping	notes 1, 2	$V_{12, 13, 14}$	4,0	4,5	5,0	V
Contrast control (pin 19)	note 1					
Control voltage for maximum contrast		V_{19}	4,0	4,2	4,4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3,4	3,6	3,8	V
Control voltage for −10 dB below max.		V_{19}	2,6	2,8	3,0	V
Minimum contrast referred to max.	V_{19} = 2 V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	–	–	2	μA
Difference between RGB channels	contrast −10 dB below max.		–	–	0,6	dB
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 1	V_{25}	5,3	5,5	5,7	V
Input resistance		$R_{25\text{-}24}$	–	10	–	kΩ
Input current at contrast control input	V_{25} = 4,5 V	I_{19}	10	20	34	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control (pin 20)	note 1					
Control voltage range		V_{20}	1	–	3	V
Input current		$-I_{20}$	–	–	10	μA
Change of black level in the control range related to the luminance signal (black/white)	ΔV_{20} = 1 V		–	±50	–	%
Tracking			95	–	–	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			–	–25	–	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 1					
AC voltage gain	note 3					
$V_{21, 22, 23}$ = 5,5 V		G_v	–	100	–	%
$V_{21, 22, 23}$ = 0 V		G_v	–35	–40	–	%
$V_{21, 22, 23}$ = 12 V		G_v	+35	+40	–	%
Input resistance		$R_{21,22,23-24}$	–	20	–	kΩ
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1, 3, 5}$	1,5	2,0	2,5	V
Black level without automatic cut-off control	note 1; $V_{28,2,4}$ = 10 V	$V_{1, 3, 5}$	6,1	6,9	7,7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1, 3, 5}$	–	–	10	mV
Cut-off control range	note 1	$V_{1, 3, 5}$	4,0	4,6	–	V
Internal current source		$I_{1, 3, 5}$	2,0	3,0	–	mA

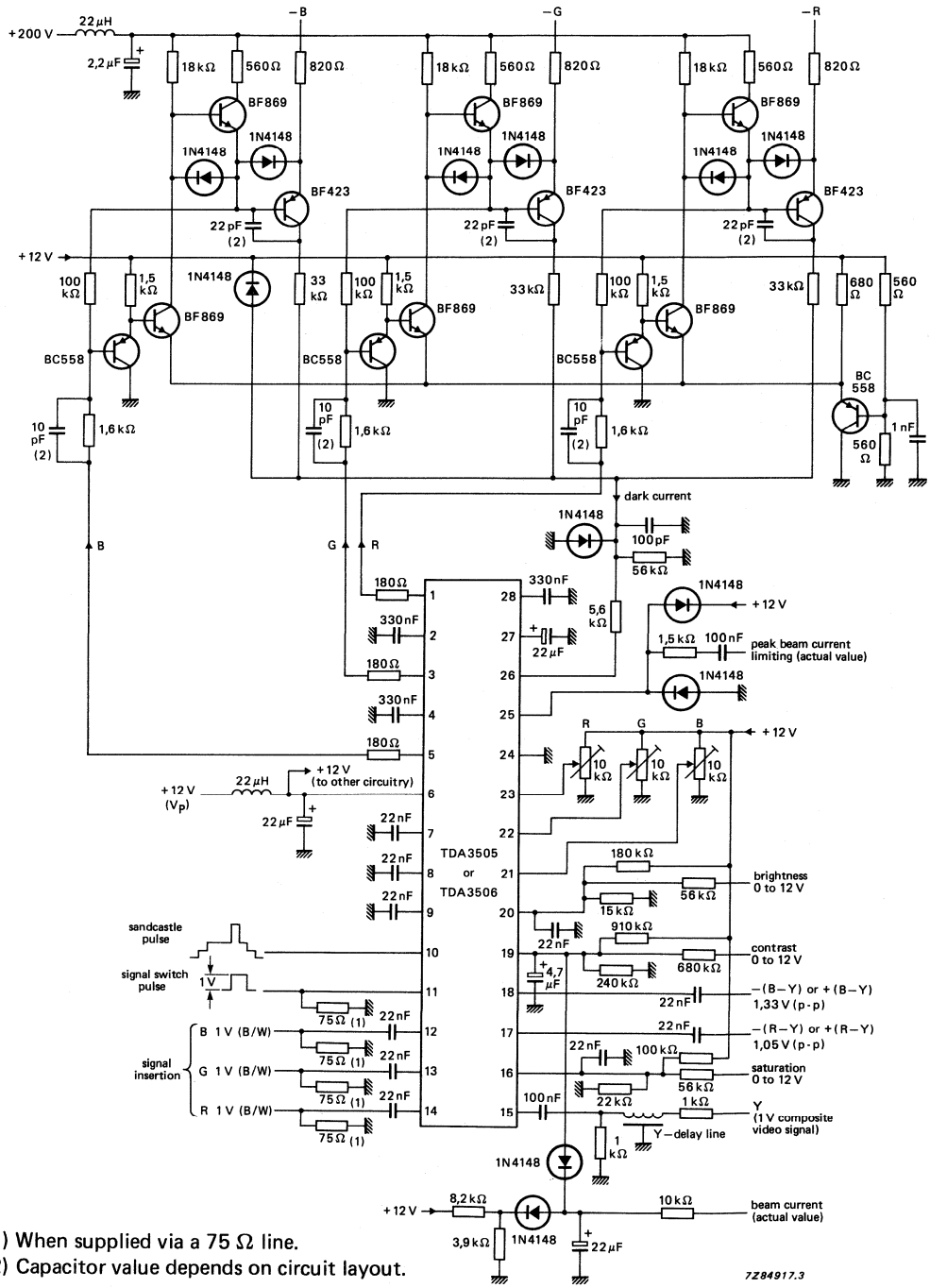
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic cut-off control (pin 26)	notes 1, 4					
Input voltage range		V_{26}	0	–	6,5	V
Voltage difference between cut-off current measurement (note 5) and leakage current measurement (note 6)		V_{26}	0,5	0,64	0,72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5\text{-}15}$	14	16	18	dB
Frequency response of luminance path	0 to 5 MHz	$d_{1,3,5\text{-}15}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		$G_{5\text{-}18}$ $G_{1\text{-}17}$	3	6	9	dB
Frequency response of colour difference paths	0 to 2 MHz	$d_{5\text{-}18}$ $d_{1\text{-}17}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{1\text{-}14}$ $G_{3\text{-}13}$ $G_{5\text{-}12}$	4	6	8	dB
Frequency response of inserted signal paths	0 to 10 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	–	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	–	40	–	ns
Difference in transit times between R, G and B channels		$\Delta t_{1,3,5}$	–	0	15	ns
Delay time between signal switching and signal insertion		t_d	–25	–	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	–	–	10	%

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (pin 10)	note 7					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 8	V_{10}	1,0	1,5	2,0	V
required pulses (H+V)		V_{10}	2,1	2,5	2,9	V
horizontal pulses		V_{10}	3,0	3,5	4,0	V
required pulses (H)		V_{10}	4,1	4,5	5,0	V
clamping pulses	note 9	V_{10}	6,5	7,0	7,5	V
required pulses		V_{10}	7,6	—	12,0	V
no keying		V_{10}	—	—	1,0	V
Input current		$-I_{10}$	—	—	110	μA

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{11\text{-}24} < 0{,}4$ V during clamping time - the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
   When $V_{11\text{-}24} > 0{,}9$ V during clamping time - the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5,5 V is supplied.
4. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:
   line 20: measurement of leakage current (R + G + B)
   line 21: measurement of red cut-off current
   line 22: measurement of green cut-off current
   line 23: measurement of blue cut-off current
5. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
6. All three channels blanked to ultra-black.
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
   The internal blanking continues until the end of the last measured line.
   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.
7. The sandcastle pulse is compared with three internal thresholds (proportional to Vp) and the given levels separate the various pulses.
8. Blanked to ultra-black (−25%).
9. Pulse duration $\geqslant 3{,}5$ μs.



(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using TDA3505 or TDA3506; colour difference inputs are negative for TDA3505 or positive for TDA3506.

VIDEO CONTROL COMBINATION CIRCUIT

WITH AUTOMATIC CUT-OFF CONTROL

GENERAL DESCRIPTION

The TDA3507 is a monolithic integrated circuit which performs video control functions in a PAL/SECAM decoder.

The required input signals are: luminance and negative colour difference −(R−Y) and −(B−Y), and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

The TDA3507 is the same as the TDA3505 but with RGB channel bandwidths of (typical) 16 MHz and an automatic cut-off cycle that ends in line 15.

Features

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G−Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	100	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0,45	–	V
Colour difference input signals (peak-to-peak value)						
–(B–Y)		$V_{18-24(p-p)}$	–	1,33	–	V
–(R–Y)		$V_{17-24(p-p)}$	–	1,05	–	V
Inserted RGB signals (black-to-white value)		$V_{12,13,14-24}$	–	1,0	–	V
Three-level sandcastle pulse		V_{10-24}	–	2,5	–	V
			–	4,5	–	V
			–	8,0	–	V
Control voltage ranges						
brightness		V_{20-24}	1,0	–	3,0	V
contrast		V_{19-24}	2,0	–	4,3	V
saturation		V_{16-24}	2,0	–	4,3	V

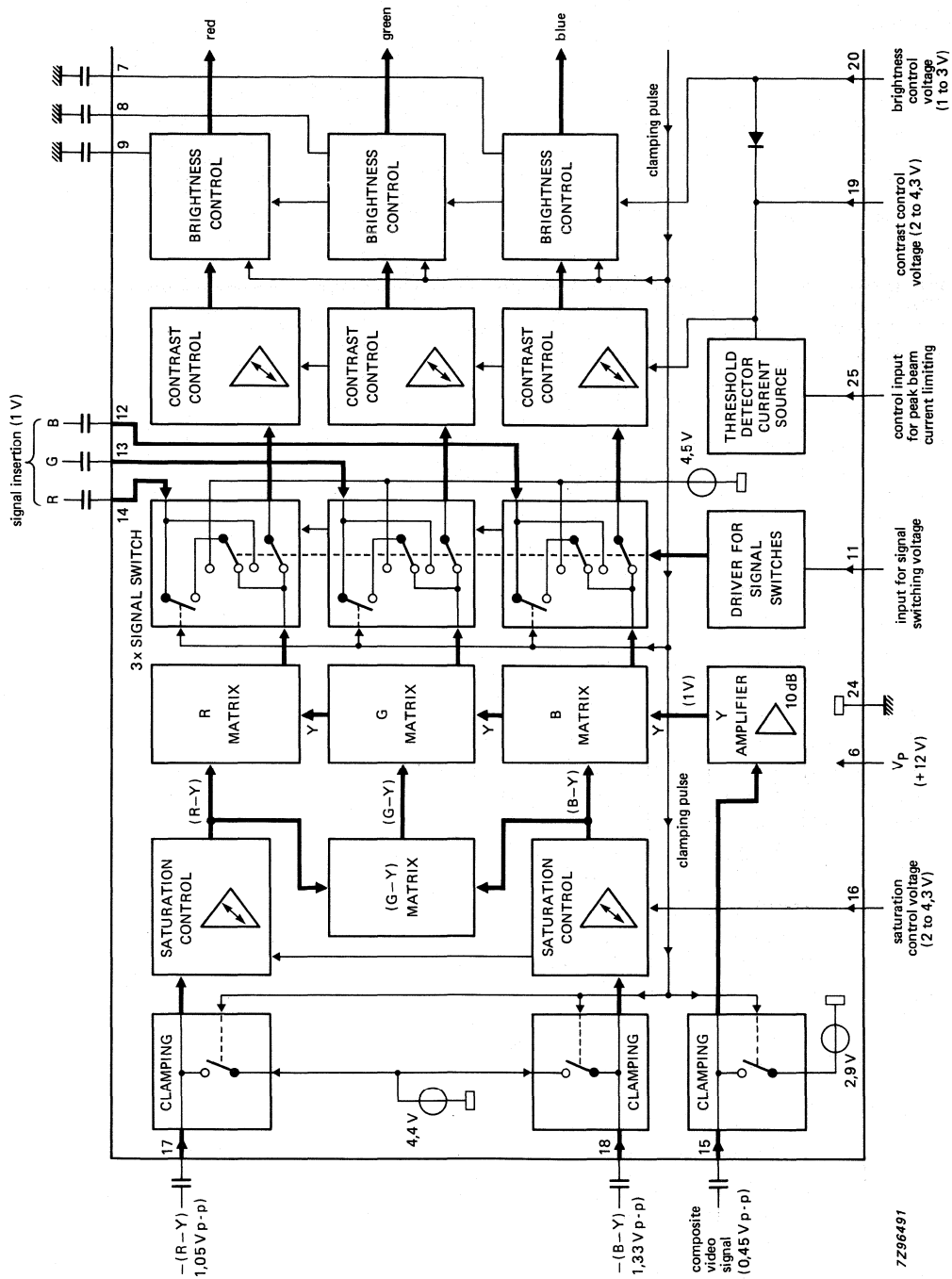


Fig. 1a Part of block diagram, continued in Fig. 1b.

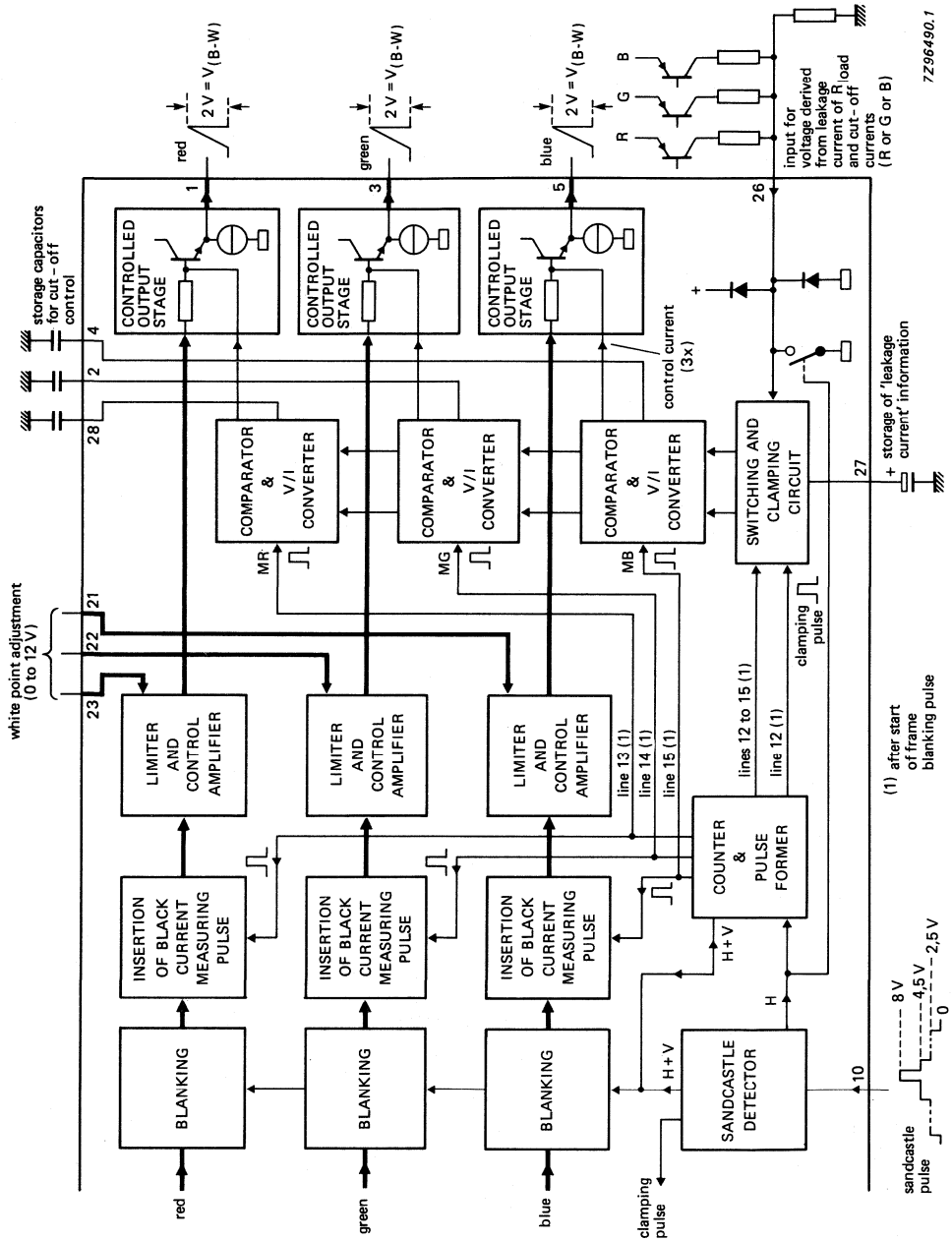


Fig. 1b Part of block diagram, continued from Fig. 1a.

PINNING

pin	description
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	−(R−Y) colour difference input
18	−(B−Y) colour difference input
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6)	$V_P = V_{6-24}$	−	13,2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	−0,5	3,0	V
at pins 16, 19, 20	$V_{16,19,20-24}$	0	$0{,}5V_P$	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1,3,5}$	−	3	mA
at pin 19	I_{19}	−	10	mA
at pin 20	I_{20}	−	5	mA
at pin 25	$-I_{25}$	−	5	mA
Total power dissipation	P_{tot}	−	1,7	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

CHARACTERISTICS

$V_P = V_{6-24} = 12{,}0$ V; $V_{12,13,14(p-p)} = 1{,}0$ V; $V_{15-24(p-p)} = 0{,}45$ V; $V_{17-24(p-p)} = 1{,}05$ V; $V_{18-24(p-p)} = 1{,}33$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 2; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10,8	12,0	13,2	V
Supply current		I_P	–	100	130*	mA
Colour difference inputs (pins 17, 18)						
–(R–Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	–	1,05	1,48	V
–(B–Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	–	1,33	1,88	V
Input current during scanning		$I_{17,18}$	–	–	1,0	μA
Input resistance		$R_{17,18-24}$	1,0	–	–	MΩ
Internal DC voltage due to clamping	note 1	$V_{17,18}$	3,8	4,4	4,8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 1	V_{16}	4,0	4,2	4,4	V
Control voltage for nominal saturation	6 dB below max. note 1	V_{16}	2,9	3,1	3,3	V
Control voltage for –26 dB saturation referred to maximum	note 1	V_{16}	1,9	2,1	2,3	V
Minimum saturation	$V_{16} = 1{,}8$ V	d	46	50	–	dB
Input current		I_{16}	–	–	20	μA
(G–Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$						
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	–	450	630	mV
Input resistance		R_{15-24}	100	–	–	kΩ
Input capacitance		C_{15-24}	–	–	5	pF

* $<$ 115 mA after warm-up

parameter	conditions	symbol	min.	typ.	max.	unit
Luminance input (continued)						
Input current during scanning		I_{15}	–	–	1	μA
Linearity	nominal settings	m	0,85	–	–	
Internal DC voltage due to clamping	note 1	V_{15}	2,5	2,9	3,3	V
RGB channels						
Signal switching input (pin 11)						
Normal state; no insertion		V_{11}	0	–	0,4	V
Level for insertion-on		V_{11}	0,9	–	3,0	V
Input capacitance		C_{11-24}	–	–	10	pF
Input current	V_{11} = 0 to 3 V	I_{11}	−100	–	+450	μA
Signal insertion (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12,13,14}$	–	1,0	1,4	V
Input current during scanning		$I_{12,13,14}$	–	–	1,0	μA
Internal DC voltage due to clamping	notes 1, 2	$V_{12,13,14}$	4,0	4,5	5,0	V
Contrast control (pin 19)	note 1					
Control voltage for maximum contrast		V_{19}	4,0	4,2	4,4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3,4	3,6	3,8	V
Control voltage for −10 dB below max.		V_{19}	2,6	2,8	3,0	V
Minimum contrast referred to max.	V_{19} = 2 V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	–	–	2	μA
Difference between RGB channels	contrast −10 dB below max.		–	–	0,6	dB
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 1	V_{25}	5,3	5,5	5,7	V
Input resistance		R_{25-24}	–	10	–	kΩ
Input current at contrast control input	V_{25} = 4,5 V	I_{19}	10	20	34	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Brightness control (pin 20)	note 1					
Control voltage range		V_{20}	1	–	3	V
Input current		$-I_{20}$	–	–	10	μA
Change of black level in the control range related to the luminance signal (black/white)	ΔV_{20} = 1 V		–	±50	–	%
Tracking			95	–	–	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			–	–25	–	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 1					
AC voltage gain	note 3					
$V_{21,22,23}$ = 5,5 V		G_V	–	100	–	%
$V_{21,22,23}$ = 0 V		G_V	–35	–40	–	%
$V_{21,22,23}$ = 12 V		G_V	+35	+40	–	%
Input resistance		$R_{21,22,23\text{-}24}$	–	20	–	kΩ
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1,3,5}$	1,5	2,0	2,5	V
Black level without automatic cut-off control	note 1; $V_{28,2,4}$ = 10 V	$V_{1,3,5}$	6,1	6,9	7,7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1,3,5}$	–	–	10	mV
Cut-off control range	note 1	$V_{1,3,5}$	4,0	4,6	–	V
Internal current source		$I_{1,3,5}$	2,0	3,0	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic cut-off control (pin 26)	notes 1,4					
Input voltage range		V_{26}	0	–	6,5	V
Voltage difference between cut-off current measurement (note 5) and leakage current measurement (note 6)		V_{26}	0,5	0,64	0,72	V
Input pin 26 switches to ground during horizontal flyback						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5\text{-}15}$	14	16	18	dB
Frequency response of luminance path	0 to 5 MHz	$d_{1,3,5\text{-}15}$	–	–	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		$G_{5\text{-}18}$ $G_{1\text{-}17}$	3	6	9	dB
Frequency response of colour difference paths	0 to 2 MHz	$d_{5\text{-}18}$ $d_{1\text{-}17}$	–	–	3	dB
Voltage gain with respect to inserted signals		$G_{1\text{-}14}$ $G_{3\text{-}13}$ $G_{5\text{-}12}$	4	6	8	dB
Frequency response of inserted signal paths	0 to 16 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	3	–	dB
Frequency response of inserted signal paths	0 to 13 MHz	$d_{1\text{-}14}$ $d_{3\text{-}13}$ $d_{5\text{-}12}$	–	–	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	–	40	–	ns
Difference in transit times between R, G and B channels		$\Delta t_{1,3,5}$	–	0	15	ns

CHARACTERISTICS (continued)

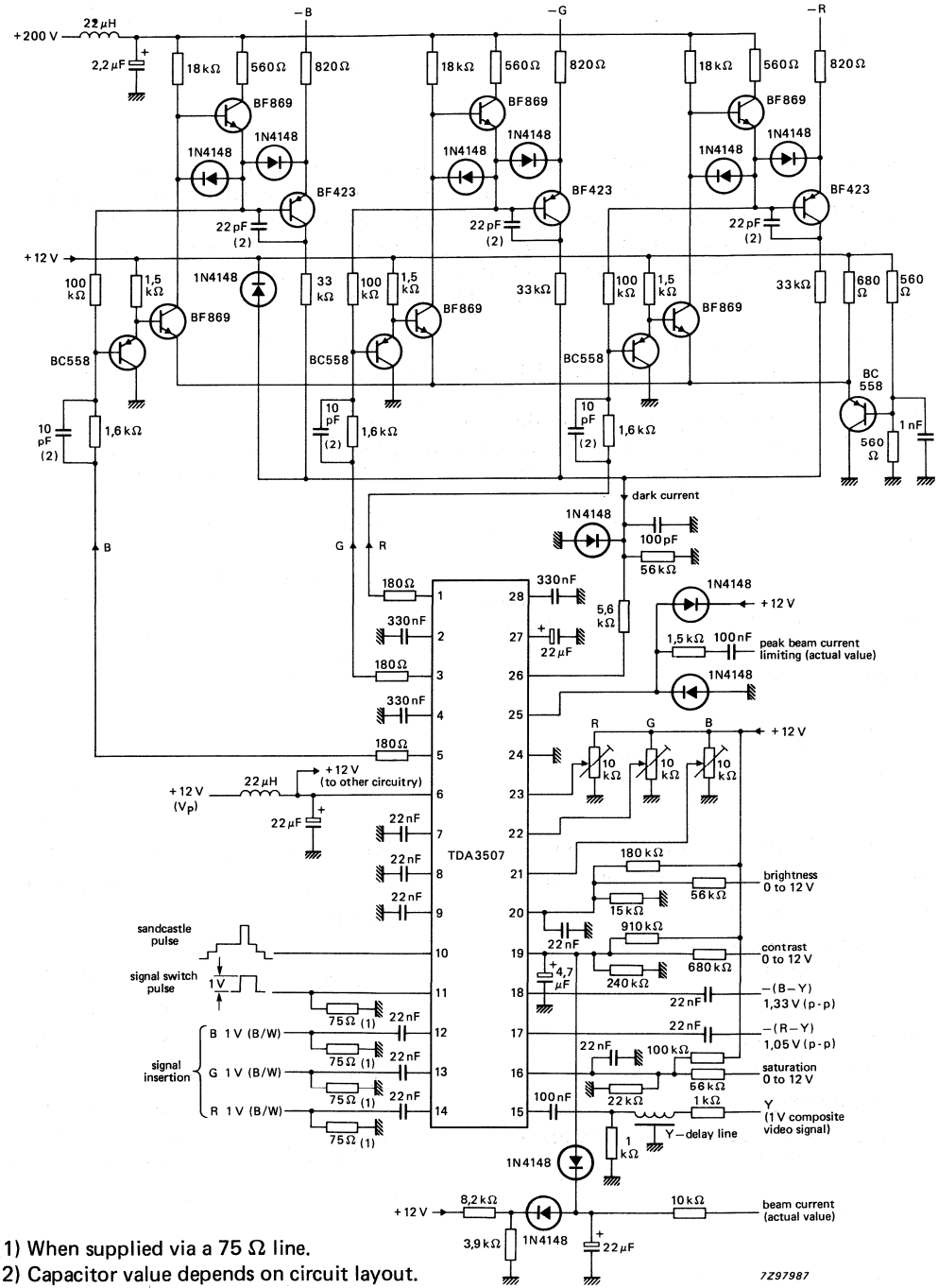
parameter	conditions	symbol	min.	typ.	max.	unit
Gain data (continued)						
Delay time between signal switching and signal insertion		t_d	−25	–	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	–	–	10	%
Sandcastle pulse detector (pin 10)	note 7					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 8	V_{10}	1,0	1,5	2,0	V
required pulses (H+V)		V_{10}	2,1	2,5	2,9	V
horizontal pulses		V_{10}	3,0	3,5	4,0	V
required pulses (H)		V_{10}	4,1	4,5	5,0	V
clamping pulses	note 9	V_{10}	6,5	7,0	7,5	V
required pulses		V_{10}	7,6	–	12,0	V
no keying		V_{10}	–	–	1,0	V
Input current		$-I_{10}$	–	–	110	μA

Notes to the characteristics

1. Values are proportional to the supply voltage.
2. When $V_{11\text{-}24} < 0{,}4$ V during clamping time – the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
   When $V_{11\text{-}24} > 0{,}9$ V during clamping time – the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
3. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5,5 V is supplied.
4. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:
   line 12: measurement of leakage current (R + G + B)
   line 13: measurement of red cut-off current
   line 14: measurement of green cut-off current
   line 15: measurement of blue cut-off current
5. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
6. All three channels blanked to ultra-black.
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
   The internal blanking continues until the end of the last measured line.
   The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.

7. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) and the given levels separate the various pulses.
8. Blanked to ultra-black (−25%).
9. Pulse duration $\geqslant 3{,}5\ \mu s$.

APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using the TDA3507.

Vervanger voor TDA 3560

PAL DECODER

The TDA3561A is a decoder for the PAL colour television standard. It combines all functions required for the identification and demodulation of PAL signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. (Teletext/ broadcast antiope), channel number display, etc. Additional to the TDA3560, the circuit includes the following features:

- The peak white limiter is only active during the time that the 9,3 V level at the output is exceeded. The start of the limiting function is delayed by one line period. This avoids peak white limiting by test patterns which have abrupt transitions from colour to white signals.
- The brightness control is obtained by inserting a variable pulse in the luminance channel. Therefore the ratio of brightness variation and signal amplitude at the three outputs will be identical and independent of the difference in gain of the three channels. Thus discolouring due to adjustment of contrast and brightness is avoided.
- Improved suppression of the internal RGB signals when the device is switched to external signals, and vice versa.
- Non-synchronized external RGB signals do not disturb the black level of the internal signals.
- Improved suppression of the residual 4,4 MHz signal in the RGB output stages.
- Cascoded stages in the demodulators and burst phase detector minimize the radiation of the colour demodulator inputs.
- High current capability of the RGB outputs and the chrominance output.

QUICK REFERENCE DATA

Supply voltage	V_{1-27}	type.	12	V
Supply current	I_1	typ.	85	mA
Luminance input signal (peak-to-peak value)	$V_{10-27(p-p)}$	typ.	0,45	V
Chrominance input signal (peak-to-peak value)	$V_{3-27(p-p)}$	55 to	1100	mV
Data input signals (peak-to-peak value)	$V_{13,15,17-27(p-p)}$	typ.	1	V
RGB output signals at nominal contrast and saturation (peak-to-peak value)	$V_{12,14,16-27(p-p)}$	typ.	5,25	V
Contrast control range		typ.	20	dB
Saturation control range		min.	50	dB
Input voltage for data insertion	V_{9-27}	min.	0,9	V
Blanking input voltage	V_{8-27}	typ.	1,5	V
Burst gating and black-level gating input voltage	V_{8-27}	typ.	7	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

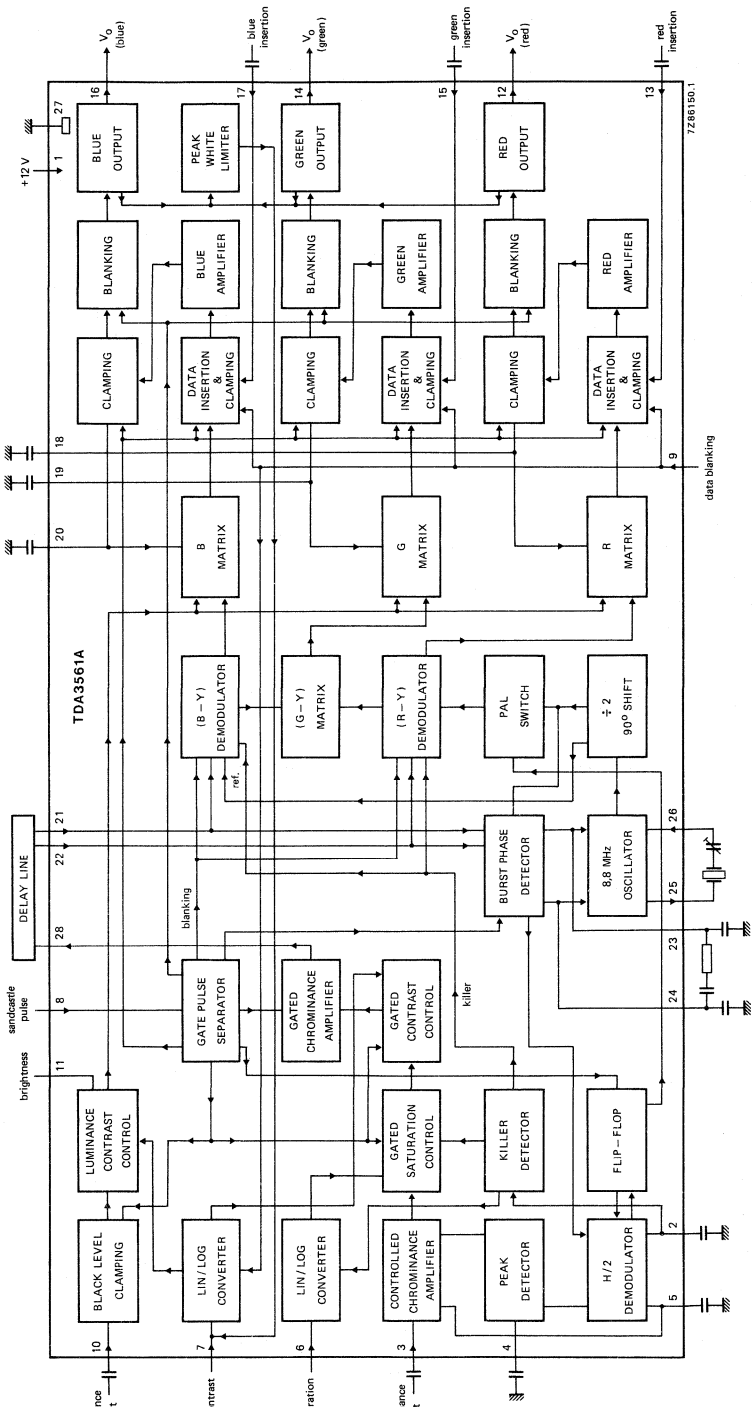


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{1-27}$	max.	13,2	V
Total power dissipation; see also Fig. 2	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	50	K/W

CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

Supply voltage	$V_P = V_{1-27}$	typ.	12	V
			8 to 13,2	V
Supply current		typ.	85	mA
		<	115	mA
Total power dissipation	P_{tot}	typ.	1,0	W
		<	1,4	W
Luminance input (pin 10)				
Input voltage (peak-to-peak value); note 1	$V_{10-27(p-p)}$	typ.	0,45	V
Input level before clipping	V_{10-27}	<	2	V
Input current; input level 2 V, clamp not active	I_{10}	typ.	0,15	μA
		<	1	μA
Contrast control range (see Fig. 3)			−17 to + 3	dB
Control voltage for 40 dB attenuation	V_{7-27}	typ.	1,2	V
Input current contrast control at $V_{7-27} = 3$ V	I_7	<	10	μA
Chrominance amplifier				
Input voltage (peak-to-peak value); note 2	$V_{3-27(p-p)}$	typ.	550	mV
			55 to 1100	mV
Input impedance	$\lvert Z_{3-27}\rvert$	typ.	9	kΩ
			6 to 12	kΩ
Input capacitance	C_{3-27}	typ.	4	pF
		<	6	pF
A.C.C. control range		>	30	dB
Change of the burst signal at the output over the whole control range		<	1,5	dB
Gain at nominal contrast/saturation pin 3 to pin 28; note 3		>	32	dB
Output signal (peak-to-peak value) at nominal contrast/saturation; burst signal: 0,5 V peak to peak	$V_{28-27(p-p)}$	typ.	1,7	V
Maximum output voltage (peak-to-peak value) $R_L = 2$ kΩ	$V_{28-27(p-p)}$	typ.	4,0	V

CHARACTERISTICS (continued)

Chrominance amplifier (continued)

Distortion of chrominance amplifier at $V_{28\text{-}27(p\text{-}p)}$ = 2 V up to $V_{3\text{-}27(p\text{-}p)}$ = 1 V	d	typ. <	1,5 5	% %
Frequency response between 0 and 5 MHz			−2	dB
Saturation control range (see Fig. 4)		>	50	dB
Input current saturation control at $V_{6\text{-}27}$ = 3 V	I_6	<	15	μA
Tracking between luminance and chrominance with contrast control over a range of 10 dB		<	2	dB
Cross-coupling between luminance and chrominance amplifier; note 10		<	−46	dB
Signal-to-noise ratio at nominal input signal; note 11	S/N	>	56	dB
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	<	± 5°	
Output impedance of chrominance amplifier	$\lvert Z_{28\text{-}27}\rvert$	typ.	25	Ω
Maximum output current	I_{28}	<	15	mA

Reference part

Phase locked loop:				
– catching range; note 4		> typ.	500 700	Hz Hz
– phase shift; note 5		<	5°	
Oscillator:				
– temperature coefficient of oscillator frequency; note 4		typ.	−1,5	Hz/K
– frequency deviation for V_P changing from 10 to 13,2 V; note 4		typ.	40	Hz
– input resistance (pin 26)	$R_{26\text{-}27}$	typ. 260 to 420	340	Ω Ω
– input capacitance (pin 26)	$C_{26\text{-}27}$	<	10	pF
– output resistance (pin 25)	$R_{25\text{-}27}$	typ. 100 to 200	150	Ω Ω
– output voltage (peak-to-peak value; pin 25)	$V_{25\text{-}27(p\text{-}p)}$	typ.	700	mV
A.C.C. generation:				
– reference voltage (pin 4)	$V_{4\text{-}27}$	typ.	4,9	V
– control voltage at nominal input signal (pin 2)	$V_{2\text{-}27}$	typ.	5,1	V
– control voltage without chrominance input (pin 2)	$V_{2\text{-}27}$	typ.	2,65	V
– colour-off voltage (pin 2)	$V_{2\text{-}27}$	typ.	3,15	V
– colour-on voltage (pin 2)	$V_{2\text{-}27}$	typ.	3,4	V
– identification-on voltage (pin 2)	$V_{2\text{-}27}$	typ.	1,9	V
– change in burst amplitude with supply voltage (± 10%)		proportional		
– change in burst amplitude with temperature		typ. <	0,1 0,25	%/K %/K
– voltage at pin 5 at nominal input signal	$V_{5\text{-}27}$	typ.	5	V

Demodulator part

Input burst signal amplitude (peak-to-peak value) between pins 21 and 22; note 6	$V_{21\text{-}22(p\text{-}p)}$	typ.	100 mV
Input impedance between pins 21 and 22	$\lvert Z_{21\text{-}22}\rvert$	typ.	2 kΩ
Ratio of demodulated signals for equal input signals at pins 21 and 22 (B−Y)/(R−Y)	$\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$	typ.	1,78 ± 10%
(G−Y)/(R−Y); no (B−Y) signal	$\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$	typ.	−0,51 ± 10%
(G−Y)/(B−Y); no (R−Y) signal	$\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$	typ.	−0,19 ± 25%
Frequency response between 0 and 1 MHz			−3 dB
Cross talk between colour demodulated signals		>	40 dB
Phase difference between (R−Y) signal and (R−Y) reference signal		<	5°
Phase difference between (R−Y) and (B−Y) reference signals		typ.	90° 85 to 95°

R.G.B. matrix and amplifiers

Output voltage (peak-to-peak value) at nominal luminance/contrast (black to white); note 3	$V_{12,14,16\text{-}27(p\text{-}p)}$	typ.	5,4 V 4,5 to 6,3 V
Output voltage (peak-to-peak value) of the RED channel at nominal contrast/saturation and no luminance signal at the input, (R−Y) signal	$V_{12\text{-}27(p\text{-}p)}$	typ.	5,25 V 3,7 to 6,7 V
Maximum peak white level; note 7		typ.	9,3 V 9,0 to 9,6 V
Maximum output current	$I_{12,14,16}$	<	15 mA
Black level at the output for a brightness control voltage of 2 V	$V_{12,14,16\text{-}27}$	typ.	2,6 V
Difference in black level between the three channels at an output level of 3 V; note 8	ΔV	<	200 mV
Black level shift with vision contents		<	40 mV
Brightness control voltage range	see Fig. 5		
Input current brightness control	I_{11}	<	50 μA
Variation of black level with temperature	ΔV	typ. <	0,35 mV/K 1,0 mV/K
Variation of black level with contrast control	ΔV	typ. <	10 mV 200 mV
Relative spread between the R, G and B output signals		<	10 %
Relative black-level variation between the three channels during variation of contrast and supply voltage		typ. <	0 mV 20 mV

CHARACTERISTICS (continued)

RGB matrix and amplifier (continued)

Differential black-level drift over a temperature range of 40 °C		typ. <	0 20	mV mV
Blanking level at the RGB outputs		typ. 1,9 to 2,3	2,1	V V
Difference in blanking level of the three channels		typ.	0	mV
Differential blanking level drift over a temperature range of 40 °C		typ.	0	mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	typ.	1,1	
Signal-to-noise ratio of output signals; note 11	S/N	>	62	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)		typ. <	40 150	mV mV
Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		typ. <	75 150	mV mV
Output impedance of RGB outputs	$\lvert Z_{12,14,16-27} \rvert$	typ.	50	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		<	−3	dB

Signal insertion (pins 13,15 and 17)

Input signals (peak-to-peak value) for an RGB output voltage of 5 V peak-to-peak	$V_{13,15,17-27(p-p)}$	typ. 0,85 to 1,1	1	V V
Difference between the black levels of the RGB signals and the inserted signals at the output; note 9	ΔV	<	260	mV
Output rise time	t_r	typ. <	40 80	ns ns
Differential delay time for the three channels	t_d	typ. <	0 40	ns ns
Input current	$I_{13,15,17}$	<	10	μA

Data blanking (pin 9)

Input voltage for no data insertion	V_{9-27}	<	0,4	V
Input voltage for data insertion	V_{9-27}	>	0,9	V
Maximum input voltage	V_{9-27}	<	3	V
Delay of data blanking	t_d	<	20	ns
Input current	I_9	<	35	μA
Input impedance	$\lvert Z_{9-27} \rvert$	typ.	10	kΩ
Suppression of the internal RGB signals when $V_{9-27} > 0,9$ V		>	46	dB

Sandcastle input (pin 8)

Level at which the RGB blanking is activated	V_{8-27}	typ.	1,5 V 1 to 2 V
Level at which burst gating and clamping pulse are separated	V_{8-27}	typ.	7,0 V 6,5 to 7,5 V
Delay between black level clamping and burst gating pulse	t_d	typ.	0,4 μs
Input current for:			
V_{8-27} = 0 to 1 V	$-I_8$	<	1 mA
V_{8-27} = 1 to 8,5 V	I_8	typ.	20 μA
V_{8-27} = 8,5 to 12 V	I_8	<	2 mA

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for a colour bar with 75% saturation, so chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −3 dB and nominal saturation as the maximum saturation −6 dB.
4. All frequency variations are referred to the 4,4 MHz carrier frequency.
5. For ± 400 Hz deviation of the oscillator frequency.
6. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
7. When this level is exceeded, the amplitude of the output signal is reduced via a discharge of the capacitor at pin 7 (contrast control). The start of the peak white limiting action has a delay of one line period.
8. The variation of the black level depends directly on the gain of each channel during brightness control in the three channels. As a consequence, the black levels at the outputs (for output levels above or below 3 V) can have a difference which exceeds 200 mV. Because the amplitude and the black level change with brightness control have a direct relationship, no discolouring can occur, caused by adjustment of contrast and brightness.
9. This difference occurs when the source impedance of the data signal inputs is 150 Ω and the black level clamp pulse duration is 4 μs (sandcastle pulse). A lower difference is obtained when the impedance is lower.
10. Cross-coupling is measured under the following condition. Input signals nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
11. The signal-to-noise ratio is specified as peak-to-peak signal with respect to r.m.s. noise.

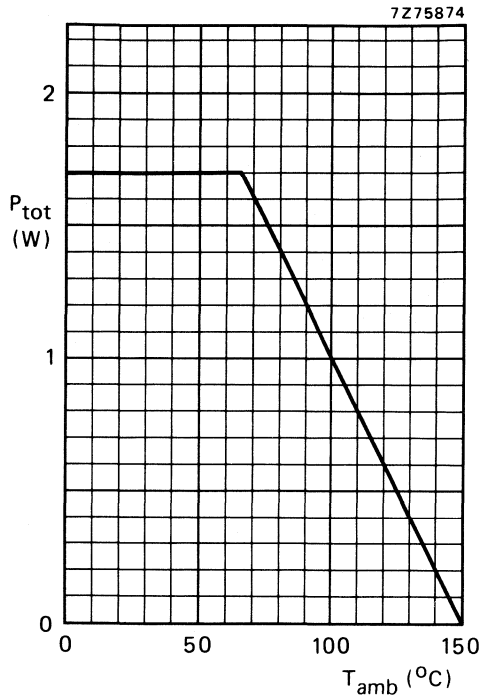


Fig. 2 Power derating curve.

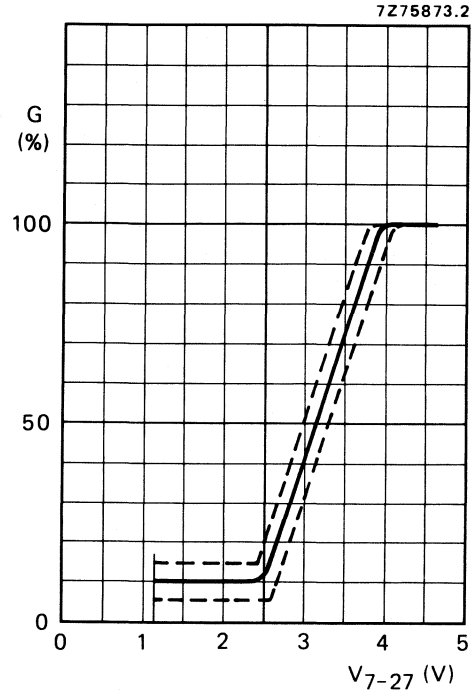


Fig. 3 Contrast control voltage range.

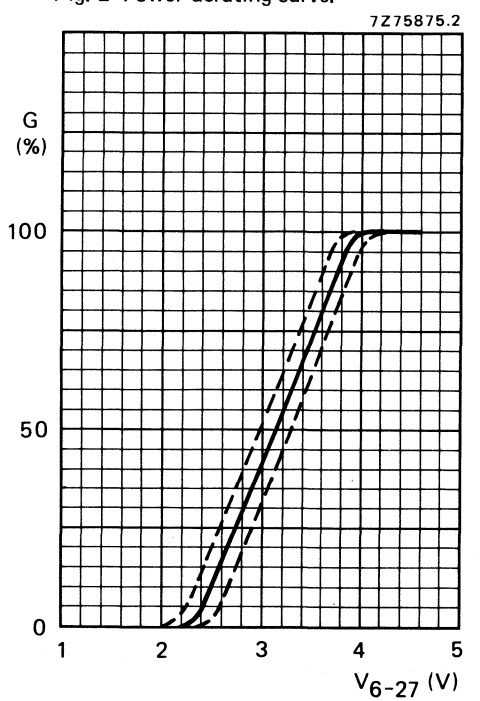


Fig. 4 Saturation control voltage range.

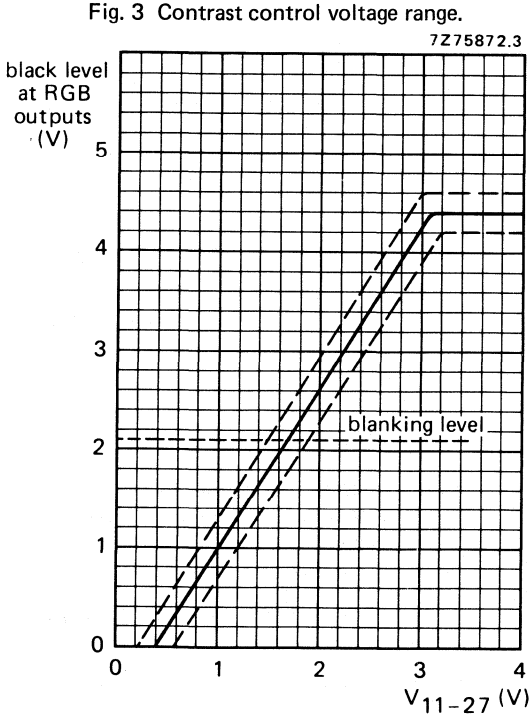


Fig. 5 Brightness control voltage range.

APPLICATION INFORMATION

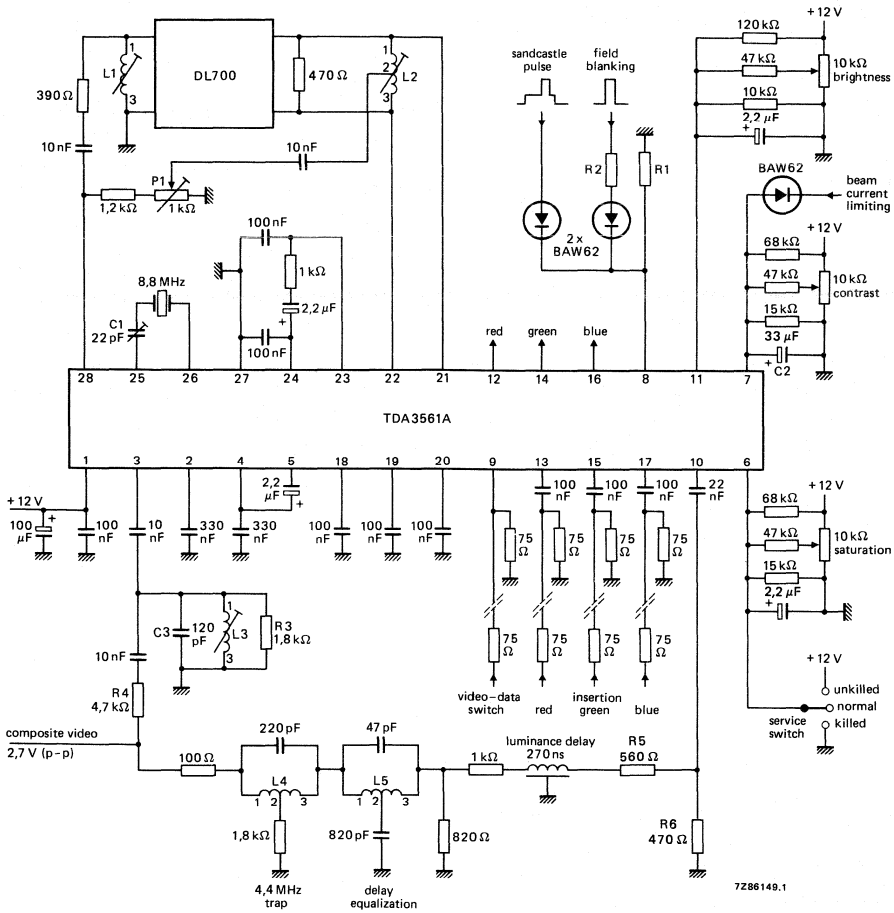


Fig. 6 Application circuit.

Adjustments (see Fig. 6)

C1	8,8 MHz oscillator	
L1	phase delay line	= 10,7 μH
L2	nominal value	= 10,7 μH
L3	4,4 MHz chrominance input filter	= 10,7 μH = L1
L4	4,4 MHz trap in luminance signal line	= 5,6 μH
L5	delay equalization	= 66,1 μH
P1	amplitude of direct chroma singal	
R1 R2	field blanking $\frac{R1}{R1+R2}$ x field blanking amplitude 2,0 V to 6,5 V.	

For a video input voltage of 1 V peak-to-peak: R3 can be omitted; R4 = 1 kΩ; R5 must be short-circuited; R6 = 1 kΩ.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage for the TDA3561A. All signal and control levels have a linear dependency on the supply voltage. The current taken by the device at 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

2. Control voltage for identification

This pin requires a detection capacitor of about 330 nF for correct operation. The voltages available under various signal conditions are given in the specification.

3. Chrominance input

The chroma signal must be a.c.-coupled to the input. Its amplitude must be between 55 mV and 1100 mV peak-to-peak (25 mV to 500 mV peak-to-peak burst signal). All figures for the chroma signals are based on a colour bar signal with 75% saturation, that is the burst-to-chroma ratio of the input signal is 1 : 2,25.

4. Reference voltage A.C.C. detector

This pin must be decoupled by a capacitor of about 330 nF. The voltage at this pin is 4,9 V.

5. Control voltage A.C.C.

The A.C.C. is obtained by synchronous detection of the burst signal followed by a peak detector. A good noise immunity is obtained in this way and an increase of the colour for weak input signals is prevented. The recommended capacitor value at this pin is 2,2 μF.

6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external saturation control network is sufficiently high. Then the chroma amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 25 and 26).

7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak white limiter circuit becomes active and reduces the output signals via the contrast control by discharging C2 via an internal current sink.

8. Sandcastle and field blanking input

The output signals are blanked if the amplitude of the input pulse is between 2 and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V.
The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of video signal on the sync pulse. The width should be about 4 μs for proper A.C.C. operation.

9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 V and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to the negative supply. The switching times are very short ($<$ 20 ns) to avoid coloured edges of the inserted signals on the screen.

10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak white to sync) to obtain a black-white output signal of 5 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage.
A 1 kΩ luminance delay line can be applied because the luminance input impedance is made very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 5). The black level can be set higher than 4 V however the available output signal amplitude is reduced (see pin 7). Brightness control also operates on the black level of the inserted signals.

12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5,25 V (R, G and B) at nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2,1 V. The peak white level is limited to 9,3 V. When this level exceeded the output signal amplitude is reduced via the contrast control (see pin 7).

13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak -to-peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to the negative supply.

18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

21, 22. Inputs (B-Y) and (R-Y) demodulators

The input signal is automatically fixed to the required level by means of the burst phase detector and A.C.C. generator which are connected to pin 21 and pin 22. As the burst (applied differentially to those pins) is kept constant by the A.C.C., the colour difference signals automatically have the correct value.

APPLICATION INFORMATION (continued)

23, 24. Burst phase detector outputs

At these pins the output of the burst phase detector is filtered and controls the reference oscillator. An adequate catching range is obtained with the time constants given in the application circuit (see Fig. 6).

25, 26. Reference oscillator

The frequency of the oscillator is adjusted by the variable capacitor C1. For frequency adjustment interconnect pin 21 and pin 22. The frequency can be measured by connecting a suitable frequency counter to pin 25.

28. Output of the chroma amplifier

Both burst and chroma signals are available at the output. The burst-to-chroma ratio at the output is identical to that at the input for nominal control settings. The burst signal is not affected by the controls. The amplitude of the input signal to the demodulator is kept constant by the A.C.C. Therefore the output signal at pin 28 will depend on the signal loss in the delay line.

PAL DECODER

GENERAL DESCRIPTION

The TDA3565 PAL decoder contains all the functions required for PAL signal decoding and colour matrixing and is contained within an 18-pin package. The oscillator, a.c.c. detector and burst phase detector each have single-pin outputs and the coupling capacitor for the luminance input at pin 8 doubles as a storage capacitor for the black level clamping circuit. Black level clamping of the three colour channels is performed using feedback proportional to the red channel black level. This feedback (variable with the brightness control) controls the input level of the luminance amplifier and therefore the clamping levels of all three colour signal outputs.

QUICK REFERENCE DATA

Supply voltage	$V_p = V_{1-17}$	typ.	12 V
Supply current	$I_P = I_1$	typ.	85 mA
Luminance input signal (peak-to-peak value)	$V_{8-17(p-p)}$	typ.	0,45 V
Chrominance input signal (peak-to-peak value)	$V_{3-17(p-p)}$	typ.	550 mV
RGB output signal amplitudes (peak-to-peak value) at nominal luminance and contrast	$V_{10,11,12-17(p-p)}$	typ.	5 V
Contrast control range			−17 to +3 dB
Saturation control range		>	50 dB
A.C.C. control range		>	30 dB
Level at which RGB blanking is activated	V_{7-17}	typ.	1,5 V
Level at which burst gate/clamping pulse are separated	V_{7-17}	typ.	7 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

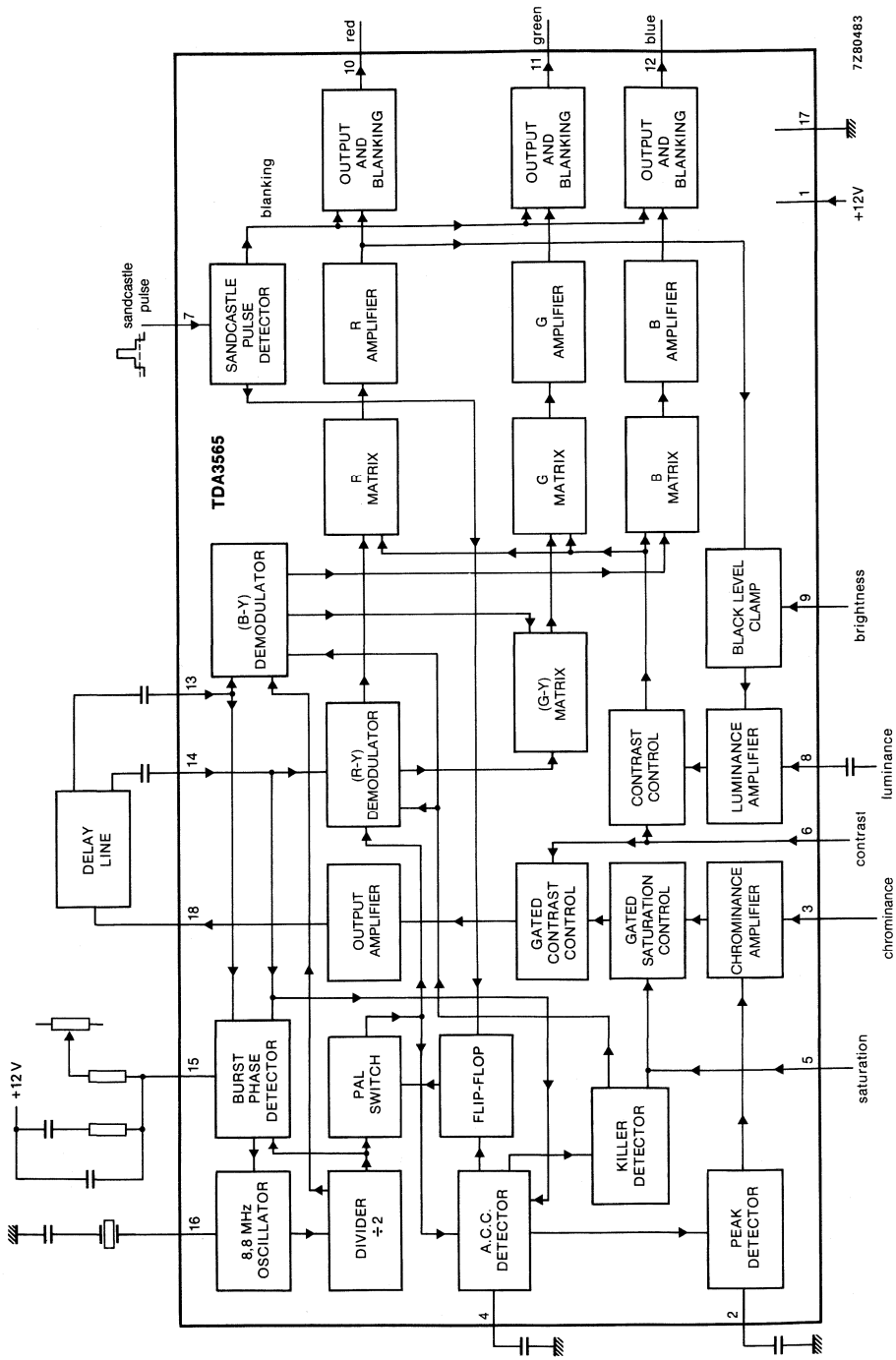


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-17}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Operating ambient temperature range	T_{amb}		−25 to +65	°C
Storage temperature range	T_{stg}		−25 to +150	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	max.	50	K/W

CHARACTERISTICS

$V_P = V_{1-17} = 12$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	V_{1-17}	9,0	12,0	13,2	V
Supply current	I_1	–	85	–	mA
Total power dissipation	P_{tot}	–	1,0	–	W
Luminance amplifier					
Input signal amplitude (note 1) (peak-to-peak value)	$V_{8-17(p-p)}$	–	0,45	–	V
Input level before clipping occurs *	$V_{8-17(p-p)}$	–	–	0,7	V
Input current at $V_{8-17} = 2$ V; clamp not active	I_8	–	0,15	1,0	μA
Contrast control range (Fig. 2)		–	−17 to +3	–	dB
Input current when peak white limiter is active ($V_{6-17} = 2{,}5$ V)	I_8	–	5,5	–	mA
Input resistance $V_{6-17} > 6$ V	R_i	1,4	2,0	2,6	kΩ
Chrominance amplifier					
Input signal amplitude (note 2)	$V_{3-17(p-p)}$	55	550	1100	mV
Minimum burst signal amplitude within the control range (peak-peak)		30	–	–	mV
Input impedance	Z_{3-17}	–	8,0	–	kΩ
Input capacitance	C_{3-17}	–	4,0	6,0	pF
A.C.C. control range		30	–	–	dB
Change of burst signal at output over whole a.c.c. control range		–	–	1	dB
Amplification pin 3 to pin 18 at nominal contrast/saturation (note 3)		32	–	–	dB

* At nominal contrast and nominal brightness.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance amplifier (continued)					
Chroma to burst ratio (note 3)		–	3,8	–	dB
Max. output voltage range (pin 18) $R_L = 2\ k\Omega$		4,0	4,5	–	V
Chrominance amplifier distortion at $V_{8\text{-}17(p\text{-}p)} = 2$ V (output) up to $V_{3\text{-}17(p\text{-}p)} = 1$ V (input)	$d_{8\text{-}3}$	–	3,0	5,0	%
Frequency response between 0 and 5 MHz		–	–	–2	dB
Saturation control range (Fig. 3)		50	–	–	dB
Saturation control input current at $V_{5\text{-}17} < 6$ V	I_5	–	1	20	μA
Input impedance for V_5 between 6 and 10 V	Z_i	1,4	2,0	2,6	kΩ
Input impedance when colour killer is active	Z_i	1,4	2,0	2,6	kΩ
Input impedance for $V_5 > 10$ V (adjustment procedure)	Z_i	0,7	1,0	1,3	kΩ
Tracking between luminance and chrominance over 10 dB of contrast control range		–	–	2	dB
Cross coupling between luminance and chrominance amplifiers (note 4)		–	–	–46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB
Burst phase shift with respect to chrominance at nominal contrast/saturation (note 3)	$\Delta\varphi$	–	–	±5	deg
Chrominance amplifier output impedance	$Z_{18\text{-}17}$	–	25	–	Ω
Output current (pin 18)	I_{18}	–	–	10	mA
Reference part					
Phase-locked loop					
Catching range	Δf	500	700	–	Hz
Phase shift for ± 400 Hz deviation of oscillator frequency	$\Delta\varphi$	–	–	5	deg
Oscillator					
Temperature coefficient of oscillator frequency	TC_{osc}	–	2	3	Hz/K
Frequency deviation when supply voltage changes from 10 to 13,2 V	Δf_{osc}	–	200	300	Hz

parameter	symbol	min.	typ.	max.	unit
Input resistance	$R_{16\text{-}17}$	250	290	330	Ω
Input capacitance	$C_{16\text{-}17}$	–	–	10	pF
A.C.C. generation					
Voltage with nominal input signal	$V_{4\text{-}17}$	–	5,0	–	V
Voltage without chrominance input	$V_{4\text{-}17}$	–	2,5	–	V
Colour-off voltage	$V_{4\text{-}17}$	–	3,2	–	V
Colour-on voltage	$V_{4\text{-}17}$	–	3,5	–	V
Identification-on voltage	$V_{4\text{-}17}$	–	2,5	–	V
Pin 2 voltage at nominal input signal	$V_{2\text{-}17}$	–	5,1	–	V
Demodulator part					
Burst signal amplitude (peak-to-peak value) at pins 13 and 14 (note 6)	$V_{13\text{-}17(p\text{-}p)}$ $V_{14\text{-}17(p\text{-}p)}$	–	80	–	mV
Input impedance of pins 13 or 14 to pin 17	$Z_{13,\,14\text{-}17}$	–	1,0	–	kΩ
Ratios of demodulated signals with equal signal inputs to pins 13 and 14 and no luminance input signal:					
(B-Y)/(R-Y)	$\frac{V_{12\text{-}17}}{V_{10\text{-}17}}$	–	1,78±10%	–	
(G-Y)/(R-Y) (no (B-Y) signal)	$\frac{V_{11\text{-}17}}{V_{10\text{-}17}}$	–	−0,51±10%	–	
(G-Y)/(B-Y) (no (R-Y) signal)	$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	−0,19±10%	–	
Frequency response between 0 and 1 MHz		–	–	−3	dB
Separation of colour difference channels		40	–	–	dB
Phase difference between (R-Y) signal and (R-Y) reference signal	$\Delta\varphi$	–	–	5	deg
Phase difference between (R-Y) and (B-Y) reference signals	$\Delta\varphi$	85	90	95	deg
RGB matrix and amplifiers					
Output signal amplitudes (peak-to-peak value) at nominal luminance signal and contrast inputs (black-white) (note 3)	$V_{10\text{-}17(p\text{-}p)}$ $V_{11\text{-}17(p\text{-}p)}$ $V_{12\text{-}17(p\text{-}p)}$	4,5	5,0	5,5	V
Red channel output amplitude (peak-to-peak value) at nominal contrast/saturation (note 3) and no luminance signal to (R-Y)	$V_{10\text{-}17(p\text{-}p)}$	3,7	5,25	7,4	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Maximum peak white level (note 7)		9,0	9,3	9,6	V
Maximum output current	$I_{10,11,12}$	–	–	15	mA
Red channel black level output when brightness control V_{9-17} = 2 V	V_{10-17}	–	2,7	–	V
Difference between black levels in R, G and B outputs		–	–	600	mV
Black level shift with picture content		–	–	40	mV
Brightness control voltage range	V_{9-17}	see Fig. 3			
Brightness control input current at V_{9-17} = 2 V	I_9	–	–	–50	μA
Variation of black level with temperature		–	+0,35	1,0	mV/K
Variation of black level with contrast control		–	10	100	mV
Relative spread between the three channel outputs		–	–	10	%
Relative variation in black level between the three channels during normal variations of contrast and supply voltage		–	0	20	mV
Differential drift of black level over a temperature range of 40 °C		–	0	20	mV
Blanking level at the three channel outputs		1,9	2,1	2,3	V
Difference in blanking level of the three channel outputs		–	0	–	mV
Differential drift of blanking levels over a temperature range of 40 °C		–	0	–	mV
Tracking of output black levels with variation of supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	–	1,1	–	
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 4,4 MHz component in output signals (peak-to-peak value)		–	25	50	mV
Residual 8,8 MHz and higher harmonic components in output signals (peak-to-peak value)		–	25	50	mV
Output impedance	$Z_{10,11,12-17}$	–	50	–	Ω
Frequency response of total luminance/RGB amplifier circuits for 0 to 5 MHz		–	–	–3	dB

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector					
Level at which RGB blanking is activated	V_{7-17}	1,0	1,5	2,0	V
Level at which burst gate and clamping pulse are separated	V_{7-17}	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		–	0,4	–	μs
Input current at:					
V_{7-17} = 0 to 1 V	I_7	–	–	−1	mA
V_{7-17} = 1 to 8,5 V	I_7	–	20	40	μA
V_{7-17} = 8,5 to 12 V	I_7	–	–	2	mA

Notes to the characteristics

1. Signal with negative-going sync pulse, amplitude includes sync pulse amplitude.
2. The signal indicated is for a colour bar with 75% saturation, so the chroma burst ratio of 2,2 : 1.
3. Nominal contrast is defined as (maximum contrast −3 dB) and nominal saturation is (maximum saturation −12 dB).
4. Cross coupling is measured under the following condition; input signals nominal and contrast/saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal signal at that output.
5. The signal-to-noise ratio is specified as peak-to-peak signal with respect to r.m.s. noise.
6. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
7. When this level is exceeded the amplitude of the output signal is reduced via a discharge of the capacitor at pin 6 (contrast control). The discharge current is 5,5 mA.

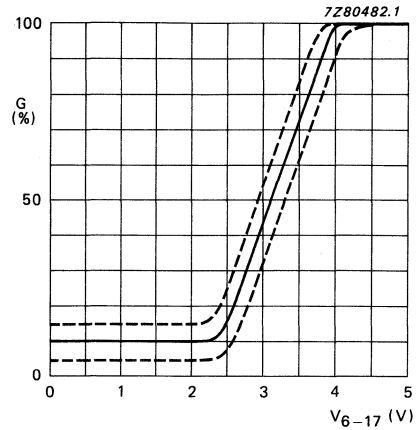


Fig. 2 Luminance contrast control voltage range.

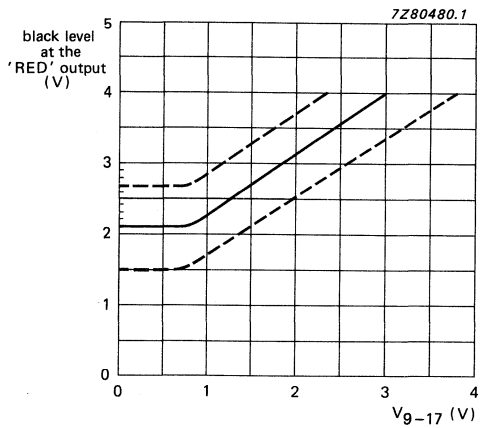


Fig. 3 Brightness control voltage range.

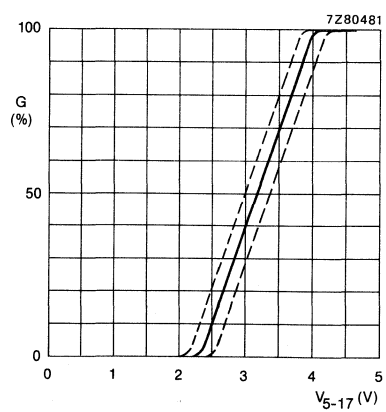


Fig. 4 Saturation control voltage range.

APPLICATION INFORMATION

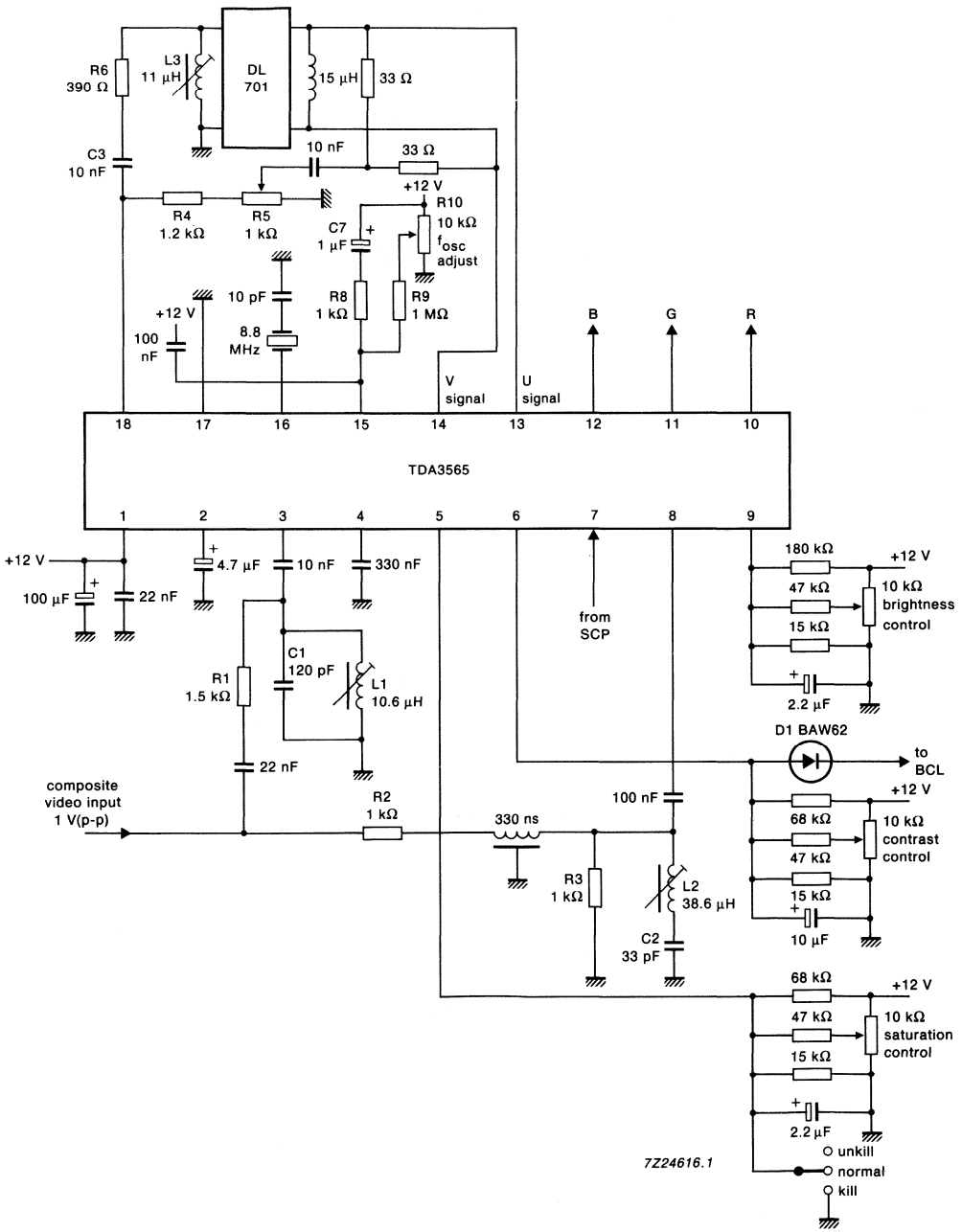


Fig. 5 Application diagram

PAL/NTSC DECODER

GENERAL DESCRIPTION

The TDA3566 is a monolithic integrated decoder for the PAL and/or NTSC colour television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 4 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. Teletext/broadcast antiope), channel number display, etc.

Features

- A black-current stabilizer which controls the black-currents of the three electron-guns to a level low enough to omit the black-level adjustment
- Contrast control of inserted RGB signals
- No black-level disturbance when non-synchronized external RGB signals are available on the inputs
- NTSC capability with hue control

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1-27}$	typ.	12 V
Supply current (pin 1)	$I_P = I_1$	typ.	80 mA
Luminance amplifier (pin 8)			
Input voltage (peak-to-peak value)	$V_{8-27(p-p)}$	typ.	450 mV
Contrast control range		typ.	20 dB
Chrominance amplifier (pin 4)			
Input voltage range (peak-to-peak value)	$V_{4-27(p-p)}$	40 to	1100 mV
Saturation control range		min.	50 dB
RGB matrix and amplifiers			
Output voltage at nominal luminance and contrast (peak-to-peak value)	$V_{13, 15, 17-27(p-p)}$	typ.	4 V
Data insertion			
Input signals (peak-to-peak value)	$V_{12, 14, 16-27(p-p)}$	typ.	1 V
Data blanking (pin 9)			
Input voltage for data insertion	V_{9-27}	min.	0,9 V
Sandcastle input (pin 7)			
Blanking input voltage	V_{7-27}	typ.	1,5 V
Burst gating and clamping input voltage	V_{7-27}	typ.	7 V

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT117).

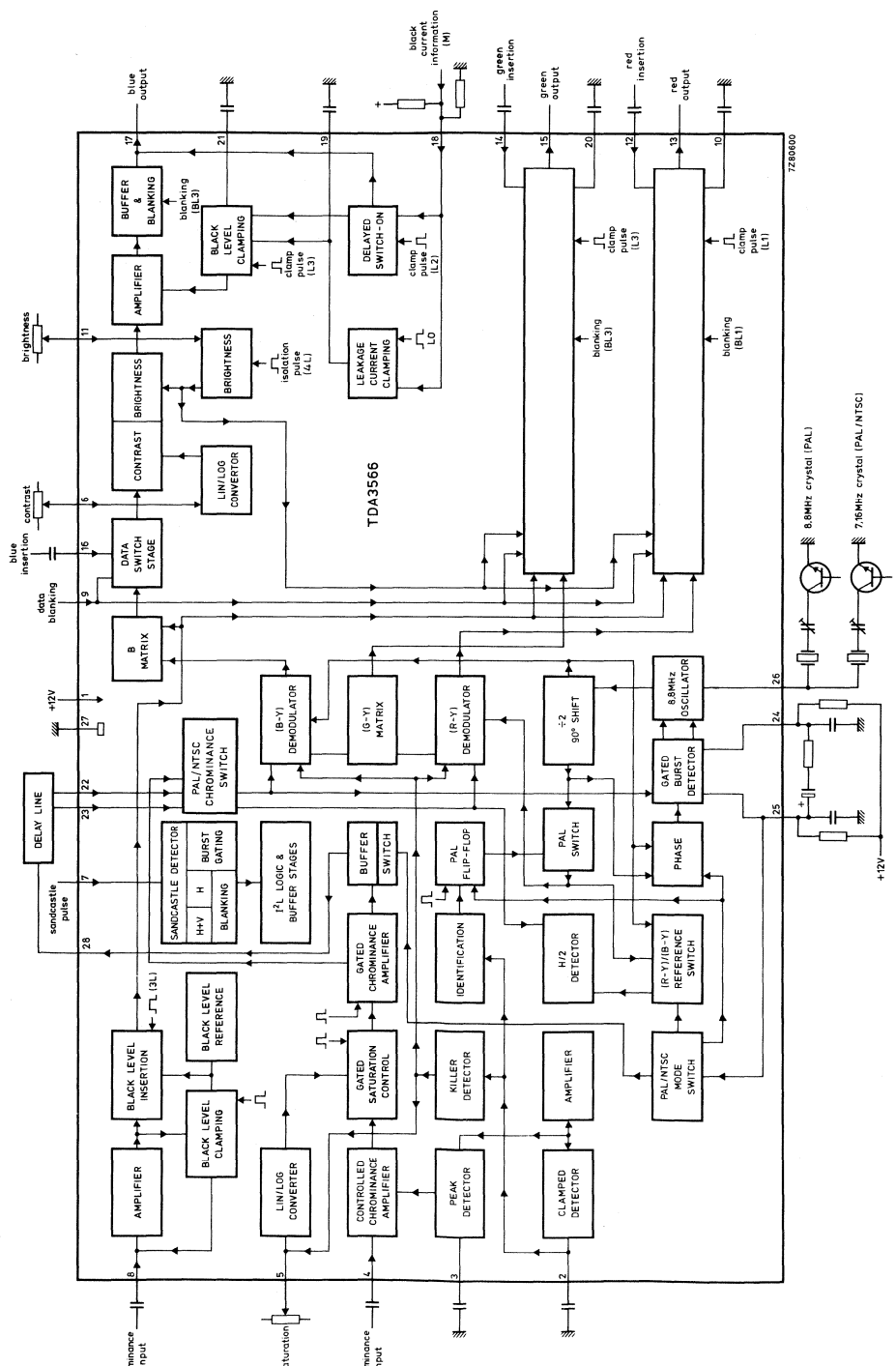


Fig. 1 Block diagram; for explanation of pulse mnemonics see Fig. 6.

FUNCTIONAL DESCRIPTION

The TDA3566 is a further development of the TDA3562A. It has the same pinning and almost the same application. The differences between the TDA3562A and the TDA3566 are as follows:

- The NTSC-application has largely been simplified. In the case of NTSC the chroma signal is now internally coupled to the demodulators, ACC and phase detectors. The chroma output signal (pin 28) is suppressed in this case. It follows that the external switches and filters which are needed for the TDA3562A are not needed for the TDA3566.
  Furthermore there is no difference between the amplitude of the colour output signals in the PAL or NTSC mode. The PAL/NTSC-switch and the hue control of the TDA3566 and the TDA3562A are identical.
- The switch-on and the switch-off behaviour of the TDA3566 has been improved. This has been obtained by suppressing the output signals during the switch-on and switch-off periods.
- The clamp capacitors connected to the pins 10, 20 and 21 can be reduced to 100 nF for the TDA3566. The clamp capacitors also receive a pre-bias voltage to avoid coloured background during switch-on.
- The crystal oscillator circuit has been changed to prevent parasitic oscillations on the third overtone of the crystal. This has the consequence that optimal tuning capacitance must be reduced to 10 pF.

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal is a.c. coupled to the input (pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed d.c. level by the black level clamping circuit. During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit. This black level reference voltage is controlled via pin 11 (brightness). At the same time the RGB signals are clamped. Noise and residual signals have no influence during clamping thus simple internal clamping circuitry is used.

Chrominance amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be a.c. coupled (pin 4) and have a minimum amplitude of 40 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. Form the gain control stage the chrominance signal is fed to the saturation control stage. Saturation is linear controlled via pin 5. The control voltage range is 2 to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12 dB higher gain during the chrominance signal. As a result the signal at the output (pin 28) has a burst to chrominance ratio which is 6 dB lower than that of the input signal when the saturation control is set at −6 dB. The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (pins 22 and 23). These signals are fed to the burst phase detector.
In the case of NTSC the chroma signal is internally coupled to the demodulators, ACC and phase detector.

FUNCTIONAL DESCRIPTION (continued)

Oscillator and identification circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (pin 7). In the detector the (R-Y) and (B-Y) signals are added to provide the composite burst signal again. This composite signal is compared with the oscillator signal divided-by-2 ((R-Y) reference signal). The control voltage is available at pins 24 and 25, and is also applied to the 8,8 MHz oscillator. The 4,4 MHz signal is obtained via the divide-by-2 circuit, which generates both the (B-Y) and (R-Y) reference signals and provides a 90^{o} phase shift between them.
The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R-Y) reference signal coming from the PAL switch, is compared to the vertical signal (R-Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst. When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the a.c.c. To avoid 'blooming-up' of the picture under weak input signal conditions the a.c.c. voltage is generated by peak detection of the H/2 detector output signal.

The killer and identification circuits get their information from a gated output signal of the H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression. The time constant of the saturation control (pin 5) provides a delayed switch-on after killing.
Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between pins 24 and 25 (see Fig. 7). With this application the trimmer capacitor in series with the 8,8 MHz crystal (pin 26) can be replaced by a fixed value capacitor to compensate for unbalance of the phase detector.

Demodulator

The (R-Y) and (B-Y) demodulators are driven by the colour difference signals from the delay-line matrix circuit and the reference signals from the 8,8 MHz divider circuit. The (R-Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G-matrix. The demodulation circuits are killed and blanked by by-passing the input signals.

NTSC mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (pins 24 and 25) is adjusted below 9 V. To ensure reliable application the phase detector load resistors are external. When the TDA3566 is used only for PAL these two 33 kΩ resistors must be connected to + 12 V (see Fig. 7). For PAL/NTSC application the value of each resistor must be reduced to 10 kΩ and connected to the slider of a potentiometer (see Fig. 8). The switching transistor brings the voltage at pins 24 and 25 below 9 V which switches the circuit to the NTSC mode. The position of the PAL flip-flop ensures that the correct phase of the (R-Y) reference signal is supplied to the (R-Y) demodulator. The drive to the H/2 detector is now provided by the (B-Y) reference signal. (In the PAL mode it is driven by the (R-Y) reference signal.)
Hue control is realized by changing the phase of the reference drive to the burst phase detector. This is achieved by varying the voltage at pins 24 and 25 between 7,5 V and 8,5 V, nominal position 8,0 V. The hue control characteristic is shown in Fig. 5.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.
The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal, which is then fed to the contrast control stage. The contrast control voltage is supplied to pin 6 (high-input impedance). The control range is + 3 dB to −17 dB nominal. The relationship between the control voltage and the gain is linear (see Fig. 2).
During the 3-line period after blanking a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at pin 11. This applies a variable offset to the normal black level, thus providing brightness control. The brightness control range is 1 V to 3 V.

While this offset level is present, the 'black-current' input impedance (pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at pin 19 with the voltage developed across the external resistor network R_A and R_B (pin 18) which is provided by picture tube beam current. The output of the comparator is stored in capacitors connected from pins 10, 20 and 21 to ground which controls the black level at the output. The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.
The RGB output signals can never exceed a level of 10 V. When the signal tends to exceed this level the output signal is clipped. The black level at the outputs (pins 13, 15 and 17) will be about 3 V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (pin 18) via a resistor network.

Data insertion

Each colour amplifier has a separate input for data insertion. A 1 V peak-to-peak input signal provides a 4 V peak-to-peak output signal. To avoid the 'black-level' of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore a.c. coupling is required for the data inputs.
To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150 Ω.
The data insertion circuit is activated by the data blanking input (pin 9). When the voltage at this pin exceeds a level of 0,9 V, the RGB matrix circuits are switched off and the data amplifiers are switched on. To avoid coloured edges, the data blanking switching time is short.
The amplitude of the data output signals is controlled by the contrast control at pin 6. The black level is equal to the video black level and can be varied between 2 and 4 V (nominal condition) by the brightness control voltage at pin 11.
Non-synchronized data signals do not disturb the black level of the internal signals.

Blanking of RGB and data signals

Both the RGB and data signals can be blanked via the sandcastle input (pin 7). A slicing level of 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of + 1 V is available at the output.
To prevent parasitic oscillations on the third overtone of the crystal the optimal tuning capacitance should be 10 pF.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-27}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Storage temperature range	T_{stg}	−25 to	+ 150 °C
Operating ambient temperature range	T_{amb}	−25 to	+ 70 °C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	40 K/W

CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1-27}$	10,8	12	13,2	V
Supply current	$I_P = I_1$	–	80	110	mA
Total power dissipation	P_{tot}	–	0,95	1,3	W
Luminance amplifier (pin 8)					
Input voltage (note 1) (peak-to-peak value)	$V_{8-27(p-p)}$	–	0,45	0,63	V
Input level before clipping	V_{8-27}	–	–	1.4	V
Input current	I_8	–	0,1	1	μA
Contrast control range (see Fig. 2)		−15	–	+5	dB
Input current contrast control	I_7	–	–	15	μA
Chrominance amplifier (pin 4)					
Input voltage (note 2) (peak-to-peak value)	$V_{4-27(p-p)}$	40	390	1100	mV
Input impedance (pin 4)	$\lvert Z_{4-27}\rvert$	–	10	–	kΩ
Input capacitance	C_{4-27}	–	–	6,5	pF
A.C.C. control range		30	–	–	dB
Change of the burst signal at the output over the whole control range	ΔV	–	–	1	dB
Gain at nominal contrast/saturation pin 4 to pin 28 (note 3)	G	34	–	–	dB
Chrominance to burst ratio at nominal saturation (notes 2 and 3) at pin 28		–	12	–	dB
Maximum output voltage range (peak-to-peak value); $R_L = 2$ kΩ	$V_{28-27(p-p)}$	4	5	–	V
Distortion of chrominance amplifier at $V_{28-27(p-p)} = 2$ V (output) up to $V_{4-27(p-p)} = 1$ V (input)	d	–	–	5	%
Frequency response between 0 and 5 MHz	α_{28-4}	–	–	−2	dB
Saturation control range (see Fig. 3)		50	–	–	dB
Input current saturation control (pin 5)	I_5	–	–	20	μA
Cross-coupling between luminance and chrominance amplifier (note 4)		–	–	−46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance amplifier (continued)					
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	–	–	± 5	deg
Output impedance of chrominance amplifier	$\lvert Z_{28\text{-}27}\rvert$	–	10	–	Ω
Output current	I_{28}	–	–	15	mA
Reference part					
Phase-locked-loop					
catching range (note 6)	Δf	500	700	–	Hz
phase shift for ± 400 Hz deviation of f_{osc} (note 6)	$\Delta\varphi$	–	–	5	deg
Oscillator					
temperature coefficient of oscillator frequency (note 6)	TC_{osc}	–	–2	–3	Hz/K
frequency variation when supply voltage increases from 10 to 13,2 V (note 6)	Δf_{osc}	–	40	100	Hz
input resistance (pin 26)	$R_{26\text{-}27}$	280	400	520	Ω
input capacitance (pin 26)	$C_{26\text{-}27}$	–	–	10	pF
A.C.C. generation (pin 2)					
control voltage at nominal input signal	$V_{2\text{-}27}$	–	4,5	–	V
control voltage without chrominance input	$V_{2\text{-}27}$	–	2	–	V
colour-off voltage	$V_{2\text{-}27}$	–	2,8	–	V
colour-on voltage	$V_{2\text{-}27}$	–	3	–	V
identification-on voltage	$V_{2\text{-}27}$	–	1,7	–	V
change in burst amplitude with temperature		–	0,1	0,25	%/K
voltage at pin 3 at nominal input signal	$V_{3\text{-}27}$	–	5,1	–	V
Demodulator part					
Input burst signal amplitude (peak-to-peak value between pins 23 and 27 (note 7)	$V_{23\text{-}27(p\text{-}p)}$	68	80	95	mV
Input impedance between pins 22 or 23 and 27	$\lvert Z_{22\text{-}27/23\text{-}27}\rvert$	0,7	1	1,3	kΩ
Ratio of demodulated signals (note 8)					
(B-Y)/(R-Y)	$\frac{V_{17\text{-}27}}{V_{13\text{-}27}}$	–	1,78 ± 10%	–	
(G-Y)/(R-Y); no (B-Y) signal	$\frac{V_{15\text{-}27}}{V_{13\text{-}27}}$	–	–0,51 ± 10%	–	
(G-Y)/(B-Y); no (R-Y) signal	$\frac{V_{15\text{-}27}}{V_{17\text{-}27}}$	–	–0,19 ± 10%	–	

parameter	symbol	min.	typ.	max.	unit
Demodulator part (continued)					
Frequency response between 0 and 1 MHz	α_{17}	–	–	–3	dB
Cross-talk between colour difference signals		40	–	–	dB
Phase difference between (R-Y) signal and (R-Y) reference signals	$\Delta\varphi$	–	–	5	deg
Phase difference between (R-Y) signal and (B-Y) reference signals	$\Delta\varphi$	85	90	95	deg
RGB matrix and amplifiers					
Output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white) (note 3)	$V_{13,15,17\text{-}27(p\text{-}p)}$	3,5	4	4,5	V
Output voltage at pin 13 (peak-to-peak value) at nominal contrast/saturation and no luminance signal to (R-Y)	$V_{13\text{-}27(p\text{-}p)}$	–	4,2	–	V
Maximum peak-white level	$V_{13,15,17\ (m)}$	9,7	10	10,3	V
Available output current (pins 13, 15 17)	$I_{13,15,17}$	10	–	–	mA
Difference between black level and measuring level at the output for a brightness control voltage at pin 11 of 2 V (note 9)	$\Delta V_{13,15,17\text{-}27}$	–	0	–	V
Difference in black level between the three channels without black current stabilization (note 10)	ΔV	–	–	100	mV
Control range of black-current stabilization at V_{b1} = 3 V; $V_{11\text{-}17}$ = 2 V		–	–	± 2	V
Black level shift with vision contents	ΔV	–	–	40	mV
Brightness control voltage range		see Fig. 4			
Brightness control input current	I_{11}	–	–	5	μA
Variation of black level with temperature	$\Delta V/\Delta T$	–	0	–	mV/K
Variation of black level with contrast*	ΔV	–	–	100	mV
Relative spread between the R, G and B output signals		–	–	10	%
Relative black-level variation between the three channels during variation of contrast, brightness and supply voltage (± 10%)*	ΔV	–	0	20	mV
Differential black-level drift over a temperature range of 40 °C	ΔV	–	0	20	mV
Blanking level at the RGB outputs	V_{bl}	–	0,95	1,1	V

* With respect to the measuring pulses.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers (continued)					
Difference in blanking level of the three channels	V_{bl}	–	0	–	mV
Differential drift of the blanking levels over a temperature range of 40 °C	V_{bl}	–	0	10	mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	0,9	1	1,1	
Tracking of contrast control between the three channels over a control range at 10 dB		–	–	0,5	dB
Output signal during the clamp pulse (3L) after switch-on	V_O	7,5	–	–	V
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)	$V_{R(p-p)}$	–	–	50	mV
Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)	$V_{R(p-p)}$	–	–	150	mV
Output impedance of RGB outputs	$\lvert Z_{13,15,17-27} \rvert$	–	50	–	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 9 MHz	α	–	−1	−3	dB
Current source of output stage	I_O	2	3	–	mA
Difference of black level at the three outputs at nominal brightness*	ΔV	–	–	10	mV
Tracking of brightness control		–	–	2	%
Signal insertion (pins 12, 14 and 16)					
Input signals (peak-to-peak value) for and RGB output voltage of 3.5 V (peak-to-peak) at nominal contrast	$V_{12,14,16-27(p-p)}$	0,9	1	1,1	V
Difference between the black levels of the RGB signals and the inserted signals at the output (note 11)	ΔV	–	–	100	mV
Output rise time	t_r	–	50	80	ns
Differential delay time for the three channels	t_d	–	0	40	ns
Input current	$I_{12,14,16}$	–	–	10	μA

* With respect to the measuring pulses.

parameter	symbol	min.	typ.	max.	unit
Data blanking (pin 9)					
Input voltage for no data insertion	$V_{9\text{-}27}$	–	–	0,4	V
Input voltage for data insertion	$V_{9\text{-}27}$	0,9	–	–	V
Maximum input voltage	$V_{9\text{-}27(m)}$	–	–	3	V
Delay of data blanking	t_d	–	–	20	ns
Input resistance	$R_{9\text{-}27}$	7	10	13	kΩ
Suppression of the internal RGB signals when $V_{9\text{-}27} > 0{,}9$ V		46	–	–	dB
Sandcastle input (pin 7)					
Level at which the RGB blanking is activated	$V_{7\text{-}27}$	1	1,5	2	V
Level at which the horizontal pulses are separated	$V_{7\text{-}27}$	3	3,5	4	V
Level at which burst gating and clamping pulse are separated	$V_{7\text{-}27}$	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse	t_d	–	0,6	–	μs
Input current					
at $V_{7\text{-}27}$ = 0 to 1 V	$-I_7$	–	–	1	mA
at $V_{7\text{-}27}$ = 1 to 8,5 V	I_7	–	–	50	μA
at $V_{7\text{-}27}$ = 8,5 to 12 V	I_7	–	–	2	mA
Black current stabilization (pin 18)					
Bias voltage (d.c.)	$V_{18\text{-}27}$	3,5	5	7,0	V
Difference between input voltage for 'black' current and leakage current	ΔV	0,35	0,5	0,65	V
Input current during 'black' current	I_{18}	–	–	1	μA
Input current during scan	I_{18}	–	–	10	mA
Internal limiting at pin 10	$V_{18\text{-}27}$	8,5	9	9,5	V
Switching threshold for 'black' current control ON	$V_{18\text{-}27}$	7,6	8	8,4	V
Input resistance during scan	$R_{18\text{-}27}$	1	1,5	2	kΩ
Input current during scan at pins 10, 20 and 21 (d.c.)	$I_{10,\ 20,\ 21}$	–	–	tbf	nA
Maximum charge/discharge current during measuring time		–	1	–	nA
NTSC					
Level at which the PAL/NTSC switch is activated (pins 24 and 25)	$V_{24\text{-}25}$	–	8,8	9,2	V
Average output current (note 12)	$I_{24\ +\ 25(AV)}$	75	90	105	μA
Hue control		see Fig. 5			

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −5 dB and nominal saturation as the maximum saturation −6 dB.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to r.m.s. noise.
6. All frequency variations are referred to 4,4 MHz carrier frequency.
7. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
8. The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal. This also applies to the (B-Y) signals.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5 V) but in that application the amplitude of the output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discolouration during adjustments of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. This difference occurs when the source impedance of the data signals is 150 Ω and the black level clamp pulse width is 4 μs (sandcastle pulse). For a lower impedance the difference will be lower.
12. The voltage at pins 24 and 25 can be changed by connecting the load resistors (10 kΩ in this application) to the slider bar of the hue control potentiometer (see Fig. 8). When the transistor is switched on, the voltage at pins 24 and 25 is reduced below 9 V, and the circuit is switched to NTSC mode. The width of the burst gate is assumed to be 4 μs typical.

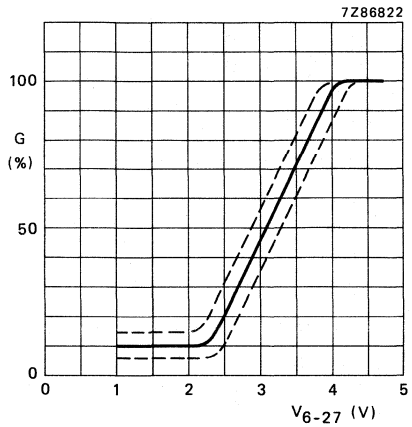


Fig. 2 Contrast control voltage range.

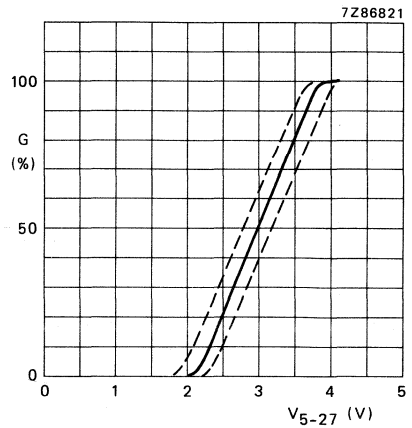


Fig. 3 Saturation control voltage range.

DEVELOPMENT DATA

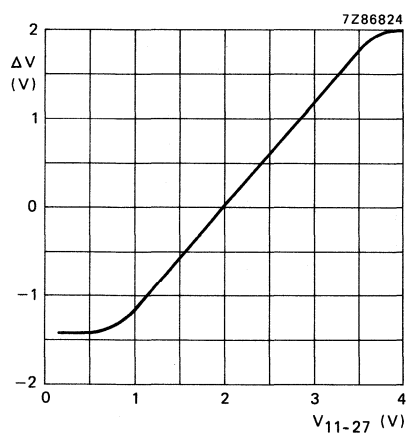


Fig. 4 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the brightness control input voltage (V_{11-27}).

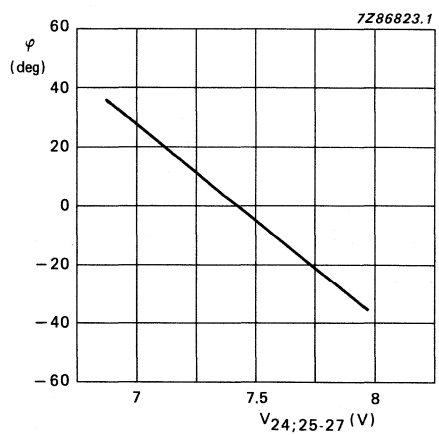


Fig. 5 Hue control voltage range.

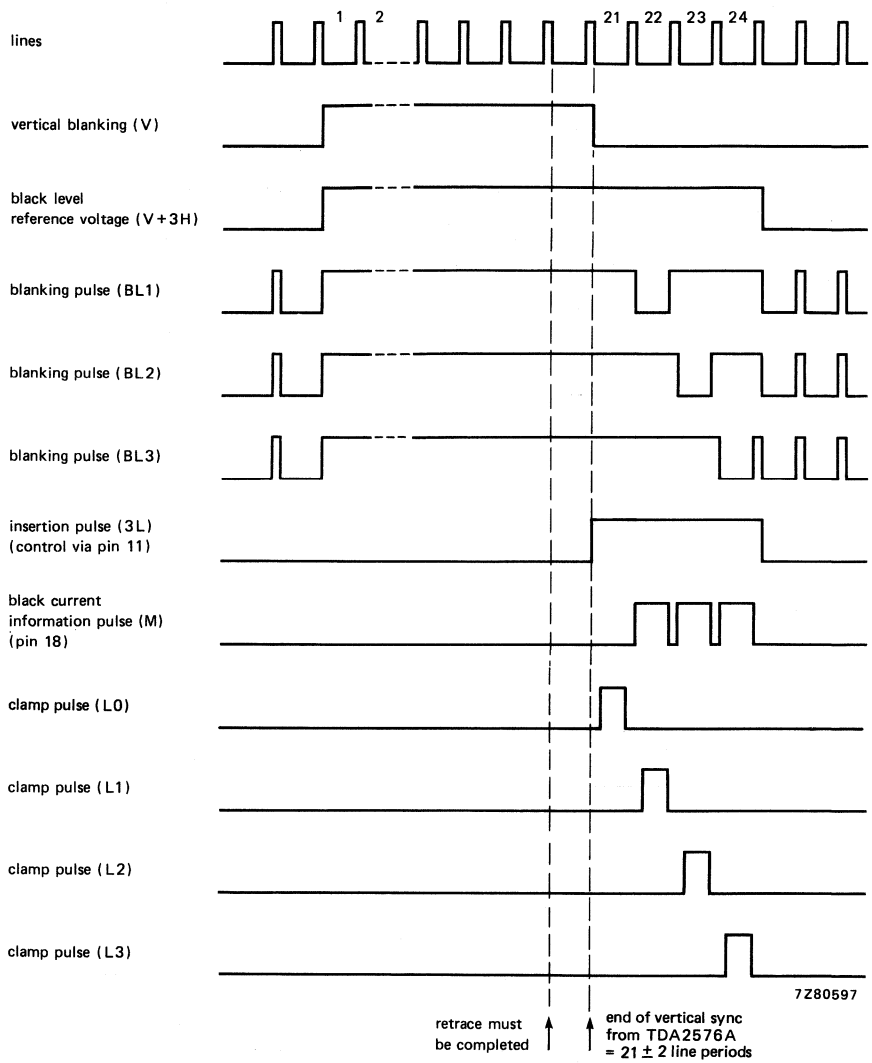


Fig. 6 Timing diagram for black-current stabilizing.

APPLICATION INFORMATION

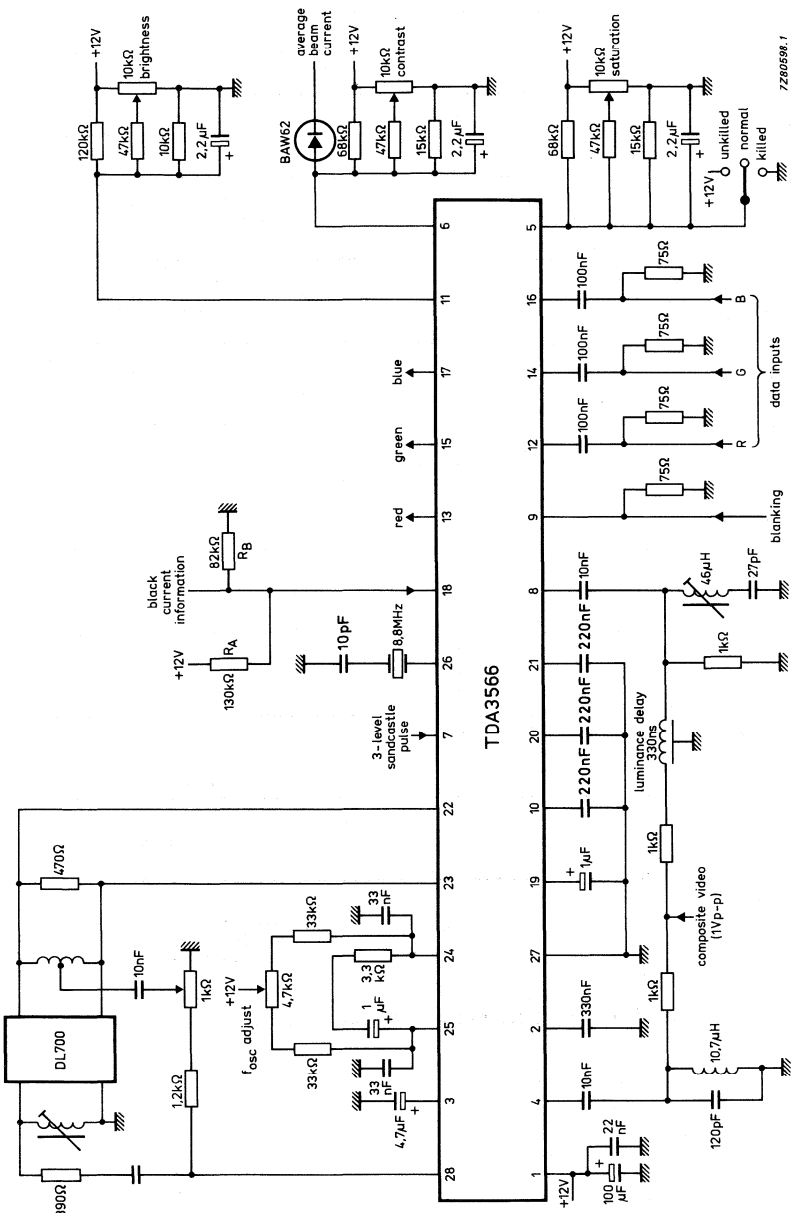


Fig. 7 Application diagram showing the TDA3566 for a PAL decoder.

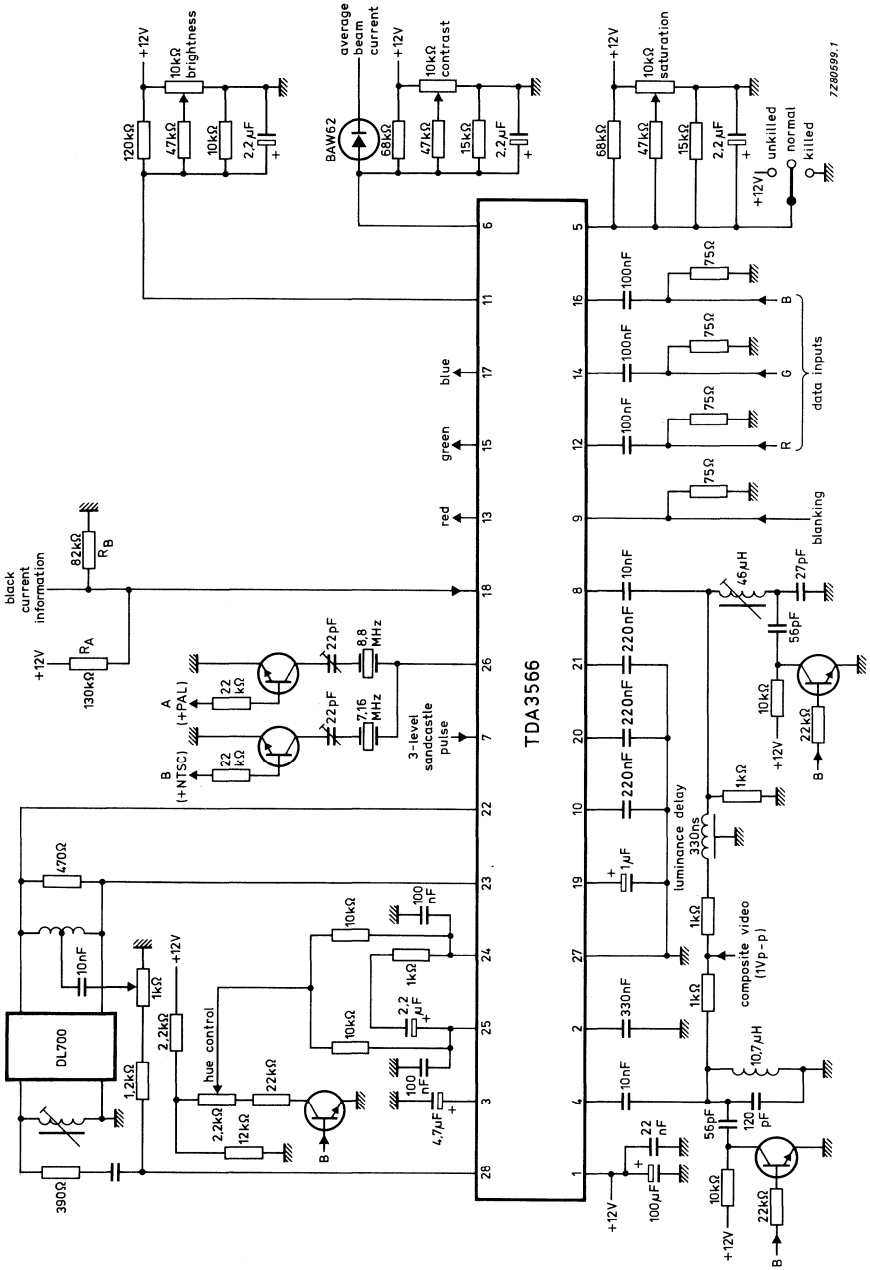


Fig. 8 Application diagram showing the TDA3566 for a PAL/NTSC decoder.

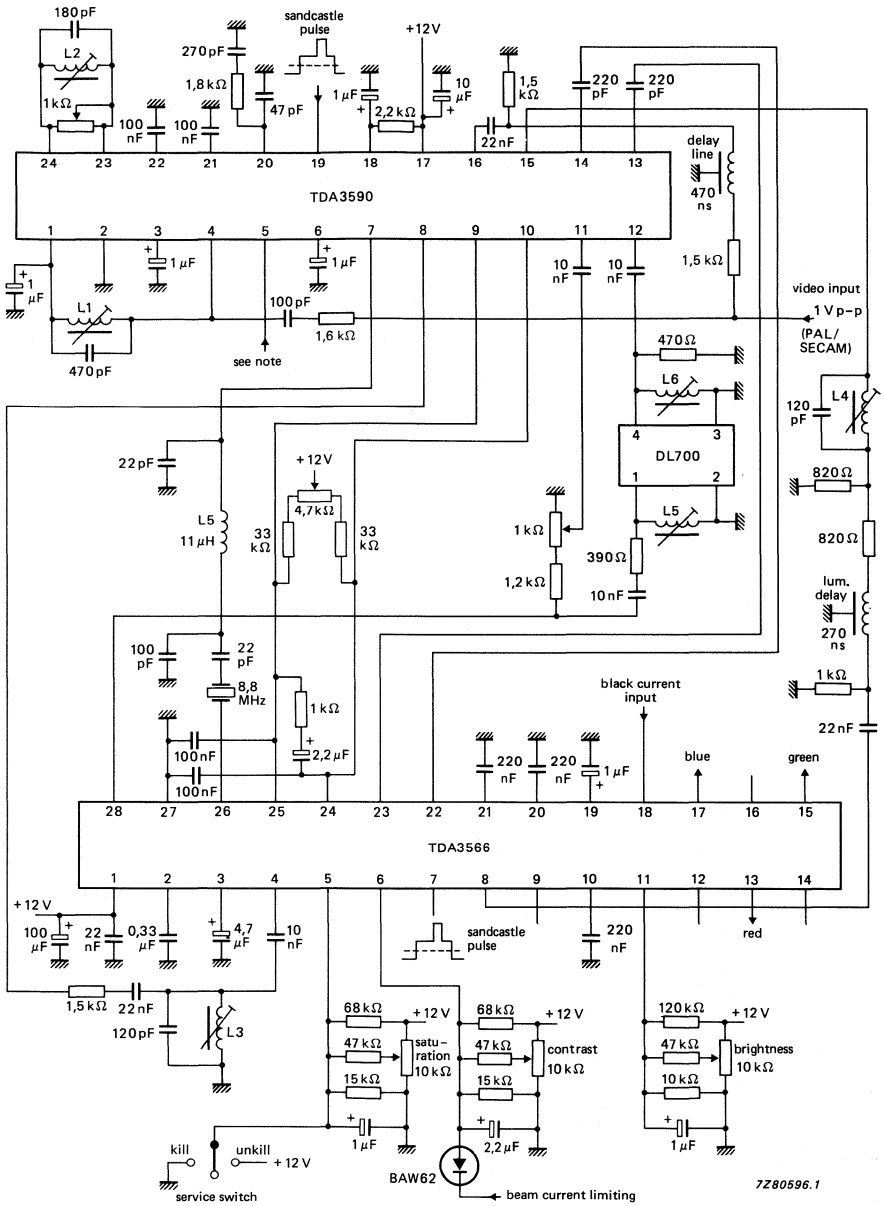


Fig. 9 PAL/SECAM application circuit diagram using the TDA3590 and TDA3566.

Note to pin 5 TDA3590:

$V_{5-2} < 1$ V; horizontal identification and black level clamping.
$V_{5-2} > 11$ V; vertical identification and artificial black level.
V_{5-2} = 5 to 7 V; horizontal identification and artificial black level.

NTSC DECODER

GENERAL DESCRIPTION

The TDA3567 is a monolithic integrated decoder for the NTSC colour television standards. It combines all functions required for the demodulation of NTSC signals. Further more it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 1	$V_P = V_{1-17}$	9	12	13,2	V
Supply current	pin 1	$I_P = I_1$	–	65	–	mA
Luminance input signal	pin 8					
Input voltage (peak-to-peak value)		$V_{8-17(p-p)}$	–	0,45	–	V
Contrast control range			–	20	–	dB
Chrominance amplifier	pin 3					
Input voltage (peak-to-peak value)		$V_{3-17(p-p)}$	–	550	–	mV
Saturation control range			50	–	–	dB
RGB matrix and amplifiers						
Output voltage at nominal luminance input signal and nominal contrast (peak-to-peak value)		$V_{10,11,12-17(p-p)}$	4,0	5,0	6,0	V
Sandcastle input	pin 7					
Blanking input voltage		V_{7-17}	1,0	1,5	2,0	V
Burst gating and clamping input voltage		$V_{7-17(p-p)}$	6,5	7,0	7,5	V

PACKAGE OUTLINE

18-lead DIL; plastic, with internal heatspreader (SOT102).

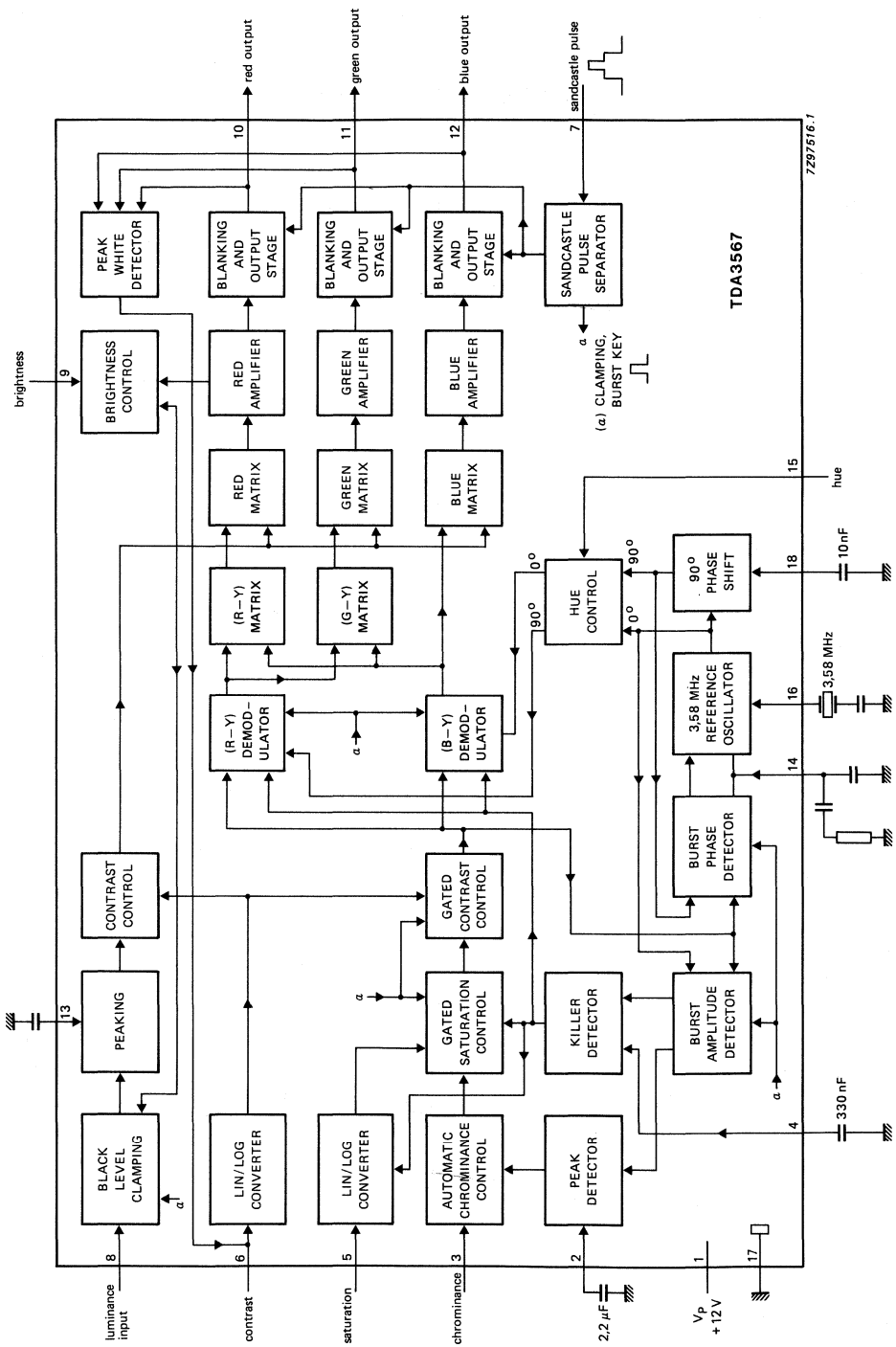


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak*. The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal must be a.c. coupled to the input pin 8.

The black level clamp circuit of the RGB amplifiers uses the coupling capacitor as a storage capacitor. After clamping the signal is fed to a peaking stage. The RC network connected to pin 13 is used to define the amount of overshoot.

The peaking stage is followed by a contrast control stage. The control voltage has to be supplied to pin 6. The control voltage range is nominally −17 to + 3 dB. The linear curve of the contrast control voltage is shown in Fig. 2.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal at pin 3 must be a.c. coupled, and must have an amplitude of 550 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal should not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation and contrast control stages. Chrominance and luminance control stages are directly coupled to obtain good tracking. The saturation is linearly controlled via pin 5. The control voltage range is 2 V to 4 V. The impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by contrast or saturation control. After the amplification and control stages the chrominance signal is internally fed to the (R-Y) and (B-Y) demodulators, burst phase and a.c.c. detectors.

Oscillator and a.c.c. circuit

The 3,58 MHz reference oscillator operates at the subcarrier frequency. The crystal must be connected between pin 16 and ground. The oscillator does not require adjustment due to the small spreads of the IC. The free running frequency of the oscillator can be checked by connecting the saturation control (pin 5) to the positive supply line. Then the loop is opened, so that the frequency can be measured. The oscillator has an internal gain limiting stage which controls the gain to unity, so that internal signals are sinusoidal. This prevents the generation of higher harmonics of the subcarrier signals. The burst signal is compared to a 0^{o} reference signal by the burst amplitude detector and is then amplified and fed to a peak detector for a.c.c. and to a sample and hold circuit which drives the colour killer circuit. The reference signal for the burst phase detector is provided by the 90^{o} phase shifted signal. An RC network is used to obtain the required catching range and noise immunity for the output voltage of the burst phase detector.

The hue control is obtained by mixing oscillator signals with a phase of 0^{o} and 90^{o} before they are fed to the (R-Y) and (B-Y) demodulators. The 90^{o} phase shifted signal is provided by a miller integrator (biased by pin 18). As the hue control is independent of the PLL, the control will react without time delay on the control voltage changes.

* Signal with negative going sync; amplitude includes sync pulse amplitude.

FUNCTIONAL DESCRIPTION (continued)

Demodulator circuits

The demodulators are driven by the amplified and controlled chrominance signals, the reference signals are obtained from the hue control circuit. In nominal hue control position the phase angle of (R-Y) reference signal is 0°, the phase angle of the (B-Y) reference signal is 90°.

For flesh tone corrections the demodulated (R-Y) signal is matrixed with the demodulated (B-Y) signal according to the following equations:

$(R\text{-}Y)_{matrixed} = 1{,}61\ (R\text{-}Y)_{IN} - 0{,}42\ (B\text{-}Y)_{IN}$

$(G\text{-}Y)_{matrixed} = 0{,}43\ (R\text{-}Y)_{IN} - 0{,}11\ (B\text{-}Y)_{IN}$

$(B\text{-}Y)_{matrixed} = (B\text{-}Y)_{IN}$

In these equations $(R\text{-}Y)_{IN}$ and $(B\text{-}Y)_{IN}$ indicate the colour difference signal amplitudes, when the chrominance signal is demodulated with a phase difference between the R-Y and B-Y demodulator of 90° and a gain ratio B-Y/R-Y = 1,78.

RGB matrix circuit and amplifiers

The three matrix and amplifier circuits are identical. The luminance signal and the colour difference signals are added in the matrix circuit to obtain the colour signal.

Output signals are 5 V (peak-to-peak) (black-white) for the following nominal input signals and control settings.

- Luminance 450 mV (peak-to-peak)
- Chrominance 550 mV (peak-to-peak) (burst-to-chrominance ratio of the input 1 : 2.2)
- Contrast −3 dB (maximum)
- Saturation −10 dB (maximum)

The maximum available output voltage is approximately 7 V (peak-to-peak). The black level of the red channel is compared with a variable external reference level (pin 9), which provides the brightness control. The control loop is closed via the luminance input.

The luminance input is varied to control the black level control, therefore the green and blue outputs will follow any variation of the red output. The output of the black control can be varied between 2 V to 4 V. The corresponding brightness control voltage is shown in Fig. 4.

If the output signal surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB signals

A slicing level of about 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the rest of the pulse. During blanking a level of + 2 V is available at the output.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-17}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	50 K/W

CHARACTERISTICS

$V_P = V_{1-17} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{1-17}$	9	12	13,2	V
Supply current		$I_P = I_1$	–	65	–	mA
Total power dissipation		P_{tot}	–	0,78	–	W
Luminance input signal						
Input voltage (peak-to-peak value)	note 1 pin 8	$V_{8-17(p-p)}$	–	450	–	mV
Input voltage level before clipping occurs in the input stage		V_{8-17}	–	–	1	V
Input current		I_8	–	0,15	1,0	μA
Contrast control range	see Fig. 2		−17	–	+ 3	dB
Input current contrast control	for $V_{6-17} < 6$ V	I_7	–	0,5	15	μA
Input current when the peak-white limiter is active	$V_{6-17} = 2,5$ V	I_7	–	5,5	–	mA
Input resistance	$V_{6-17} > 6$ V	R_{7-17}	1,4	2,0	2,6	kΩ
Peaking of luminance signal						
Output impedance	pin 13	$\lvert Z_{13-17} \rvert$	–	200	–	Ω
Ratio of internal/external current when pin 13 is short-circuited			–	3	–	

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance amplifier						
Input signal amplitude (peak-to-peak value)	note 2 pin 3	$V_{3\text{-}17(p\text{-}p)}$	–	550	–	mV
Input signal amplitude before clipping occurs in the input stage (peak-to-peak value)		$V_{3\text{-}17(p\text{-}p)}$	–	–	1,1	V
Minimum burst signal amplitude within the a.c.c. control range (peak-to-peak)			35	–	–	mV
A.C.C. control range			30	–	–	dB
Change of the burst signal at the output for the complete control range		ΔV	–	–	+ 1	dB
Input impedance	pin 3	$\lvert Z_{3\text{-}17}\rvert$	6	8	10	kΩ
Input capacitance	pin 3	$C_{3\text{-}17}$	–	4	6	pF
Saturation control range	see Fig. 3		50	–	–	dB
Input current saturation control	for $V_{5\text{-}17} > 6$ V	I_5	–	1	20	μA
Input impedance	$V_{5\text{-}17} = 6$ V to 10 V	$\lvert Z_{5\text{-}17}\rvert$	1,4	2,0	2,6	kΩ
Input impedance when the colour killer is active		$\lvert Z_{5\text{-}17}\rvert$	1,4	2,0	2,6	kΩ
Input impedance	for $V_{5\text{-}17} > 10$ V	$\lvert Z_{5\text{-}17}\rvert$	0,7	1,0	1,3	kΩ
Tracking between luminance and chrominance contrast	for 10 dB of control		–	1	2	dB
Cross coupling between luminance and chrominance amplifier	note 4		–	–50	–46	dB
Reference part						
Phase locked loop						
Catching range		Δf	±400	±500	–	Hz
Phase shift for 400 Hz deviation of the carrier frequency		Δ	–	–	5	deg

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Temperature coefficient of oscillator frequency		TC_{osc}	–	1,5	2,5	Hz/K
Frequency deviation	$\Delta V_P = \pm 10\%$	Δf_{osc9}	–	150	250	Hz
Input resistance	pin 16	$R_{16\text{-}17}$	260	360	460	Ω
Input capacitance	pin 16	$C_{22\text{-}17}$	–	–	10	pF
A.C.C. generation						
Voltage at pin 4 nominal input signal		$V_{4\text{-}17}$	–	4,0	–	V
Voltage at pin 4 without burst input		$V_{4\text{-}17}$	–	1,9	–	V
Colour-off voltage		$V_{4\text{-}17}$	–	2,5	–	V
Colour-on voltage		$V_{4\text{-}17}$	–	2,8	–	V
Change in burst amplitude with temperature			–	0,1	–	%/K
Change in burst amplitude with 10% supply voltage change			–	0	–	%/V
Voltage at pin 2 at nominal input signal		$V_{2\text{-}17}$	–	5,0	–	V
Hue control						
Control voltage range				see Fig. 5		
Input current	for $V_{15\text{-}17} < 5$ V	I_{14}	–	0,5	20	μA
Input impedance	for $V_{15\text{-}17} > 5$ V	$\lvert Z_{14\text{-}17} \rvert$	1,5	2,5	3,5	kΩ
Demodulation part						
Ratio of demodulation signals (measured at the various outputs)	note 7					
(R-Y)/(B-Y); no (R-Y) signal		$\frac{V_{10\text{-}17}}{V_{12\text{-}17}}$	–	–0,42	–	
(R-Y)/(B-Y); colour bar signal		$\frac{V_{10\text{-}17}}{V_{12\text{-}17}}$	–	1,4	–	
(G-Y)/(R-Y); no (B-Y) signal		$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	–0,25	–	
(G-Y)/(B-Y); no (R-Y) signal		$\frac{V_{11\text{-}17}}{V_{12\text{-}17}}$	–	–0,11	–	
Frequency response	0 to 0,7 MHz		–	–	–3	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RGB matrix and amplifier						
Output signal amplitude	at nominal luminance input signal and nominal contrast (peak-to-peak value) note 3 black-white	$V_{10,11,12-17(p-p)}$	4,0	5,0	6,0	V
Output signal amplitude of the "blue" channel	at nominal contrast and saturation control setting and no luminance signal to the input (B-Y) signal (peak-to-peak value)	$V_{12-17(p-p)}$	–	3,8	–	V
Maximum peak-white level	note 6	$V_{10,11,12-7}$	9,0	9,3	9,6	V
Maximum output current		$I_{10,11,12-17}$	–	–	10	mA
Difference in the black level between the three channels			–	–	600	mV
Black level shift with vision content			–	10	40	mV
Brightness control voltage range			see Fig. 4			
Brightness control input current		I_9	–	–	–50	μA
Black level variation with temperature		V/T	–	0,15	1,0	mV/K
Black level variation with contrast control		ΔV	–	75	200	mV
Relative spread between the three output signals			–	–	10	%
Relative variation in black level between the three channels	during variations of contrast (10 dB), brightness (± 1 V), and supply voltage (± 10%)	ΔV	–	0	20	mV
Differential drift of black level over a temperature range of 40 °C		ΔV	–	0	20	mV
Blanking level at the RGB outputs		V_{b1}	1,95	2,15	2,35	V

parameter	conditions	symbol	min.	typ.	max.	unit
Tracking of output black levels with supply voltage		$\frac{\Delta V_{b1}}{V_{b1}} \times \frac{V_P}{\Delta V_P}$	1,0	1,05	1,1	
Signal-to-noise ratio of output signals	note 5	S/N	62	–	–	dB
Residual 3,58 MHz in RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	–	50	75	mV
Residual 7,1 MHz and higher harmonics in the RGB outputs (peak-to-peak value)		$V_{R(p-p)}$	–	50	75	mV
RGB output impedance		$\lvert Z_{10,11,12-17} \rvert$	–	–	50	
Frequency response of total luminance and RGB amplifier circuits	0 to 5 MHz		–	–	–3	dB
Sandcastle input						
Level at which the RGB blanking is activated		V_{7-17}	1,0	1,5	2,0	V
Level at which burst gate clamping pulses are separated		V_{7-17}	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse		t_d	300	375	450	ns
Input currents	V_{7-17} = 0 to 1 V	I_7	–	–	–1	mA
	V_{7-17} = 1 to 8,5 V	I_7	–	–20	–40	μA
	V_{7-17} = 8,5 to 12 V	I_7	–	–	2	mA

Noted to the characteristics

1. Signal with negative going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for colour bar with 75% saturation, so the chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as maximum contrast –3 dB and nominal saturation as maximum saturation –10 dB.
4. Cross coupling is measured under the following condition:
   - input signals nominal;
   - contrast and saturation such that nominal output signals are obtained;
   - the signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is specified as peak-to-peak signal with respect to RMS noise.
6. When this level is exceeded the amplifier of the output signal is reduced via a discharge of the capacitor on pin 7 (contrast control). Discharge current is 5,5 mA.
7. These matrixed values are found by measuring the ratio of the various output signals. The values are derived from the matrix equations given in the section 'FUNCTIONAL DESCRIPTION'.

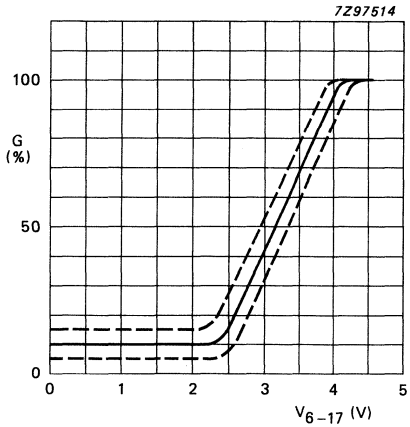


Fig. 2 Contrast control voltage range.

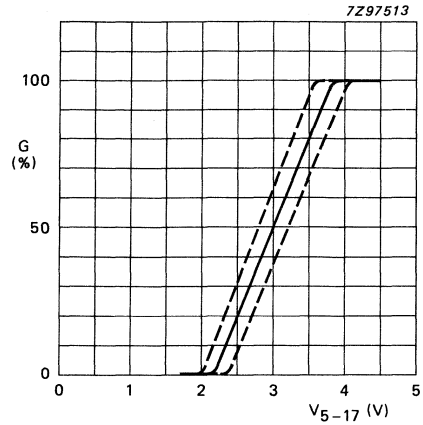


Fig. 3 Saturation control voltage range.

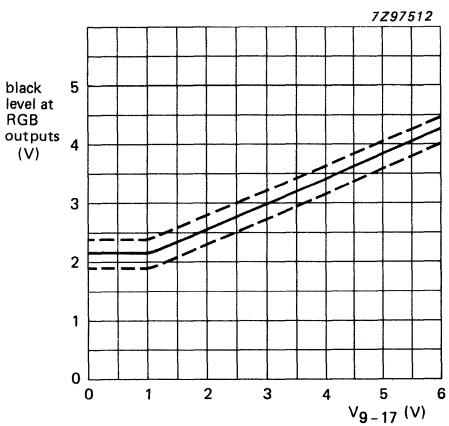


Fig. 4 Brightness control voltage range.

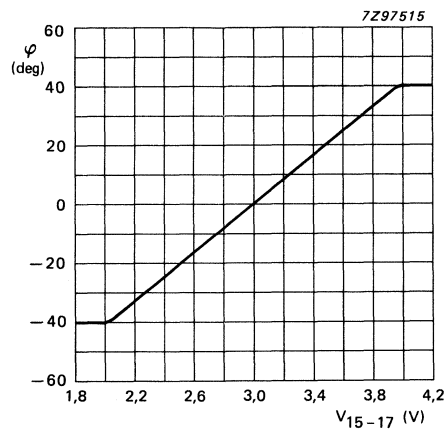


Fig. 5 Hue control voltage range.

APPLICATION INFORMATION

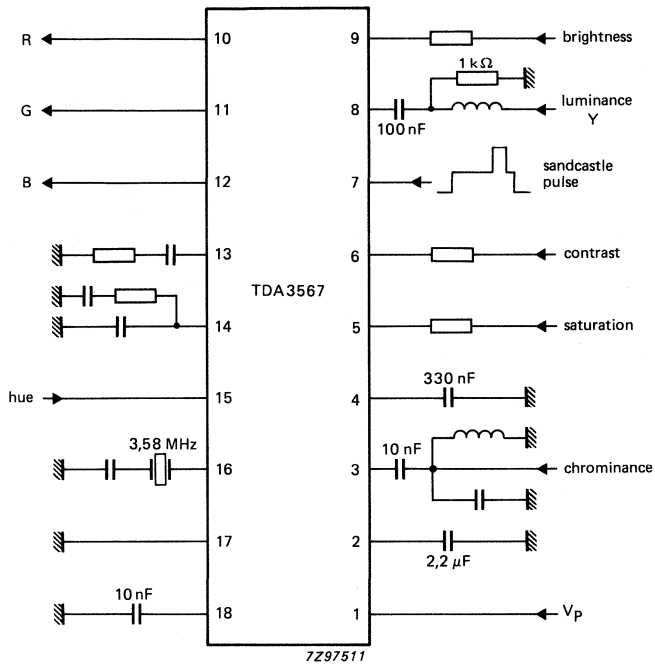


Fig. 6 Application diagram.

NTSC Decoder with fast RGB blanking

TDA3569B

GENERAL DESCRIPTION

The TDA3569B is a monolithic integrated decoder for the NTSC colour television standard. It combines all functions required for the identification and demodulation of NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of discrete output stages.

FEATURES

- Automatic chrominance levelling (avoids saturation at the chrominance input)
- Peaking circuit with DC control
- Fast RGB output blanking

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)		10.8	12	13.2	V
I_P	supply current (pin 1)		-	90	-	mA
Luminance input signal						
$V_{8\text{-}19\ (p\text{-}p)}$	input voltage (peak-to-peak value)		-	450	-	mV
-	contrast control range		-	−17 to +3	-	dB
Chrominance amplifier						
$V_{3\text{-}19\ (p\text{-}p)}$	input voltage (peak-to-peak value)		-	550	-	mV
-	saturation control range		50	-	-	dB
RGB matrix and amplifiers						
$V_{12,\ 13,\ 14\text{-}19\ (p\text{-}p)}$	output voltage (peak-to-peak value)	note 1	4	5	6	V
Sandcastle input						
$V_{7\text{-}19}$	slicing level for RGB blanking		1.0	1.5	2.0	V
$V_{7\text{-}19}$	burst gate/clamping pulse separation level		6.5	7.0	7.5	V

Note to the quick reference data

1. With nominal luminance and nominal contrast (black-white)

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3569B	20	DIL	plastic	SOT146

NTSC Decoder with fast RGB blanking

TDA3569B

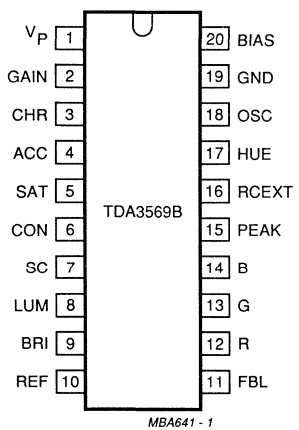


Fig.1 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
GAIN	2	peak detector gain control input
CHR	3	chrominance input
ACC	4	ACC control input
SAT	5	saturation control input
CON	6	contrast control input
SC	7	sandcastle input
LUM	8	luminance input
BRI	9	brightness control input
REF	10	setting of luminance overshoot level
FBL	11	fast blanking input
RED	12	red output
GRN	13	green output
BLUE	14	blue output
PEAK	15	control input (DC) for luminance overshoot
RCEXT	16	phase detection network
HUE	17	hue control input
OSC	18	oscillator frequency input
GND	19	ground
BIAS	20	bias capacitor input

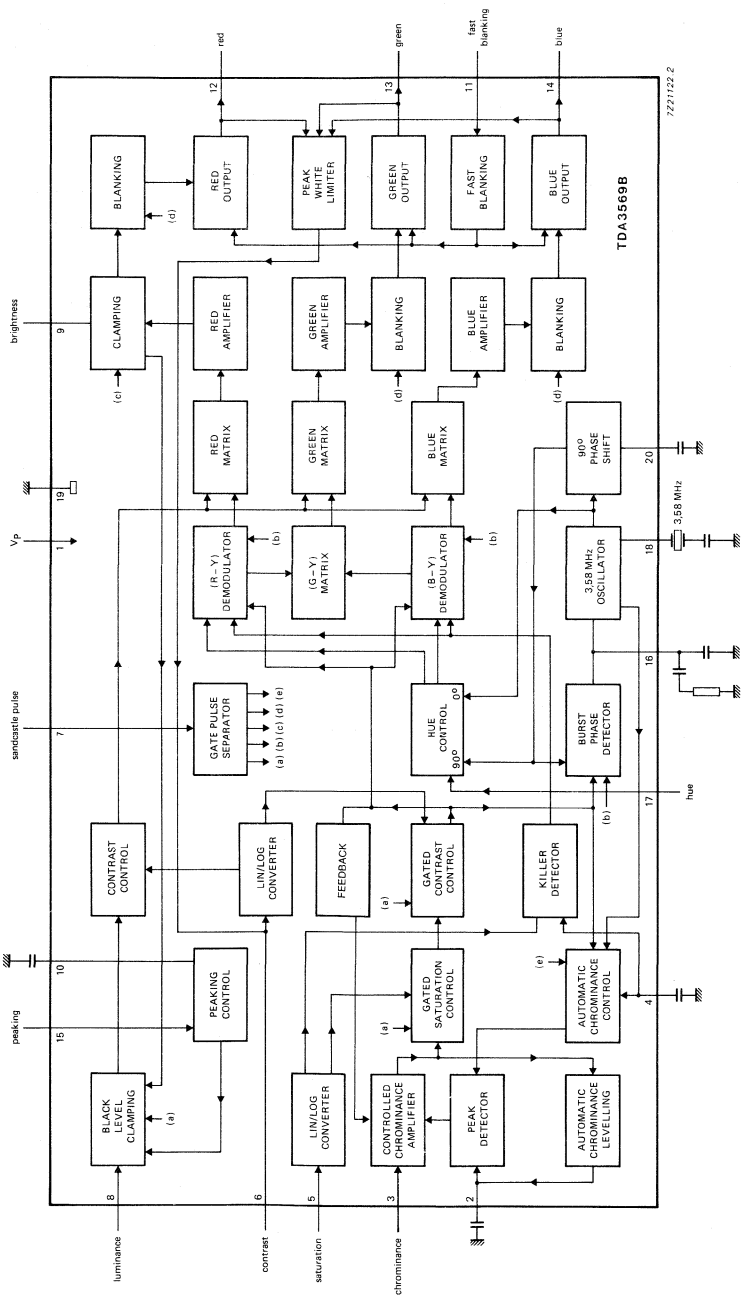


Fig.2 Block diagram.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The input signal must be AC coupled to the input (pin 8). The coupling capacitor provides storage for the black level clamp circuit of the RGB amplifiers . After clamping the signal is fed to a peaking stage. The DC voltage network connected to pin 15 is used to define the amount of overshoot. The peaking stage is followed by a contrast control stage. The control voltage has to be supplied to pin 6. The control voltage range is nominally −17 to +3 dB. The linear curve of the contrast control voltage is shown in Fig.3.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal at pin 3 must be AC coupled. The minimum input signal must have an amplitude of 55 mV peak-to-peak (colour bar signal with 75% saturation, so with a burst signal of 25 mV peak-to-peak). The gain control stage has a control range in excess of 30 dB, the maximum input signal should not exceed 1.1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the automatic chrominance levelling circuit (ACL) which avoids heavy over saturation when the chrominance/burst ratio exceeds a level of 2.9 : 1. The ACL circuit controls the chrominance signal amplitude via the automatic chrominance control (ACC) circuit. The controlled chrominance signal is then fed to the saturation and contrast control stages. Chrominance and luminance control stages are directly coupled to obtain good tracking. The saturation is linearly controlled via pin 5. The control voltage range is 2 V to 4 V, the input impedance is high. The saturation control range is in excess of 50 dB. The burst signal is not affected by contrast or saturation control. After the amplification and control stages the chrominance signal is internally fed to the (R-Y) and (B-Y) demodulators, burst phase and ACC detectors.

Oscillator and ACC circuit

The 3.58 MHz reference oscillator operates at the subcarrier frequency. The crystal must be connected between pin 18 and ground (pin 19). The oscillator does not require adjustment due to the small spreads of the IC. To check the free running frequency of the oscillator the loop is opened by connecting the saturation control (pin 5) to the positive supply line. The oscillator has an internal gain -limiting stage which holds the gain at unity. This ensures internal signals remain sinusoidal thus preventing higher harmonics of the subcarrier signal and allowing hue control obtained by mixing two signals with a phase of 0° and 90°. The 90° phase-shifted signal is provided by a miller integrator (biased by pin 20). The ACC detector compares the burst signal with the 0° reference signal. The detected burst signal is then amplified and fed to a peak detector for ACC and to a sample and hold circuit which drives the colour killer circuit. The reference signal for the burst phase detector is provided by the 90° phase shifted signal. An RC network is used to obtain the required catching range and noise immunity for the output voltage of the burst phase detector. The hue control is obtained by mixing oscillator signals with a phase of 0° and 90° before they are fed to the (R-Y) and (B-Y) demodulators. As the hue control is independent of the PLL, the control will react without time delay on the control voltage changes.

Demodulator circuits

The demodulators are driven by the amplified and controlled chrominance signals, the reference signals are obtained from the hue control circuit. In nominal hue control position the phase angle of (R-Y) reference signal is 90°, the phase angle of the (B-Y) reference signal is 0°. For flesh tone corrections the demodulated (R-Y) signal is matrixed with the demodulated (B-Y) signal according to the following equations:

$$(R\text{-}Y)_{matrixed} = 1.29\ (R\text{-}Y)_{IN} - 0.29\ (B\text{-}Y)_{IN}$$

$$(G\text{-}Y)_{matrixed} = -0.50\ (R\text{-}Y)_{IN} - 0.10\ (B\text{-}Y)_{IN}$$

$$(B\text{-}Y)_{matrixed} = (B\text{-}Y)_{IN}$$

In these equations $(R\text{-}Y)_{IN}$ and $(B\text{-}Y)_{IN}$ indicate the colour difference signal amplitudes when the chrominance signal is demodulated with a phase difference between the R-Y and B-Y demodulator of 90° and a gain ratio B-Y/R-Y = 1.78.

RGB matrix circuit and amplifiers

The three matrix and amplifier circuits are identical. The luminance signal and the colour difference signals are added in the matrix circuit to obtain the colour signal. Output signals are 5 V (peak-to-peak) (black-white) for the following nominal input signals and control settings.

- Luminance 450 mV (peak-to-peak)

- Chrominance 550 mV (peak-to-peak) (burst-to-chrominance ratio of the input = 1 : 2.2)
- Contrast –4 dB (maximum)
- Saturation –9 dB (maximum)

The maximum available output voltage is approximately 7 V (peak-to-peak). The black level of the red channel is compared with a variable external reference level (pin 9), which provides the brightness control. The control loop is closed via the luminance input. The coupling capacitor of pin 8 is used as a storage capacitor for the black level clamp circuit. The luminance input is varied to control the black level control, therefore the green and blue outputs will follow any variation of the red output. The output of the black level control can be varied between 2 V to 4 V. The corresponding brightness control voltage is shown in Fig.5. If the output signal surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB signals

The TDA3569B comprises two blanking facilities. The RGB signals can be blanked via the sandcastle input (pin 7). In addition to the normal flyback blanking (via pin 7), the RGB signals at the outputs can be blanked also via the fast blanking input pin 11 (with a typical delay of 40 ns). A slicing level of about 1 5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated form the rest of the pulse. During blanking, a level of +2.15 V (typical) is available at the output.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	-	13.2	V
P_{tot}	total power dissipation	-	1700	mW
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	–25	+65	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient	50	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; all voltages referenced to pin 19; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 1)						
V_P	supply voltage		10.8	12	13.2	V
I_P	supply current		-	90	-	mA
P_{tot}	total power dissipation		-	1.08	-	W
Luminance amplifier (pin 8)						
$V_{8\ (p-p)}$	input voltage (peak-to-peak value)	note 1	-	450	-	mV
V_8	input level before clipping		-	-	1.0	V
I_8	input current		-	0.15	1.0	µA
-	contrast control range	see Fig.3	-	−17 to +3	-	dB
I_6	input current contrast control	V_6 < 6 V	-	0.5	15	µA
I_6	input current contrast control	V_6 = 2.5 V; note 2	3	7	-	mA
Peaking of luminance signal						
$\lvert Z_{15} \rvert$	input impedance (pin 15)		7	10	13	kΩ
$\lvert Z_{10} \rvert$	output impedance (pin 10)		50	75	90	Ω
-	luminance gain ratio	note 3	-	10	-	
-	control voltage for peaking adjustment (pin 15)	see Fig.7	-	-	-	
Chrominance amplifier (pin 3)						
$V_{3\ (p-p)}$	input signal amplitude (peak-to-peak value)	note 4	-	550	-	mV
$V_{3\ (p-p)}$	input signal amplitude (peak-to-peak value)	note 5	-	-	1100	mV
-	minimum burst signal amplitude within the ACC control range (peak-to-peak value)		35	-	-	mV
ΔV_{12}	change of red output signal over 30 dB ACC control range		-	-	2	dB
$\lvert Z_3 \rvert$	input impedance (pin 3)		6	9	12	kΩ
C_3	input capacitance		-	4	6	pF
-	saturation control range	see Fig.4	50	-	-	dB
I_5	saturation control input current (pin 5)	V_5 < 6 V	-	1	20	µA
$\lvert Z_5 \rvert$	input impedance (pin 5)	V_5 = 6 to 10 V	1.5	2.1	2.7	kΩ
$\lvert Z_5 \rvert$	input impedance (pin 5)	colour killer active	1.5	2.1	2.7	kΩ
-	tracking between luminance and chrominance contrast control	for 10 dB of control	-	1	2	dB
ACL circuit						
-	chrominance/burst ratio at which ACL commences	note 6	-	2.9	-	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference part; note 7						
PHASE-LOCKED LOOP						
Δf	phase-locked-loop catching range		±300	±400	-	Hz
$\Delta\varphi$	phase shift for 400 Hz deviation of f_{osc}		-	-	5	deg
OSCILLATOR; SEE NOTE 7						
TC_{osc}	oscillator temperature coefficient of oscillator frequency		-	−1.5	−2.5	Hz/K
Δf_{osc}	frequency deviation	$\Delta V_p = \pm 10\%$	-	150	250	Hz
R_{18}	input resistance (pin 18)		1	1.4	1.8	kΩ
C_{18}	input capacitance (pin 18)		-	-	10	pF
ACC GENERATION (PIN 4)						
V_4	control voltage at nominal input signal		-	5.2	-	V
V_4	control voltage without burst input		-	2	-	V
V_4	colour-off voltage		-	2.6	-	V
ΔV_4	Δcolour-on/-off voltage		100	300	500	mV
V_2	control voltage at nominal input signal (pin 2)		-	5.2	-	V
HUE CONTROL						
-	control voltage range	see Fig.6	-	-	-	
I_{17}	input current (pin 17)	$V_{17} < 5$ V	-	0.5	20	µA
$\lvert Z_{17} \rvert$	input impedance (pin 17)	$V_{15} > 5$ V	1.5	2.5	3.5	kΩ
Demodulator part; ratio of demodulated signals ± 25%; note 8						
$\frac{V_{12}}{V_{14}}$	(R-Y)/(B-Y)	no (R-Y) signal	-	−0.29	-	
$\frac{V_{13}}{V_{12}}$	(G-Y)/(R-Y)	no (B-Y) signal	-	−0.39	-	
$\frac{V_{13}}{V_{14}}$	(G-Y)/(B-Y)	no (R-Y) signal	-	−0.10	-	
α_{17}	frequency response between 0 and 0.7 MHz		-	-	−3	dB
RGB matrix and amplifiers						
$V_{12, 13, 14(p-p)}$	output signal amplitude(peak-to-peak value)	note 9	4.0	5.0	6.0	V
$V_{14(p-p)}$	output signal amplitude of the "blue" channel (B-Y) at pin 14 (peak-to-peak value)	note 10	-	3.8	-	V
$V_{12, 13, 14\ (m)}$	maximum peak-white level	note 11	9.0	9.3	9.6	V
$I_{12, 13, 14}$	available output current (pins 12, 13, 14)		10	-	-	mA
$\Delta V_{12, 13, 14}$	difference in black level between the three channels		-	-	600	mV
-	brightness control voltage range	see Fig.5	-	-	-	
$-I_9$	brightness control input current		-	-	−50	µA
$\Delta V/\Delta T$	variation of black level with temperature		-	0.15	1.0	mV/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB matrix and amplifiers						
ΔV	variation of black level with contrast	note 12	-	75	200	mV
-	relative spread between the R, G, and B output signals (black-white)		-	-	10	%
-	relative black-level variation between the three channels during variation of contrast	note 13	-	-	20	mV
-	relative black-level variation between the three channels during variation of brightness	note 14	-	-	20	mV
V_{blk}	blanking level at the RGB outputs		1.95	2.15	2.35	V
ΔV	differential drift of the blanking levels over a temperature range of 40 °C		-	0	20	mV
$\frac{DV_{bl}}{V_{bl}} x \frac{V_P}{DV_P}$	tracking of output black level with supply voltage		1.0	1.05	1.1	
S/N	signal-to-noise ratio of output signals	note 15	62	-	-	dB
$V_{R\ (p-p)}$	residual 3.58 MHz signal at RGB outputs (peak-to-peak value)		-	50	75	mV
$V_{R\ (p-p)}$	residual 7.1 MHz signal at the RGB outputs (peak-to-peak value)		-	50	75	mV
$\lvert Z_{10} \rvert$	output impedance		-	-	50	Ω
$\lvert Z_{11} \rvert$	output impedance		-	-	50	Ω
$\lvert Z_{12} \rvert$	output impedance		-	-	50	Ω
α	frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz	note 16	-	-	–3	dB
Sandcastle input						
V_7	level at which the RGB blanking is activated		1	1.5	2	V
V_7	level at which the burst gate clamping pulses are separated		6.5	7	7.5	V
t_d	delay between black level clamping and burst gating pulse		300	375	450	ns
$-I_7$	input current at V_7 = 0 to 0.8 V		-	-	–1	mA
I_7	input current at V_7 = 1 to 8 V		-	-	–40	µA
I_7	input current at V_7 = 8.5 to 12 V		-	-	2	mA
Fast blanking						
V_{11}	level at which the fast blanking is activated (pin 11)		3.5	-	-	V
V_{11}	allowable voltage at blanking input		-	-	5	V
t_d	delay between fast blanking input and output		-	40	-	ns
I_{11}	input current	V_{11} = 3.5 V	-	160	-	µA
-	difference between normal black-level and the fast blanking black-level		-	–0.9	-	V

Notes to the characteristics

1. Signal with negative going sync; amplitude includes sync. pulse amplitude.
2. Peak white limiter active.
3. Pin 10 AC short-circuit to ground.
4. Indicated is a signal for colour bar with 75% saturation, so the chrominance to burst ratio is 2.2 : 1.
5. Before clipping occurs in the input stage.
6. The ACL circuit limits the chrominance amplitude to a particular value as soon as the chrominance/burst ratio exceeds 2.9 : to 1. The limiting is performed via the ACC function.
7. All frequency variations are referenced to the 3.58 MHz carrier frequency.
8. These matrixed values are found when hue is in a normal condition and by measuring the ratio of the various output signals. The values are derived from the matrix equations given in the section 'FUNCTIONAL DESCRIPTION'..
9. With nominal luminance and contrast (black-to-white), nominal contrast is specified as maximum contrast –4 dB and nominal saturation as maximum saturation –9 dB.
10. With nominal contrast, saturation and hue, no luminance input.
11. When this level is exceeded the amplifier of the output signal is reduced via a discharge of the capacitor on pin 6 (contrast control). Discharge current is 7 mA.
12. Control range: nominal –10dB.
13. During variations of contrast (10 dB) at nominal saturation.
14. During variations of brightness (± 1 V) at nominal controls.
15. The signal-to-noise ratio is specified as peak-to-peak signal with respect to RMS noise. The effective bandwidth is 5 MHz.
16. Disconnected peaking capacitor.

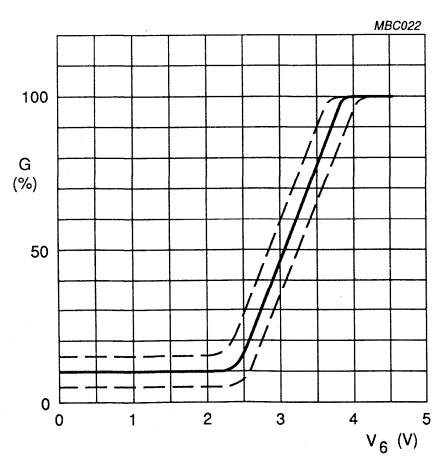


Fig.3 Contrast control voltage range.

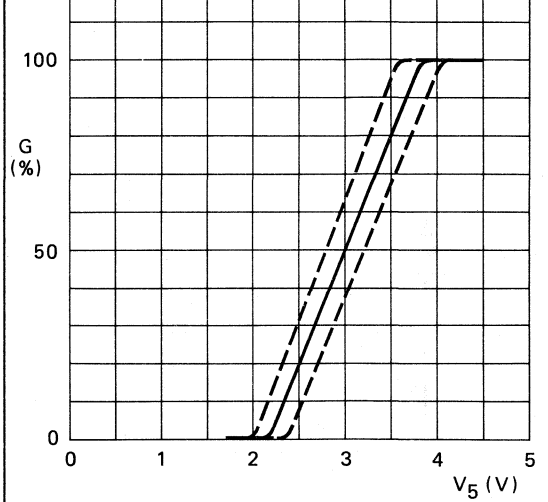


Fig.4 Saturation control voltage range.

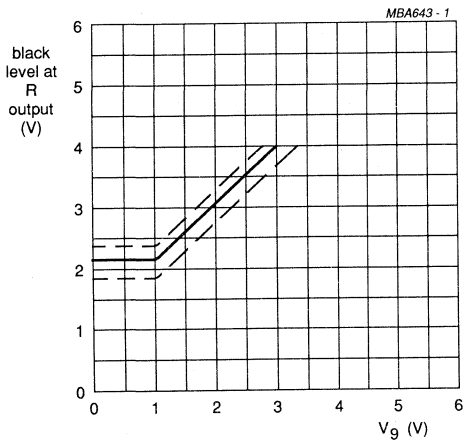


Fig.5 Brightness control range.

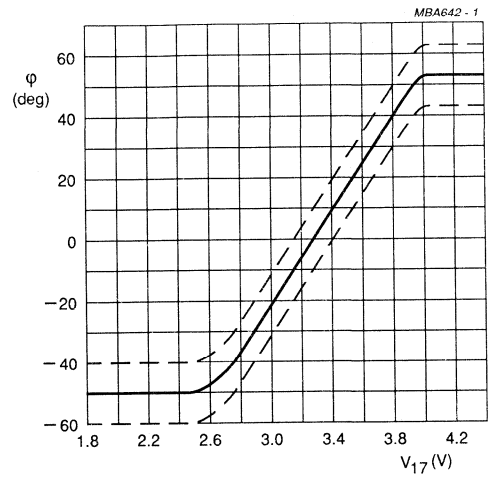


Fig.6 Hue control voltage range.

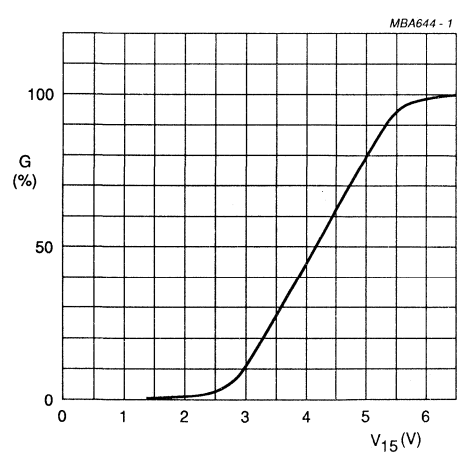


Fig.7 Peaking control voltage range.

APPLICATION DIAGRAM

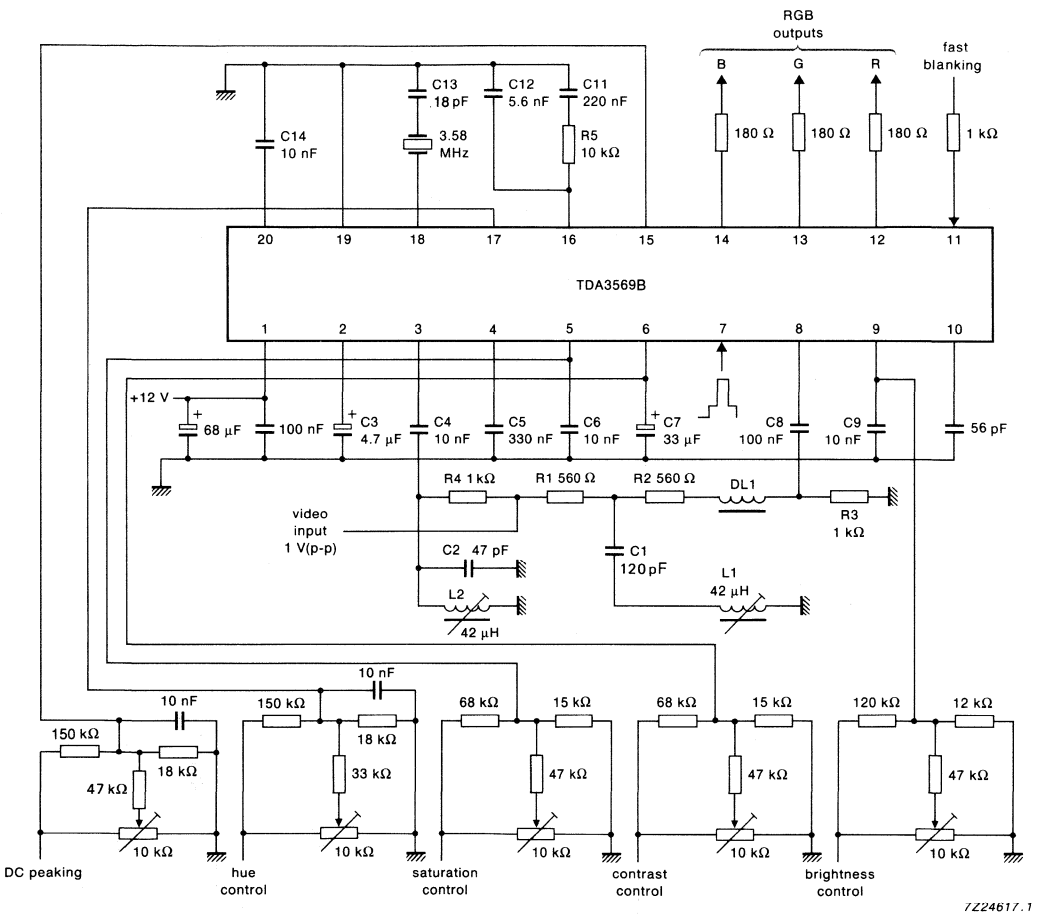


Fig.8 Application diagram.

SECAM PROCESSOR CIRCUIT

GENERAL DESCRIPTION

The TDA3590A processor circuit converts SECAM signals into sequential phase-modulated (quasi-PAL) signals. It combines all the functions of the TDA3590, TDA3591 and TDA3591A to provide a complete SECAM processor system. The circuit is intended for use in conjunction with TDA3560, TDA3561, TDA3561A, TDA3562A or TDA3566 to provide SECAM/PAL/NTSC/black-and-white processor combinations.

Features

- Limiter/amplifier for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Modulator to convert colour difference signals into sequential, phase-modulated signals
- Identification circuit for horizontal, vertical or combined horizontal and vertical SECAM identification
- Divider circuit to provide 4,4 MHz carrier from 8,8 MHz signals generated in TDA3560/61/61A/62A/66
- Sandcastle pulse detector
- SECAM switch and PAL matrix
- Video amplifier
- Pin compatibility with TDA3590, TDA3591 and TDA3591A when application requires SECAM ident priority (does not apply with PAL ident priority)

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{17-2}$	typ.	12 V
Supply current	$I_P = I_{17}$	typ.	100 mA
Chrominance amplifier and demodulator			
Input signal PAL (peak-to-peak value)	$V_{4-2(p-p)}$	typ.	550 mV
Input signal SECAM (peak-to-peak value)	$V_{4-2(p-p)}$	typ.	100 mV
Output signal PAL (peak-to-peak value) at $V_{16(p-p)} = 1,2$ V	$V_{8-2(p-p)}$	typ.	900 mV
Output signal SECAM (peak-to-peak value)	$V_{8-2(p-p)}$	typ.	500 mV
Identification			
Input voltage range for horizontal identification (pin 5)	V_{5-2}		0 to 8 V
Input voltage range for vertical identification (pin 5)	V_{5-2}		10,5 to 12,0 V
Voltage at pin 6 for PAL	V_{6-2}	typ.	10,2 V
Voltage at pin 6 for SECAM	V_{6-2}	typ.	7,0 V
Sandcastle pulse detector			
Vertical blanking level	V_{19-2}	typ.	1,5 V
Horizontal blanking level	V_{19-2}	typ.	3,5 V
Burst gating level	V_{19-2}	typ.	7,2 V
Luminance amplifier			
Luminance input signal (peak-to-peak value)	$V_{16-2(p-p)}$	typ.	1,2 V
Luminance output signal (peak-to-peak value)	$V_{15-2(p-p)}$	typ.	3,0 V
PAL matrix and SECAM switch			
Burst signal amplitude (peak-to-peak value)	$V_{11;12-2(p-p)}$	typ.	60 mV
Amplification for PAL		typ.	0,5 dB
Amplification for SECAM		typ.	6 dB

PACKAGE OUTLINE

24-lead DIL; plastic (with internal heat spreader) (SOT101B).

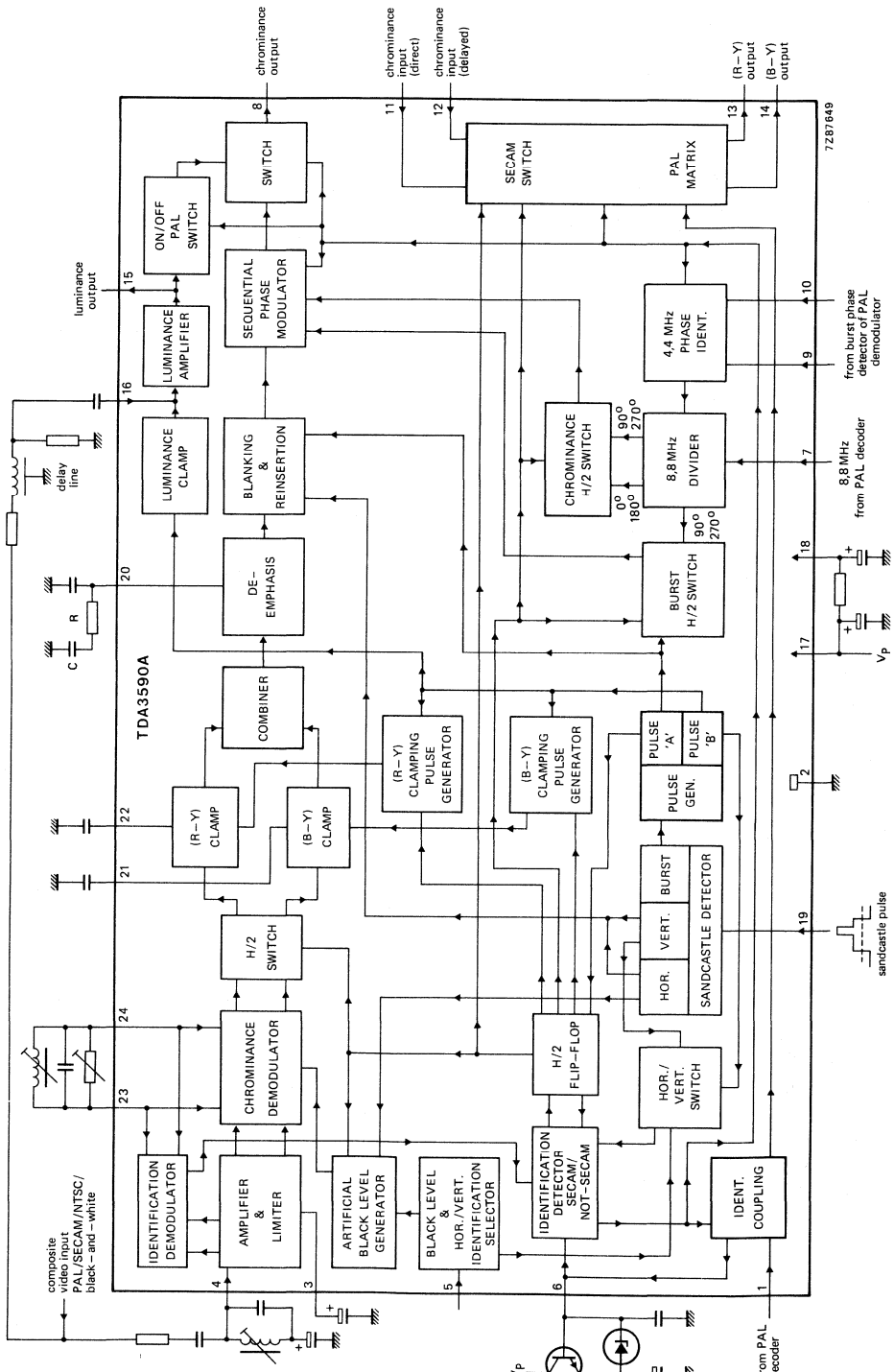


Fig. 1 Block diagram.

PINNING

1. Identification coupling input for PAL/not-PAL identification using half the saturation voltage of the PAL decoder.
2. Ground.
3. Limiter feedback.
4. SECAM video input.
5. Identification selection input using a d.c. level to preset the identification mode of horizontal/vertical detection + black level clamping/insertion.
6. Storage circuit input to SECAM/not-SECAM identification detector.
7. Divider circuit input of 8,8 MHz from the PAL decoder.
8. Chrominance signal output comprising PAL or processed SECAM (quasi-PAL).
9. Carrier signal phase identification input from the burst phase detector of the PAL decoder.
10. As for pin 9.
11. Direct chrominance input to SECAM switch/PAL matrix.
12. Delayed chrominance input to SECAM switch/PAL matrix.
13. Colour difference output (R-Y).
14. Colour difference output (B-Y).
15. Luminance output.
16. Luminance/PAL input.
17. Positive supply voltage (V_P).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input.
20. De-emphasis circuit connection.
21. Storage capacitor connection for (B-Y) clamp.
22. Storage capacitor connection for (R-Y) clamp.
23. Connection for reference tuned circuit for SECAM chrominance and identification demodulators.
24. As for pin 23.

FUNCTIONAL DESCRIPTION

Demodulation

The chrominance and identification demodulators of the TDA3590A both share the same reference tuned circuit (pins 23 and 24). The identification circuit automatically detects whether the incoming signal is SECAM or not-SECAM.

When the incoming signals are not-SECAM (PAL/NTSC/black-and-white) they are diverted via pin 16 to the chrominance output at pin 8 and no signal demodulation takes place. The delay line connected to pin 16 delays the signals to equalize the delay of the SECAM processor circuitry. When SECAM signals are received the PAL signal path is switched off.

Incoming SECAM signals are applied to pin 4 via an external bell filter. The signals are amplified, limited and then demodulated. The limiters give optimum i.f. interference suppression. Only one demodulator is necessary as the colour difference signals are available sequentially. After demodulation the colour difference signals are separated by an H/2 switch and then applied to (R-Y) and (B-Y) clamp circuits where the black levels are clamped to the same d.c. level. The optimum black level can be obtained at the end of the horizontal burst, so the timing of the (R-Y) and (B-Y) clamp is determined by the last 1,45 μs of the burst gate pulse.

The two colour difference signals are combined again after clamping and then applied to the modulator via de-emphasis, blanking and reinsertion circuits.

The ratio of (R-Y) to (B-Y) at the de-emphasis output (pin 20) is 1,78. The external de-emphasis components of R = 1 kΩ and C = 470 pF give a spread at the internal de-emphasis network $< 20\%$.

FUNCTIONAL DESCRIPTION (continued)

If artificial black level reinsertion is required the burst gating pulse (Fig. 2) is used to time black level clamping. Artificial black levels are inserted during the horizontal blanking period when $V_{5\text{-}2} > 2$ V. The clamp circuits then react to the artificial levels instead of the demodulated burst signals (this is necessary when no horizontal burst signals are available). The inserted signals may not be identical to the demodulated signals because of circuitry spread but this can be corrected by detuning the demodulator reference tuned circuit.

Modulation

A burst signal is reinserted into the combined SECAM signal at the input to the sequential phase modulator. The nominal duration of this burst is 2,85 μs which approximates to the duration of the PAL burst and, in combination with the horizontal blanking pulse (used as keying pulse in the SECAM switch), minimizes interference in the a.c.c. loop of the TDA3560/61/62.

At the input to the modulator the (R-Y) and (B-Y) signals have a positive phase position for magenta colour. The modulation carriers for the (R-Y) and (B-Y) signals are 90° out of phase; the burst is modulated in the + (R-Y) direction and is only present during an (R-Y) line, the modulated (R-Y) component has the same phase position as the (R-Y) burst for magenta colour.

The chrominance output from pin 8, in the SECAM mode, is a quasi-PAL signal with alternate line, sequential modulation. Odd and even harmonics of the 4,4 MHz carrier introduced by the modulator are suppressed by internal filters. A correction is made to the burst-chrominance ratio of the quasi-PAL signals for equal saturation of PAL and SECAM signals.

Identification

Identification of the SECAM signal is performed using the fact that only SECAM has a line-to-line difference in demodulated voltage level. This is detected during the last 1,5 μs of the burst gate pulse. A flip-flop, which is switched by the leading edge of the sandcastle time blanking pulse, provides the reference input to the identification detector. Here the phase of the flip-flop is compared with that of the changing voltage levels from the demodulator. The SECAM identification circuits operate when selected by the voltage on pin 5; this may be horizontal, vertical or combined horizontal and vertical identification, depending on the switching arrangements of pin 5. An internal voltage divider presets pin 5 to 6 V to give automatic selection of horizontal identification plus black level re-insertion. Vertical identification is selected by taking the voltage on pin 5 above 10,5 V, then the system compares the demodulator output voltage only during line scanning of the vertical blanking.

Information obtained from the identification detector is also used for colour killing and, if required, for switching to PAL.

Luminance amplification

The luminance amplifier input at pin 16 can be up to 1,2 V (peak-to-peak value) which equates to a peak-to-peak voltage of 2,7 V −7 dB. The amplifier gain is typically 8 dB. The luminance clamping circuit is activated during the SECAM identification timing (see Fig. 2).

Sandcastle pulse detection

The sandcastle pulse detector requires a three-level sandcastle pulse to provide horizontal blanking, vertical blanking and burst gate pulses. The detected burst gate pulse triggers a pulse generator which produces two timing pulses, pulse 'A' and pulse 'B' (see Fig. 2). Pulse 'A' is used to time the PAL burst modulator. Pulse 'B' provides the timing of the (R-Y) clamp (present only during a red line); the (B-Y) clamp (present only during a blue line); the luminance clamp (present every line); and the SECAM horizontal identification circuit.

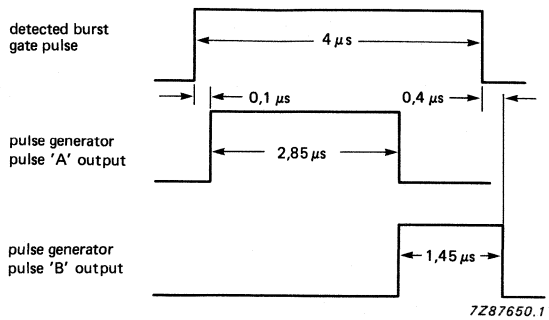


Fig. 2 Burst gate timing pulse generation.

PAL matrix and SECAM switch

The PAL matrix and SECAM switch is included in the TDA3590A to facilitate handling of the two chrominance signal types, PAL and SECAM. For PAL, the direct chrominance signal and the chrominance signal delayed by the PAL delay line are used by the PAL matrix to separate the two colour difference signals. Phase accuracy is not critical for this operation as the colour difference signals are not mixed. For SECAM, the quasi-PAL sequential colour difference signals are separated by switching. The gain of the switching circuit is two times that for normal PAL reception to maintain signal balance between the two systems. The (B-Y) output from the SECAM switch is a signal with no burst; the (R-Y) output has a burst modulated in the + (R-Y) direction during the + (R-Y) line. There is minimal crosstalk between the colour difference signals in the SECAM switch.

Carrier generation

The carrier for the sequential phase modulator is obtained using the 8,8 MHz input from the PAL decoder. This input is divided by two to provide two 4,4 MHz signals with a phase relationship of 90°. Correct phasing between the 4,4 MHz and the PAL decoder is ensured by the 4,4 MHz phase identifier circuit which resets the divider if the phasing is wrong (see Figs 3 and 4 for inter-connections). The inputs/outputs to the phase identifier have internal current sources in the case of SECAM.

Coupling of identification systems

Coupling of system identification between TDA3590A and a PAL decoder is performed using the functions of pins 1 and 6. The voltage level at pin 1 is controlled by the PAL/not-PAL detection of the PAL decoder; the voltage level at pin 6 is a function of SECAM/not-SECAM detection of the TDA3590A modified by the action of pin 6 external circuit.

The circuit action is as follows and is summarized in Table 1.

Channel switching — During channel switching pin 6 is taken rapidly to a high voltage (± 10,2 V) by the external circuit. This corresponds to the not-SECAM mode of the TDA3590A.

PAL — The high voltage level at pin 6 caused by channel switching is maintained by the TDA3590A when it recognizes the signal as not-SECAM. An internal current source keeps pin 6 voltage high, locking the TDA3590A in the not-SECAM mode. This condition is maintained even if reflected PAL signals are present. The PAL decoder recognizes the signal as PAL and takes pin 1 of TDA3590A to a voltage of between 0,5 and 2,6 V, depending on the setting of the saturation voltage. The system is thus locked in the PAL mode.

FUNCTIONAL DESCRIPTION (continued)

SECAM

The initial high voltage level (± 10,2 V) at pin 6 caused by channel switching sets the TDA3590A in the not-SECAM mode and during this time the PAL decoder detects a not-PAL signal. This causes a voltage at pin 1 of $< 0,4$ V which prevents the internal current source of TDA3590A maintaining the high voltage level of pin 6 which, in turn, allows the TDA3590A to detect SECAM. The initiation of SECAM detection is delayed by the action of pin 6 external circuit and commences when pin 6 approaches 9,1 V. The SECAM signals are converted by TDA3590A to quasi-PAL signals at pin 8 which are detected by the PAL decoder as PAL signals. The resulting modes of operation are SECAM for the TDA3590A and PAL for the PAL decoder, together giving a system operation in the SECAM mode.

Black-and-white

The TDA3590A is initially set in the not-SECAM mode as previously described. The PAL decoder detects not-PAL and the TDA3590A detects not-SECAM which results in a system operation in the colour-killing mode.

Table 1 System operating modes

TDA3590A mode	PAL decoder mode	system operating mode
SECAM	PAL	SECAM
SECAM	not-PAL	condition not used
not-SECAM	PAL	PAL
not-SECAM	not-PAL	black-and-white

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 17)	$V_P = V_{17-2}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,88 W
Operating ambient temperature range	T_{amb}		−25 to + 65 °C
Storage temperature range	T_{stg}		−25 to + 150 °C

CHARACTERISTICS

$V_P = V_{17-2} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified. The parameter values are valid only when the reference tuned circuit has been aligned as detailed in note 1.

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range (pin 17)	V_{17-2}	10,8	12,0	13,2	V
Supply current (pin 17)	I_{17}	–	100	–	mA
Input current (pin 18)	I_{18}	–	–	170	μA
Total power dissipation	P_{tot}	–	1,2	–	W
Chrominance amplifier and demodulator					
Input signal PAL (peak-to-peak value)	$V_{4-2(p-p)}$	–	–	1,1	V
Input signal SECAM (peak-to-peak value)	$V_{4-2(p-p)}$	15	100	300	mV
Input resistance (pin 4)	R_{4-2}	–	10	–	kΩ
Input capacitance (pin 4)	C_{4-2}	–	–	5	pF
(R-Y)/(B-Y) ratio before modulation (pin 20)		–	1,78	–	
Relative black level deviation of colour difference signals before modulation (note 2)					
Output signal PAL (peak-to-peak value) at $V_{16(p-p)} = 1,2$ V	$V_{8-2(p-p)}$	–	900	–	mV
Output signal SECAM (peak-to-peak value)	$V_{8-2(p-p)}$	–	500	–	mV
Output impedance	$\lvert Z_{8-2} \rvert$	–	50	–	Ω
Input voltage for clamping on back porch of colour difference signals	V_{5-2}	–	–	0,5	V
Input voltage for artificial black level insertion after demodulation	V_{5-2}	2	–	–	V
Input resistance between pins 23 and 24	R_{23-24}	–	4	–	kΩ
Input capacitance between pins 23 and 24	C_{23-24}	–	15	–	pF
Linearity of (B-Y) signal (pin 8) (note 3)		85	92	–	%
Linearity of (R-Y) signal (pin 8) (note 4)		93	100	–	%
Input resistance (pin 5)	R_{5-2}	–	10	–	kΩ
Chrominance demodulator zero point stability (pin 20) (note 5)	f_0	–	5	–	kHz
Offset (B-Y) black level (pin 8) at f_0 clamping; $f_{offset} = 4,4$ MHz		–	−15	–	kHz
Offset (R-Y) black level (pin 8) at f_0 clamping; $f_{offset} = 4,4$ MHz		–	−25	–	kHz

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification SECAM/not-SECAM					
Input voltage range for horizontal identification (pin 5)	V_{5-2}	0	–	8	V
Input voltage range for vertical identification (pin 5)	V_{5-2}	10,5	–	V_P	V
Voltage at pin 6 for PAL	V_{6-2}	–	10,2	–	V
Voltage at pin 6 for SECAM	V_{6-2}	–	7,0	–	V
Identification ON for SECAM	V_{6-2}	–	10,6	–	V
Colour OFF for SECAM	V_{6-2}	–	9,7	–	V
Colour ON for SECAM	V_{6-2}	–	9,0	–	V
Voltage at pins 9 and 10 for SECAM	$V_{9-2;\ 10-12}$	–	10,5	–	V
Voltage between pins 9 and 10 for SECAM	V_{9-10}	–	–	3	mV
Permissible voltage range at pins 9 and 10 for PAL	$V_{9-2;\ 10-2}$	6,8	–	10,2	V
Sandcastle pulse detector and clamping pulse generator					
Voltage level at which the vertical blanking pulse is separated	V_{19-2}	1,0	1,5	2,0	V
required pulse amplitude (peak-to-peak value)	$V_{19-2(p-p)}$	2,1	–	2,9	V
Voltage level at which the horizontal blanking pulse is separated	V_{19-2}	3,0	3,5	4,0	V
required pulse amplitude (peak-to-peak value)	$V_{19-2(p-p)}$	4,1	–	6,6	V
Voltage level at which the burst gating pulse is separated	V_{19-2}	6,7	7,2	7,7	V
required pulse amplitude (peak-to-peak value)	$V_{19-2(p-p)}$	7,8	–	V_P	V
Input current at $V_{19-2} = 7$ V	I_{19}	–	–	40	μA
Carrier generator (note 6)					
Input signal from TDA3560/61/61A/62A/66 (peak-to-peak value)	$V_{7-2(p-p)}$	150	–	–	mV
Input resistance	R_{7-2}	–	4	–	kΩ
Input capacitance	C_{7-2}	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
Luminance amplifier					
Input signal (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	–	1,2	1,7	V
Chrominance input signal when no luminance information is present (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	–	–	1	V
Gain (pin 16 to 15) at f_{16} = 4,4 MHz	$G_{16\text{-}15}$	–	8	–	dB
Input current (pin 16)	I_{16}	–	–	1	μA
Input resistance during clamping (pin 16)	$R_{16\text{-}2}$	–	2,9	–	kΩ
Output impedance (pin 15) at I_{15} = 2 mA	$\lvert Z_{15\text{-}2}\rvert$	–	20	–	Ω
Frequency response at −3 dB (pin 16 to 15)	f	6	–	–	MHz
Gain (pin 16 to 8) at f_{16} = 4,4 MHz; not-SECAM condition	$G_{16\text{-}8}$	–	7	–	dB
Frequency response at −3 dB (pin 16 to 8) not-SECAM condition	f	–	5	–	MHz
PAL matrix and SECAM switch					
Burst signal amplitude (peak-to-peak value)	$V_{11;12(p\text{-}p)}$	–	60	–	mV
Input resistance	$R_{11;12\text{-}2}$	–	900	–	Ω
Input capacitance	$C_{11;12\text{-}2}$	–	3	–	pF
Amplification for PAL	A	–	0,5	–	dB
Amplification for SECAM	A	–	6	–	dB
Difference in amplification from inputs to one output for PAL	ΔA	–	–	0,5	dB
Line-to-line phase error in (R-Y) output for zero error in (B-Y) output for PAL		–	–	3,5	deg
Output impedance	$\lvert Z_{13;14\text{-}2}\rvert$	–	50	–	Ω
Identification PAL/not-PAL					
Input condition for PAL (pin 1)	$V_{1\text{-}2}$	0,8	–	2,1	V
Input conditions for not-PAL (pin 1):					
lower voltage level	$V_{1\text{-}2}$	–	–	$<0,4$	V
upper voltage level	$V_{1\text{-}2}$	$>2,6$	–	V_P	V

Notes to the characteristics

1. The parameter values given in the characteristics are valid only when the following alignment procedure is performed:
   a. Supply a SECAM signal input to pin 4 at 100 mV (peak-to-peak value) without deviation during a red and blue line (SECAM black colour information).
   b. Align the reference tuned circuit so that the output signal from pin 8 to the PAL decoder is minimum during scan (PAL black colour information).
2. When an artificial black level is inserted after demodulation the resulting black level deviation depends on the adjustment of the demodulator tuned circuit. It is therefore possible to obtain a value of 0%.
3. (B-Y) linearity is defined by $V_{out(yellow)}/V_{out(blue)}$ where f_{yellow} = (typ.) 4,02 MHz; f_{blue} = (typ.) 4,48 MHz; $V_{5\text{-}2}$ = 2,0 V.
4. (R-Y) linearity is defined by $V_{out(cyan)}/V_{out(red)}$ where f_{cyan} = (typ.) 4,68 MHz; f_{red} = (typ.) 4,12 MHz; $V_{5\text{-}2}$ = 2,0 V.
5. When the input signal to the limiter (pin 4) changes from 300 to 15 mV (peak-to-peak value) the zero point of the chrominance demodulator shifts by a typical value of 5 kHz.
6. The phase delay between the oscillator output of TDA3560/61/61A/62A/66 and the input to TDA3590A pin 7 must be adjusted for minimum burst amplitude at pin 28 of the PAL decoder.

APPLICATION INFORMATION

The pin-to-pin functions of the application shown in Fig. 3 are described against the corresponding pin numbers.

Pin 4. Chrominance input

Typical input signal values (peak-to-peak) are: SECAM 100 mV; PAL 0,55 V. The input signal, which should be free from any sound modulation, is applied single-ended to pin 4 via a filter which has the bell-shaped bandpass required for SECAM signals.

Pin 5. Horizontal/vertical identification

Selection of horizontal or vertical identification depends on the external voltage applied to pin 5. When the d.c. level on pin 5 changes with time (pulse information) a combination of horizontal and vertical identification is possible.

Horizontal identification

When the voltage at pin 5 is $< 0,5$ V horizontal identification and black level clamping occur. The clamping is during the back porch of the colour difference signals. If artificial black level insertion is required the voltage at pin 5 should be between 2 and 8 V.

Vertical identification

When the voltage on pin 5 is $> 10,5$ V vertical identification occurs (identification on 9 lines in the vertical blanking period). In this mode the black level is artificially inserted after demodulation.

Pin 6. System identification

During PAL reception the typical voltage at pin 6 is 10,2 V. This causes the luminance stage to be connected internally to the chrominance output at pin 8 and also activates the PAL matrix for normal PAL signals. During SECAM reception the typical voltage at pin 6 is 7 V. This changes the internal connection of the output from the luminance stage to the sequential phase modulator and enables the SECAM switch. Noisy SECAM signals cause the voltage at pin 6 to increase, colour killing occurs at 9,8 V and colour is reinstated at 9,1 V.

Pin 7. Carrier generation

An 8,8 MHz signal from the PAL decoder is applied via pin 7 to the divider circuit in the TDA3590A. From this two 4,4 MHz signals are obtained with a phase shift of 90° with respect to each other. These signals are applied to the modulator via an H/2 switch. The delay of the 8,8 MHz input must be adjusted for minimum burst amplitude of the chrominance signal at pin 28 of the PAL decoder. With this condition the burst generated by the TDA3590A is in phase with the (R-Y) reference signal for the PAL decoder demodulator (the a.c.c. of the PAL decoder operates in the + (R-Y) direction).

Pin 8. Chrominance output

During PAL reception this output is connected internally to the luminance stage and a composite PAL video signal is present at pin 8. During SECAM reception the sequential phase modulator is connected to this output to give a quasi-PAL signal from pin 8. Typical peak-to-peak amplitudes of the signal from pin 8 are 900 mV for PAL (with peak-to-peak input at pin 16 of 1,2 V) and 500 mV for SECAM. The output signals are applied via a chrominance bandpass filter to the chrominance a.c.c. amplifier input of the PAL decoder.

Pins 9 and 10. Divider resetting

The output of the PAL decoder burst phase detector is connected to pins 9 and 10 of TDA3590A. During SECAM reception this signal carries differential a.c. current information about the phase relationship of the 4,4 MHz dividers of both ICs. The TDA3590A generates a minimum relative voltage between pins 9 and 10 at an absolute voltage level of 10,5 V. This overrules the PAL decoder oscillator control function causing the oscillator to run at 2 x 4,43 MHz.

Pins 11, 12, 13 and 14. SECAM switch and PAL matrix

The PAL matrix circuit is enabled by system identification of PAL reception. The signal inputs to the matrix are the (direct) a.c.c. composite video output from the PAL decoder via an attenuator to pin 11 and a delayed version of the same signal via a glass delay line to pin 12. Active matrixing takes place in the IC and the separated (R-Y) and (B-Y) signals are available at pins 13 and 14 respectively.

The SECAM switch circuit is selected by system identification of SECAM reception. The inputs to the SECAM switch are the sequentially modulated quasi-PAL signals, direct and delayed, to pins 11 and 12 respectively. The SECAM switch separates the (R-Y) and (B-Y) signals which are then available at pins 13 and 14 respectively.

Pins 15 and 16. Luminance signals

The maximum peak-to-peak amplitude of the input to pin 16 should be 1,7 V. The relatively high input impedance of the luminance amplifier allows a 22 nF coupling capacitor to be used. The luminance amplifier has internal input clamping and a gain of 8 dB. The output is available at pin 15.

During SECAM reception the luminance signal is delayed approximately 470 ns by an external delay line to equalize the SECAM processing delay. The luminance and chrominance outputs are then correctly timed.

During PAL reception the PAL composite video signal passes through the external delay line and, after amplification, is available at pins 15 and 8.

APPLICATION INFORMATION (continued)

Pins 17 and 18. Supply voltage (+ 12 V)

Correct operation is ensured within the supply voltage range of 10,8 to 13,2 V. The typical power dissipation of the IC at 12 V is 1,2 W.

Pins 17 and 18 are separated by an external RC filter. Pin 18 supplies all the output stages and the biasing for several current sinks in the IC. Separation of the supply voltages minimizes crosstalk between the various parts of the IC. The capacitor at pin 18 must be small ($\approx 1\ \mu F$) to avoid the possibility of internal damage to the IC by discharge current should pin 17 be short-circuited to ground.

Pin 19. Sandcastle pulse

The required three-level sandcastle pulse may be coupled directly to the sandcastle pulse detector input at pin 19. The horizontal blanking, vertical blanking and burst gate pulses are separated by the IC.

Pin 20. De-emphasis

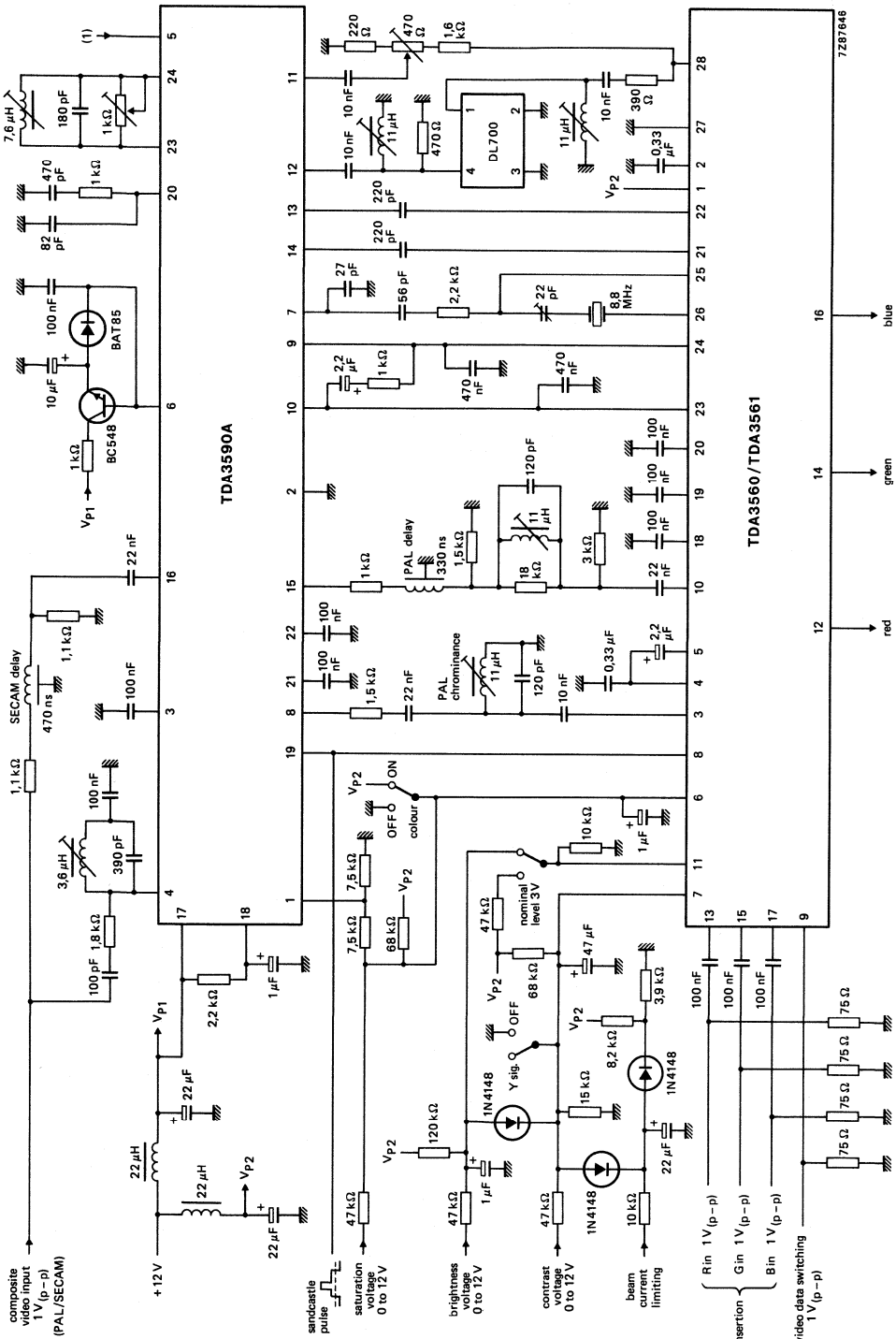
De-emphasis is performed at this pin with a 1 kΩ resistor and a 470 pF capacitor. Additional filtering of the 8,8 MHz signal using an 82 pF coupling capacitor prevents moiré patterns appearing on the screen.

Pins 21 and 22. Clamping of (R-Y) and (B-Y) signals

Clamping of the colour difference signals is performed after they have been separated. The normal value for the clamping storage capacitors is 100 nF but this may be increased to 470 nF if required.

Pins 23 and 24. Demodulator reference tuned circuit

The SECAM signal is applied to the demodulator via a bell filter and a limiter amplifier. Only one chrominance demodulator is used because of the sequential nature of the signal. The reference signal from the tuned circuit is applied to pins 23 and 24. Tuning and damping adjustments of the reference tuned circuit should be performed at $V_{5\text{-}2} > 2$ V (SECAM video (R-Y) (B-Y) information switched off). Adjustments should be such that minimum modulator voltage appears at pin 8, then any deviations between the black levels (when clamping on the back porch and when an artificial black level is filled in) can be made minimum.



(1) See Application Information for pin 5 – horizontal/vertical identification.

Fig. 3 PAL/SECAM decoder application.

APPLICATION INFORMATION (continued)

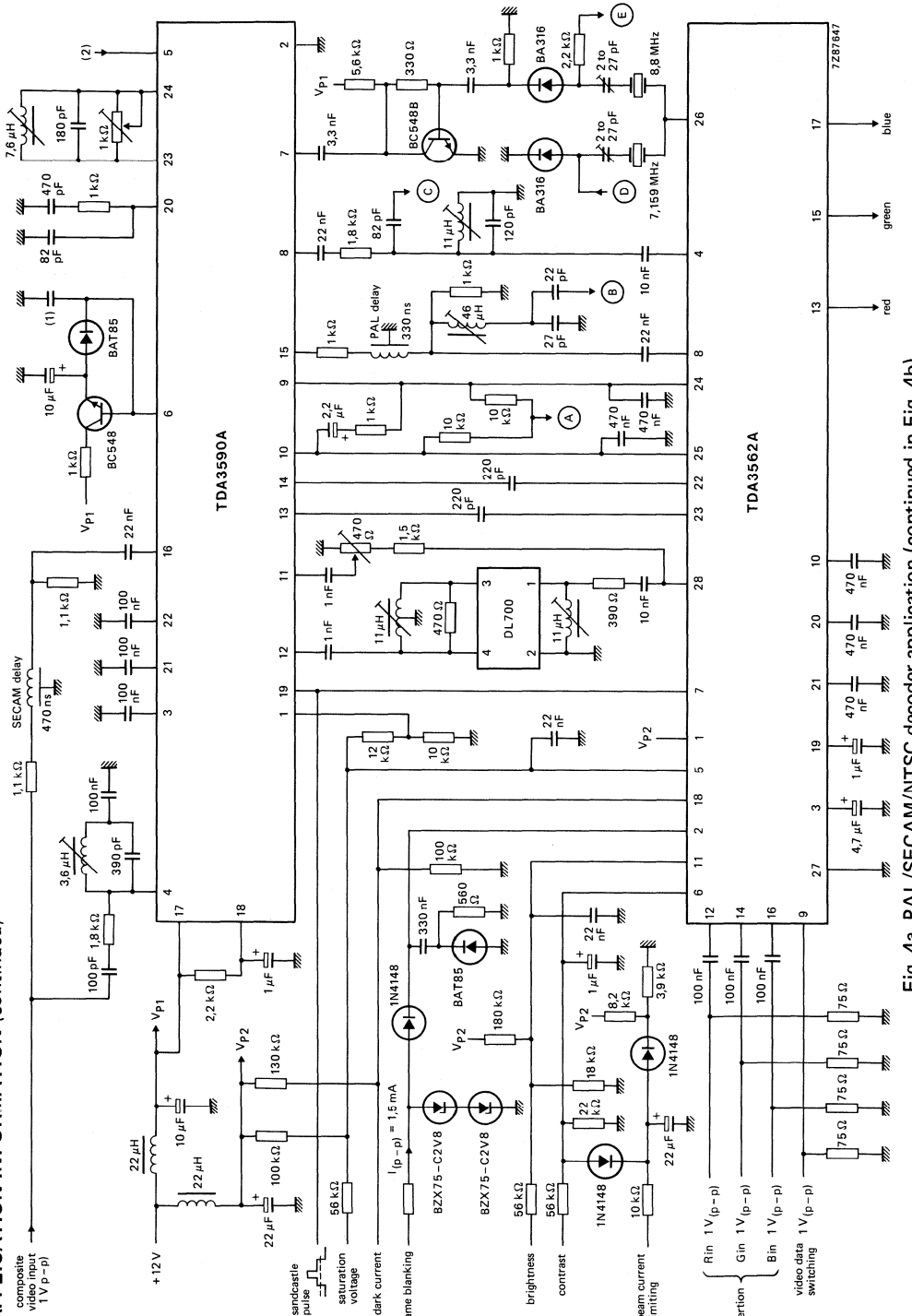
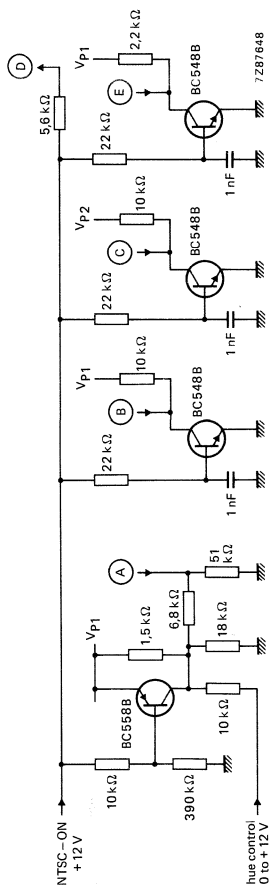


Fig. 4a PAL/SECAM/NTSC decoder application (continued in Fig. 4b).



(1) Capacitor value = 100 nF for horizontal identification or 1 μF for vertical identification.
(2) See Application Information for pin 5 — horizontal/vertical identification.

Fig. 4b PAL/SECAM/NTSC decoder application (continued from Fig. 4a).

SECAM-PAL TRANSCODER

GENERAL DESCRIPTION

The TDA3592A transcoder circuit converts SECAM input signals into true PAL signals, and can be used in combination with all types of PAL decoder.

Features

- Limiter input for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Modulator to provide true PAL signals
- 4,43 MHz oscillator
- Sandcastle pulse detector
- Identification circuit for horizontal and vertical SECAM identification
- Can be used with all types of PAL decoder
- Power-saving feature operates when supply voltage falls to (typ.) 5 V: SECAM processing shuts down but $\overline{\text{SECAM}}$ signal path remains active

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 17)		V_P	9,0	12,0	13,2	V
Supply current (pin 17)	V_P = 12 V	I_P	65	90	115	mA
Supply current (pin 17 and 18) (SECAM only)	V_P = 5 V	I_P	16	20	24	mA
Chrominance amplifier and demodulator						
Input signal $\overline{\text{SECAM}}$ (pin 3) (peak-to-peak value)		$V_{3\text{-}1(p\text{-}p)}$	–	–	1100	mV
Input signal SECAM (pin 3) (peak-to-peak value)		$V_{3\text{-}1(p\text{-}p)}$	15	100	300	mV
Output signal PAL (pin 9) (peak-to-peak value)	pin 3 = 280 kHz	$V_{9\text{-}1(p\text{-}p)}$	–	820	–	mV
Identification						
Input voltage range for horizontal identification (pin 4)		$V_{4\text{-}1}$	4,1	–	V_P	V
Input voltage range for vertical identification (pin 4)		$V_{4\text{-}1}$	0	–	2,9	V
Identification at pin 6		$V_{6\text{-}1}$	–	10,6	–	V
Slicing level reference voltage (pin 5)		$V_{5\text{-}1}$	–	7,0	–	V
Sandcastle pulse detector						
Vertical blanking level		$V_{19\text{-}1}$	–	1,5	–	V
Horizontal blanking level		$V_{19\text{-}1}$	–	3,5	–	V
Burst gating level		$V_{19\text{-}1}$	–	7,0	–	V
Luminance amplifier						
Luminance input signal (peak-to-peak value)		$V_{16\text{-}1(p\text{-}p)}$	–	1,2	–	V
Luminance amplifier gain at 4,4 MHz		$G_{16\text{-}15}$	–	7,0	–	dB

PACKAGE OUTLINE

24-lead DIL; plastic with heat spreader (SOT-101B).

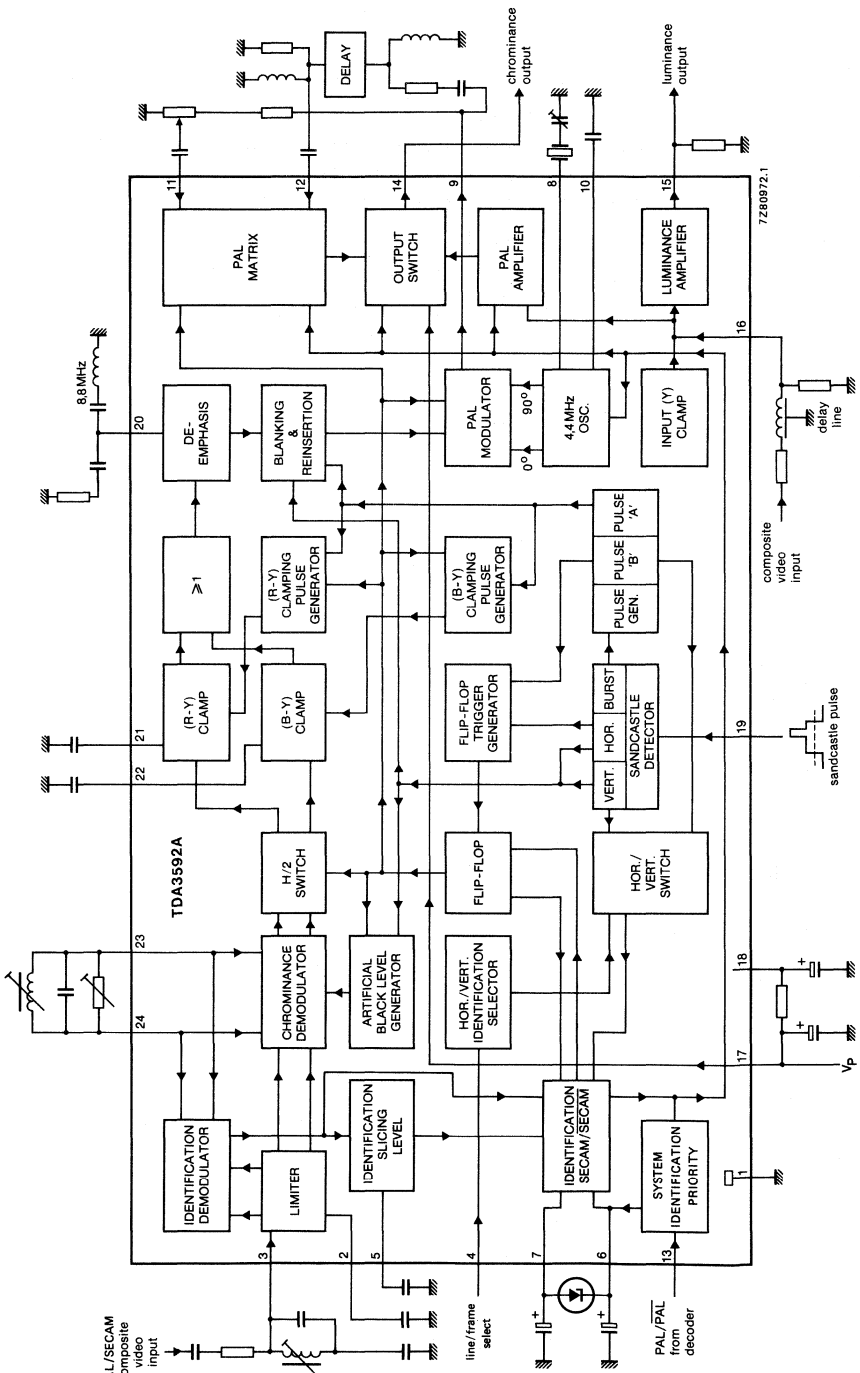


Fig. 1 Block diagram.

PINNING

1. Ground.
2. Limiter feedback.
3. Limiter input: chrominance input SECAM; identification input SECAM/$\overline{\text{SECAM}}$.
4. Identification selection input using a DC level to preset the identification mode.
   At $V_4 < 2{,}9$ V the TDA3592A is preset for frame identification.
   At $V_4 > 4{,}1$ V the TDA3592A is preset for line identification.
5. Storage capacitor input for floating level identification.
6. Storage capacitor input to SECAM/$\overline{\text{SECAM}}$ identification circuit.
7. Double time-constant input to SECAM/$\overline{\text{SECAM}}$ identification circuit.
8. 4,43 MHz oscillator.
9. Sequentially modulated output.
10. Decoupling capacitor for miller integrator feedback circuit.
11. Direct input chrominance signal.
12. Delayed input chrominance signal.
13. PAL/$\overline{\text{PAL}}$ input signal from PAL decoder.
14. Chrominance output signal.
15. Luminance output signal.
16. Luminance/$\overline{\text{SECAM}}$ input signal.
17. Positive supply voltage (V_P).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input.
20. De-emphasis circuit connection: R = 560 Ω; C = 1 nF.
21. Storage capacitor connection for (R-Y) clamp.
22. Storage capacitor connection for (B-Y) clamp.
23. Demodulator reference tuned circuit: nominal frequency = 4,33 MHz; nominal $Q_L = 2{,}45$.
24. As for pin 23.

FUNCTIONAL DESCRIPTION

Demodulation

The chrominance and identification demodulators of the TDA3592A both share the same reference tuned circuit (pins 23 and 24). The identification circuit automatically detects whether the incoming signal is SECAM or $\overline{\text{SECAM}}$ (NTSC, PAL or black-and-white).

When the incoming signals are PAL they are diverted via pin 16 to the chrominance output at pin 14 and no signal demodulation takes place. The delay line connected to pin 16 delays the signals to equalize the delay of the SECAM-PAL transcoding process. When SECAM signals are received, the PAL signal path is switched off.

Incoming SECAM signals are applied to pin 3 via an external bell filter. The signals are amplified, limited and then demodulated. Only one demodulator is necessary as the colour difference signals are available sequentially. After demodulation the colour difference signals are separated by an H/2 switch and then applied to (R-Y) and (B-Y) clamp circuits where the black levels are clamped to the same DC level. With all conditions at pin 4, artificial black levels are inserted during the horizontal blanking periods. This is done because of the possibility of horizontal burst signals not being available. The artificial levels may not be identical to the detected black level due to circuit spread but this can be corrected by detuning the reference tuned circuit.

The two colour difference signals are combined again after clamping and then applied to the modulator via de-emphasis, blanking and reinsertion circuits. The ratio of (R-Y) to (B-Y) at the de-emphasis output (pin 20) is 1,78.

Modulation

A burst signal is reinserted into the combined SECAM signal at the input to the PAL modulator. At this input the phase relationship for magenta colour is +(R-Y) and −(B-Y). The modulation carriers for the (R-Y) and (B-Y) signals are 90^{o} out of phase; for a magenta colour the modulated (R-Y) component has the same phase position as the (R-Y) burst. The (B-Y) burst is modulated 180^{o} out of phase with respect to the (B-Y) component of a magenta-coloured input signal.

Identification SECAM/$\overline{\text{SECAM}}$

Identification of the SECAM signal is performed using the fact that only SECAM signals have a line-to-line difference in voltage level. The identification circuit compares the phase of the demodulated voltage difference waveform with the phase of the flip-flop output. If the phase relationship is not correct, the flip-flop is reset by an extra pulse from the flip-flop trigger generator. For horizontal identification the phase comparison is performed during the period of pulse 'B' (see Fig. 2). When vertical identification is selected, the comparison is performed only during the horizontal scan of the vertical blanking. The SECAM identification circuits operate when selected by the voltage on pin 4; this may be horizontal, vertical or combined horizontal and vertical identification, depending on the switching arrangements of pin 4.
These are as follows:

- Horizontal identification preset when $V_{4\text{-}1} < 2{,}9$ V;
- Vertical identification preset when $V_{4\text{-}1} > 4{,}1$ V;
- Horizontal/vertical combination when sandcastle pulse is present on pin 4.

Information obtained from the identification detector is also used for colour killing and, if required, for switching to PAL.

Sandcastle pulse detection

The sandcastle pulse detector requires a three-level sandcastle pulse to provide horizontal blanking, vertical blanking and burst gate pulses. The detector burst gate pulse triggers a pulse generator which produces two timing pulses, pulse 'A' and pulse 'B' (see Fig. 2). Pulse 'A' is used to time the PAL modulator burst and to sample the (R-Y) and (B-Y) clamping pulse generators. A (R-Y) clamping pulse is generated only during a red line and a (B-Y) clamping pulse only during a blue line. Pulse 'B' times the SECAM horizontal identification.

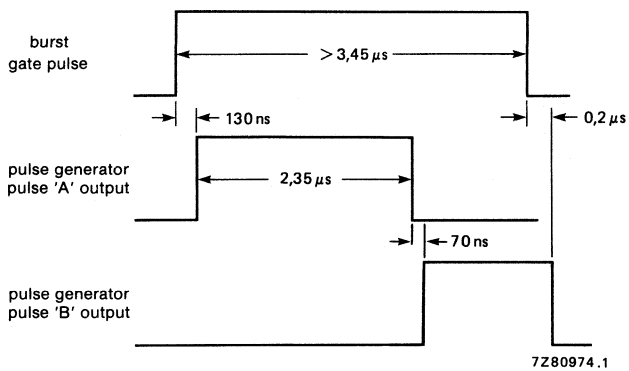


Fig. 2 Burst gate timing pulse generation.

Carrier generation

The carrier signal for the PAL modulator is obtained from a 4,43 MHz oscillator. An internal Miller integrator operates in conjunction with the decoupling capacitor at pin 10 to provide the required 90^{o} phase shift.

PAL matrix

The signal output from the PAL modulator at pin 9 is sequentially modulated with (R-Y) burst phased in the +(R-Y) direction, and (B-Y) burst phased in the −(B-Y) direction. This PAL signal is applied directly to pin 11 and via a 64 μs delay to pin 12. A true PAL signal is constructed in the PAL matrix by means of an additional/substraction process (in a correct H/2 sequence) using the delayed and undelayed inputs.

FUNCTIONAL DESCRIPTION (continued)

Coupling of identification systems

Coupling of a TDA3592A and a PAL decoder can be performed to obtain an optimum identification system. The system operates using the functions of pins 13, 6 and 7: the voltage level at pin 13 is controlled by the PAL/$\overline{\text{PAL}}$ detection of the PAL decoder; and the voltage level at pins 6 and 7 are functions of SECAM/$\overline{\text{SECAM}}$ detection in the TDA3592A.

The circuit action is as follows and is summarized in Table 1.

Channel switching — During channel switching pin 6 is taken rapidly to a high voltage (± 10,2 V), this corresponds to the $\overline{\text{SECAM}}$ mode of the TDA3592A.

PAL — The high voltage level at pin 6 caused by channel switching is maintained by the TDA3592A when it recognizes the signal as $\overline{\text{SECAM}}$ (this condition is maintained even if reflected PAL signals are present). The PAL decoder recognizes the signal as PAL and takes pin 13 of TDA3592A to a voltage greater than 1,7 V. The TDA3592A is now held in the $\overline{\text{SECAM}}$ condition by an internal current source at pin 6.

SECAM — The initial high voltage level (+ 10,2 V) at pin 6 caused by channel switching sets the TDA3592A in the $\overline{\text{SECAM}}$ mode and during this time the PAL decoder detects a $\overline{\text{PAL}}$ signal. This causes a voltage at pin 13 of $< 1{,}1$ V which prevents the internal current source of TDA3592A maintaining the high voltage level of pin 6 which, in turn, allows the TDA3592A to detect SECAM. The initiation of SECAM detection is delayed by the action of the external circuit at pins 6 and 7 and commences as pin 6 approaches 7,0 V. The SECAM signals are converted by TDA3592A to PAL signals at pin 14, which results in the PAL decoder switching to the PAL mode (the TDA3592A remains in the SECAM mode).

Black-and-white — The TDA3592A is initially set in the $\overline{\text{SECAM}}$ mode as previously described. The PAL decoder detects $\overline{\text{PAL}}$ and the TDA3592A detects $\overline{\text{SECAM}}$ which results in a system operation in the colour-killing mode.

Table 1 System operating modes

TDA3592A	PAL decoder mode	System operating mode
SECAM	PAL	SECAM
SECAM	$\overline{\text{PAL}}$	condition not used
$\overline{\text{SECAM}}$	PAL	PAL
$\overline{\text{SECAM}}$	$\overline{\text{PAL}}$	black-and-white

System priorities

When TDA3592A pin 13 is connected to the PAL/$\overline{\text{PAL}}$ output of a PAL decoder, the system will give PAL priority in signal identification. Connecting TDA3592A pin 13 to ground will give SECAM priority.

Luminance and chrominance signal paths

The signal input at pin 16 is clamped by a circuit which detects the top of the luminance signal sync pulse. This clamp, the luminance signal path to pin 15 and the $\overline{\text{SECAM}}$ signal path to pin 14 remain active when the supply voltage falls to (typ.) 5 V. At this level of supply voltage the SECAM processing circuits are switched off, giving a reduction in total power dissipation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	V_P	–	13,2	V
Total power dissipation	P_{tot}	–	1,78	W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−25	+150	°C

CHARACTERISTICS

$V_P = V_{17-1} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified.
The parameter values are valid only when the reference tuned circuit has been aligned as detailed in note 1. All voltages are reference to ground pin 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 17)		V_{17}	9,0	12	13,2	V
Supply current (pin 17)		I_{17}	65	90	115	mA
Supply current (pin 18)		I_{18}	40	–	160	μA
Decoupled supply voltage (pin 18)	$R_{ext17-18} = 2$ kΩ	V_{18}	8,8	11,8	13,2	V
External capacitance (pin 18)		C_{18}	–	–	10	μF
Total power dissipation		P_{tot}	–	1,08	1,38	W
Thermal resistance, junction to ambient		$R_{th\ j-a}$	–	40	45	K/W
Chrominance amplifier and demodulator						
Input signal SECAM (peak-to-peak value)		$V_{3(p-p)}$	–	–	1100	mV
Input signal SECAM at which correct limiting occurs (peak-to-peak value)		$V_{3(p-p)}$	15	100	300	mV
Input resistance (pin 3)		R_3	9,6	12,1	14,6	kΩ
Input capacitance (pin 3)		C_3	–	–	5	pF
Input resistance between pins 23 and 24		R_{23-24}	2,9	3,6	4,3	kΩ
Input capacitance between pins 23 and 24		C_{23-24}	–	12	–	pF
De-emphasis output resistance (pin 20)		R_{20}	0,9	1,1	1,3	kΩ
Chrominance demodulator zero point stability (pin 20)	note 2	f_0	–	5	–	kHz

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Chrominance amplifier and demodulator (continued)						
Linearity of (B-Y) demodulation (pin 20)	note 3	–	–	94	–	%
Linearity of (R-Y) demodulation (pin 20)	note 4	–	–	100	–	%
(R-Y)/(B-Y) ratio (pin 20)		–	–	1,78	–	%
Relative deviation of reinserted black level/demodulated black level (pin 20) as a function of temperature						
(R-Y) signals	note 5	–	–	0,22	–	kHz/°C
(B-Y) signals	note 5	–	–	0,22	–	kHz/°C
Identification SECAM/$\overline{\text{SECAM}}$	note 6					
Input voltage for line identification (pin 4)		V_4	4,1	–	V_P	V
Input voltage for frame identification (pin 4)		V_4	0	–	2,9	V
Switching level for line/frame identification (pin 4)		V_4	3,0	3,5	4,0	V
Input current (pin 4)		$-I_4$	–	5	25	μA
Voltage at pin 6 during $\overline{\text{SECAM}}$/PAL		V_6	–	10,2	–	V
Voltage at pin 6 during $\overline{\text{SECAM}}$/PAL		V_6	–	11,5	–	V
Voltage at pin 6 during SECAM		V_6	–	7,0	–	V
Identification at pin 6		V_6	–	10,6	–	V
Colour OFF for SECAM		V_6	9,8	10,1	10,4	V
Colour ON for SECAM		V_6	8,8	9,1	9,4	V
Slicing level reference voltage (pin 5)		V_5	–	8,4	–	V
Sandcastle pulse detector and clamping pulse generator						
Voltage level at which the vertical blanking pulse is separated		V_{19}	1,0	1,5	2,0	V
Voltage level at which the horizontal blanking pulse is separated		V_{19}	3,0	3,5	4,0	V
Voltage level at which the burst gating pulse is separated		V_{19}	6,5	7,0	7,5	V

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle pulse detector and clamping pulse generator (continued)						
Input current	V_{19} = 0 V	$-I_{19}$	–	30	100	μA
Width of pulse 'A' (Fig. 2)	note 7		1,85	2,35	2,85	μA
Required width of pulse 'B' (Fig. 2)	note 7		0,6	–	–	μs
Luminance amplifier						
Input signal (peak-to-peak value) (pin 16)		$V_{16(p-p)}$	–	1,2	1,7	V
Gain (pin 16 to 15)	f_{16} = 4,4 MHz	G_{16-15}	6,5	7,5	8,5	dB
Input current (pin 16)		I_{16}	–	1,0	5,0	μA
Output impedance (pin 15)		Z_{15}	–	20	–	Ω
Frequency response at −3 dB (pin 15 and 16)		f	6,0	–	–	MHz
Gain (pin 16 to 14)	f_{16} = 4,4 MHz	G_{16-14}	6,0	7,0	8,0	dB
Frequency response at −3 dB (pin 14 and 16)		f	6,0	–	–	MHz
External load resistance (pin 15)		R_L	2,0	–	–	kΩ
Limiter, chrominance demodulator and PAL modulator	note 8					
Output resistance (pin 9)		R_9	–	25	–	Ω
DC output voltage during horizontal blanking (pin 9)		V_9	–	9,6	–	V
Internal biasing resistor for emitter follower (pin 9)			–	9,0	–	kΩ
External load resistance (pin 9)		$R_{L(9)}$	2	–	–	kΩ
Output signal (pin 9) when input to pin 3 has a Δf of 280 kHz; without external load (peak-to-peak value)		$V_{9(p-p)}$	–	0,82	–	mV
(R-Y)/(B-Y) ratio (pin 9)			1,50	1,78	2,11	
Chrominance/burst ratio for SECAM (pin 9)			2,5	3,0	3,5	
Linearity of (B-Y) signal (pin 9)	note 3		85	92	99	%
Linearity of (R-Y) signal (pin 9)	note 4		93	100	107	%
Black level shift as a function of temperature (pin 9)						
(R-Y) signals	note 9		–	0,22	–	kHz/°C
(B-Y) signals	note 9		–	0,22	–	kHz/°C

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Limiter, chrominance demodulator and PAL modulator (continued)						
Phase relationship of modulated (R-Y) burst to modulated (B-Y) burst (pin 9)			87	90	93	deg
Amplitude relationship of modulated (R-Y) burst to modulated (B-Y) burst (pin 9)			−1,5	0	+1,5	dB
Black level shift as a function of supply voltage (pin 9)						
(R-Y) signal			–	−1,5	–	kHz/V
(B-Y) signal			–	1,0	–	kHz/V
Oscillator						
Oscillator frequency (pin 9) (set with series capacitor)		f_{OSC}	–	4,433619	–	MHz
Frequency deviation without spread of external components (pin 9)		Δf_{OSC}	–	–	±150	Hz
Temperature coefficient of oscillator frequency (pin 9)			–	−2	−3	Hz/°C
Frequency deviation for change of V_P from 9,0 to 13,2 V		Δf_{OSC}	–	–	150	Hz
DC voltage (pin 8)		V_8	–	4,7	–	V
Input resistance (pin 8)		R_8	–	1	–	kΩ
DC voltage (pin 10)		V_{10}	–	4,4	–	V
Input resistance (pin 10)		R_{10}	–	2	–	kΩ
PAL matrix						
Input resistance (pin 11)		R_{11}	700	900	1100	Ω
Input resistance (pin 12)		R_{12}	700	900	1100	Ω
Output resistance (pin 14) (SECAM/$\overline{\text{SECAM}}$)		R_{14}	–	40	–	Ω
Internal emitter follower load resistance (pin 14)		$R_{INT(14)}$	–	7	–	kΩ
External load resistor (pin 14)		$R_{L(14)}$	2,4	–	–	kΩ
DC voltage (pin 11)		V_{11}	–	5,0	–	V
DC voltage (pin 12)		V_{12}	–	5,0	–	V
DC voltage (pin 14)	SECAM mode	V_{14}	–	6,2	–	V
DC voltage (pin 14)	$\overline{\text{SECAM}}$ mode and line blanking	V_{14}	–	4,9	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
PAL matrix (continued)						
H/2 ripple on chrominance output (pin 14) (peak-to-peak value)	SECAM mode	$V_{14(p-p)}$	–	–	100	mV
Gain A; pin 11 to 14		G_A	9	10	11	dB
Gain B; pin 12 to 14 ((R-Y) at pin 9)		G_B	9	10	11	dB
Gain C; pin 12 to 14 ((B-Y) at pin 9)		G_C	9	10	11	dB
Gain A – gain B		G_A-G_B	–0,7	–	+0,7	dB
Gain A – gain C		G_A-G_C	–0,7	–	+0,7	dB
Gain B – gain C		G_B-G_C	–0,7	–	+0,7	dB
Phase A; pins 11, 14 to pins 12, 14 ((R-Y) at pin 9)			–	181,5	–	deg
Phase B; pins 11, 14 to pins 12, 14 ((B-Y) at pin 9)			–	1,5	–	deg
Phase A – phase B			178	180	182	deg
Identification PAL/$\overline{\text{PAL}}$						
Input condition for PAL (pin 13)		V_{13}	1,7	–	V_P	V
Input condition for $\overline{\text{PAL}}$ (pin 13)		V_{13}	–	–	1,1	V
Input current	V_{13} = 6 V	I_{13}	–	–	10	μA
Input resistance	V_{13} = 8,2 V	R_{13}	7,5	11,5	15,5	kΩ
Pin 6 internal current in PAL/$\overline{\text{SECAM}}$ mode		$-I_6$	0,24	0,4	0,58	mA
Switching level PAL/$\overline{\text{PAL}}$ (pin 13)		V_{13}	1,2	1,4	1,6	V

CHARACTERISTICS AT LOW SUPPLY VOLTAGE

$V_P = V_{17-1} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply current		$I_{17}+I_{18}$	16	20	24	mA
Supply voltage switching level for preset SECAM signal path	SECAM processing OFF	V_{17-1}	6,5	7,5	8,2	V
Luminance amplifier						
Input signal (peak-to-peak value)		$V_{16(p-p)}$	–	0,45	0,56	V
Gain (pin 16 to 15)	$f_{16} = 4,4$ MHz	G_{16-15}	6,0	7,0	8,0	dB
Input current (pin 16)		I_{16}	–	1,0	5,0	μA
Output impedance (pin 15)		$\lvert Z_{15-1} \rvert$	–	20	–	Ω
Minimum load resistance (pin 15)		R_L	2	–	–	kΩ
Frequency response at –3 dB (pin 16 to 15)		f	6,0	–	–	MHz
Gain (pin 16 to 14)	$f_{16} = 4,4$ MHz	G_{16-14}	5,7	6,8	7,9	dB
Frequency response at –3 dB (pin 16 to 14)		f	6	–	–	MHz

Notes to the characteristics

1. The parameter values given in the characteristics are valid only when the following alignment procedure is performed:
   a. Supply a SECAM signal input to pin 3 at 100 mV (peak-to-peak value) without deviation during a red and blue line (SECAM black colour information).
   b. Align the reference tuned circuit so that the output signal from pin 14 to the PAL decoder is minimum during scan (PAL black colour information).
2. When the input signal to the limiter (pin 3) changes from 300 to 15 mV (peak-to-peak value) the zero point of the chrominance demodulator shifts by a typical value of 5 kHz; f = 4,33 MHz (typ.).
3. (B-Y) linearity is defined by $V_{out(yellow)}/V_{out(blue)}$ where f_{yellow} = (typ.) 4,02 MHz; f_{blue} = (typ.) 4,48 MHz.
4. (R-Y) linearity is defined by $V_{out(cyan)}/V_{out(red)}$ where f_{cyan} = (typ.) 4,68 MHz; f_{red} = (typ.) 4,12 MHz.
5. The parameter value is equated by: $\frac{(B\text{-}D)/F - (A\text{-}C)/E}{Y - X} \times \frac{\Delta f\ (kHz)}{^{o}C}$

   $E = \frac{E1 - E2}{2}$ $\quad F = \frac{F1 - F2}{2}$

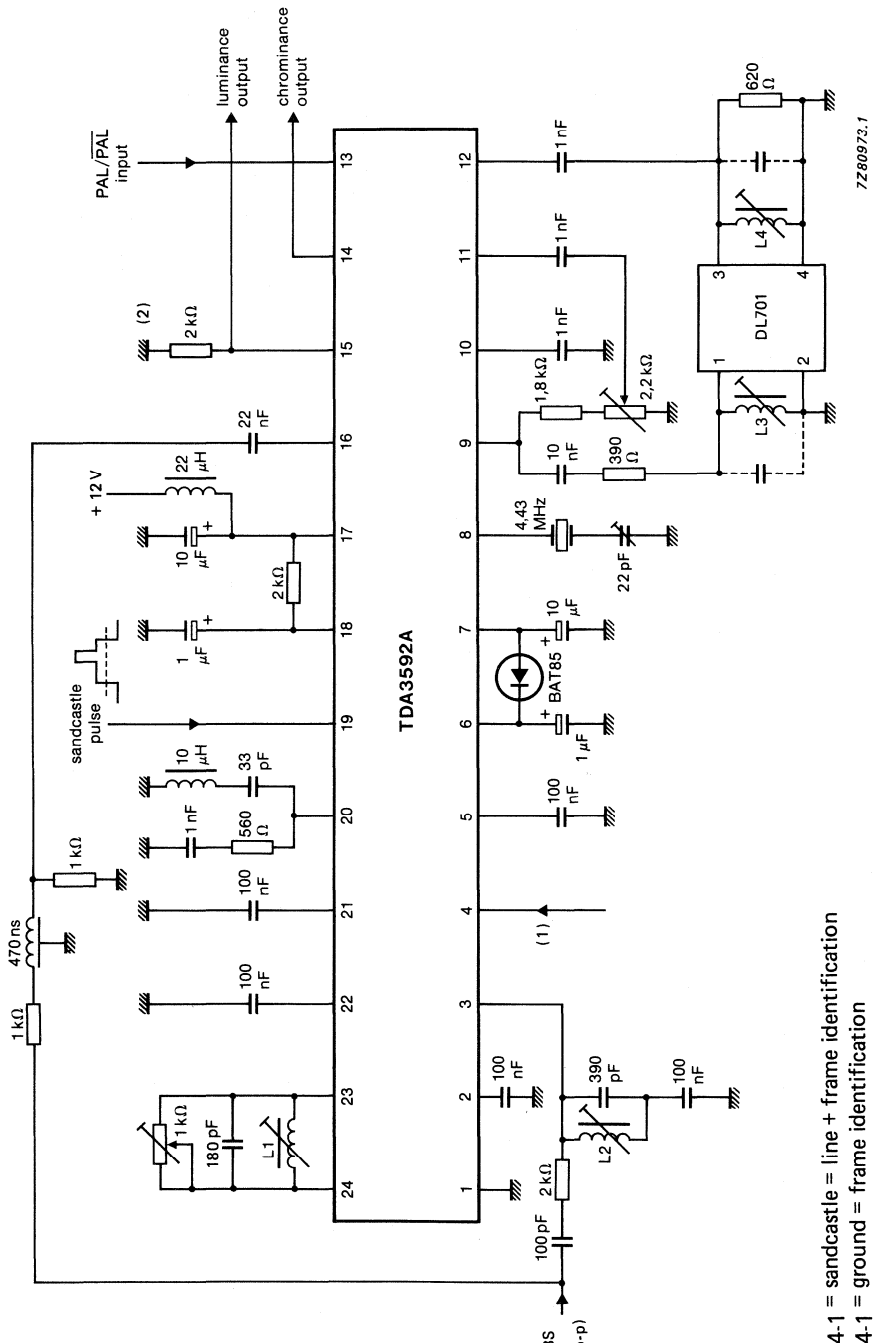
   Where A = demodulated black level at temperature X
   B = demodulated black level at temperature Y
   C = artificial black level at temperature X
   D = artificial black level at temperature Y
   E1 = demodulated output signal at temperature X ($f_o - \Delta f$)
   E2 = demodulated output signal at temperature X ($f_o + \Delta f$)
   F1 = demodulated output signal at temperature Y ($f_o - \Delta f$)
   F2 = demodulated output signal at temperature Y ($f_o + \Delta f$)

   for B-Y: $f_o = f_{ob}$ = 4,25 MHz (Δf = 230 kHz)
   for R-Y: $f_o = f_{or}$ = 4,40625 MHz (Δf = 280 kHz)
6. During stable signal conditions V_7 is always at V_F(BAT85) below V_6.
7. The burst gate pulse width > 3,45 μs.
8. The specification figures are only valid when the reference tuned circuit is aligned as indicated in note 1.
9. Ensure that the 4,433 MHz carrier is in the correct phase; black level shift at temperature X = A and at Y = B.
   Output signal (Δf = 230 kHz for B-Y; Δf = 280 kHz for R-Y) at temperature X = E and at Y = F.

   The parameter is equated by: $\frac{(B/(F\text{-}B) - A/(E\text{-}A)}{Y - X} \times 230;\ 280\ kHz$
10. Chrominance definition — burst ratio at SECAM condition (pin 9).

    The parameter is equated by: $\frac{V_{out(p\text{-}p)}\ Red\ (R\text{-}Y)}{V_{burst(p\text{-}p)}\ (R\text{-}Y)}$.

APPLICATION INFORMATION



(1) V4-1 = sandcastle = line + frame identification
V4-1 = ground = frame identification
V4-1 = Vp = line identification

(2) minimum load resistance at pin 15 = 2 kΩ

Fig. 3 Application circuit.

VERTICAL DEFLECTION AND GUARD CIRCUIT (90°)

GENERAL DESCRIPTION

The TDA3653B/C is a vertical deflection output circuit for drive of various deflection systems with currents up to 1.5 A peak-to-peak.

Features

- Driver
- Output stage
- Thermal protection and output stage protection
- Flyback generator
- Voltage stabilizer
- Guard circuit

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply (note 1)					
Supply voltage range					
pin 9	$V_P = V_{9-4}$	10	–	40	V
pin 6	V_{6-4}	–	–	60	V
Output (pin 5)					
Peak output voltage during flyback	V_{5-4M}	–	–	60	V
Output current	$I_{5(p-p)}$	–	1.2	1.5	A
Operating junction temperature range	T_j	−25	–	+ 150	°C
Thermal resistance junction to mounting base					
(SOT110B)	$R_{th\ j-mb}$	–	10	–	K/W
(SOT131)	$R_{th\ j-mb}$	–	3.5	–	K/W

Note to the quick reference data

1. The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 60 V.

PACKAGE OUTLINES

TDA3653B: 9-lead SIL; plastic (SOT110B).
TDA3653C: 9-lead SIL; plastic power (SOT131).

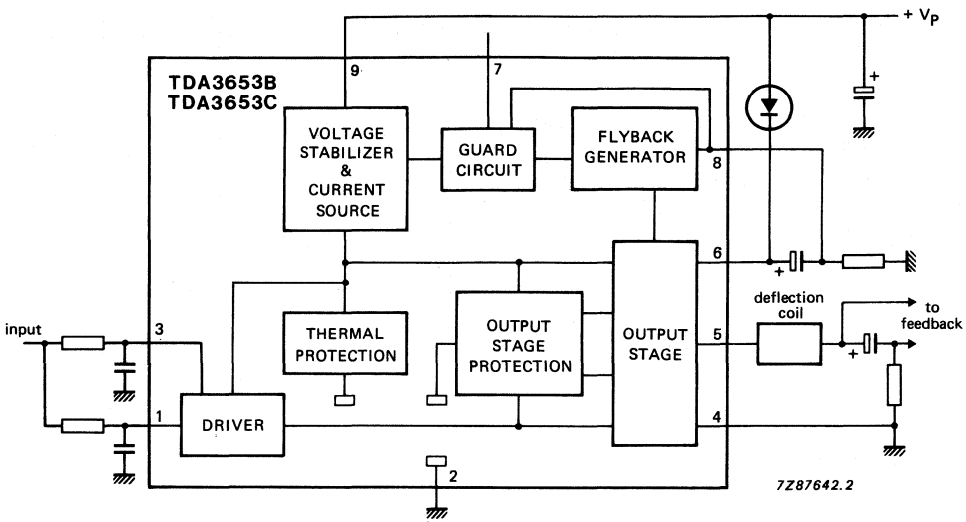


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Output stage and protection circuit

Pin 5 is the output pin. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. The output transistors of the class-B output stage can each deliver 0.75 A maximum. The maximum voltage for pin 5 and 6 is 60 V.

The output power transistors are protected such that their operation remains within the SOAR area. This is achieved by the co-operation of the thermal protection circuit, the current-voltage detector, the short-circuit protection and the special measures in the internal circuit layout.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied via external resistors to pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator.

External connection of pin 1 to pin 3 allows for applications in which the pins are driven separately.

Flyback generator

During scan the capacitor connected between pins 6 and 8 is charged to a level which is dependent on the value of the resistor at pin 8 (see Fig.1).
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage, the flyback generator is activated.
The supply voltage is then connected in series, via pin 8, with the voltage across the capacitor during the flyback period.
This implies that during scan the supply voltage can be reduced to the required scan voltage plus saturation voltage of the output transistors.
The amplitude of the flyback voltage can be chosen by changing the value of the external resistor at pin 8.
It should be noted that the application is chosen such that the lowest voltage at pin 8 is > 2.5 V, during normal operation.

Guard circuit

When there is no deflection current and the flyback generator is not activated, the voltage at pin 8 reduces to less than 1.8 V. The guard circuit will then produce a DC voltage at pin 7, which can be used to blank the picture tube and thus prevent screen damage.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V to drive the output stage, which prevents the drive current of the output stage being affected by supply voltage variations.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134); pins 4 and 2 externally connected to ground.

paramater	symbol	min.	max.	unit
Supply voltage (pin 9)	$V_P = V_{9-4}$	—	40	V
Supply voltage output stage (pin 6)	V_{6-4}	—	60	V
Output voltage (pin 5)	V_{5-4}	—	60	V
Input voltage (pins 1 and 3)	$V_{1;\,3-2}$	—	V_P	V
External voltage at pin 7	V_{7-2}	—	5.8	V
Peak output current (pin 5)				
repetitive	$\pm I_{5RM}$	—	0.75	A
non-repetitive	$\pm I_{5SM}$	—	1.5	A*
Peak output current (pin 8)				
repetitive	I_{8RM}	0.85	0.75	A
non-repetitive	$\pm I_{8SM}$	—	1.5	A*
Total power dissipation	P_{tot}	see Fig. 2		
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	see Fig. 2		
Operating junction temperature range	T_j	−25	+150	°C

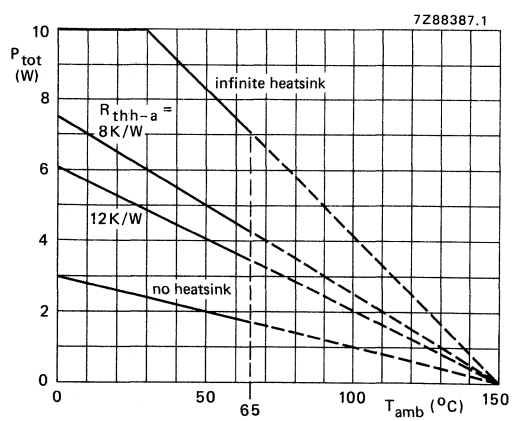


Fig. 2 Power derating curves (for SOT110B).

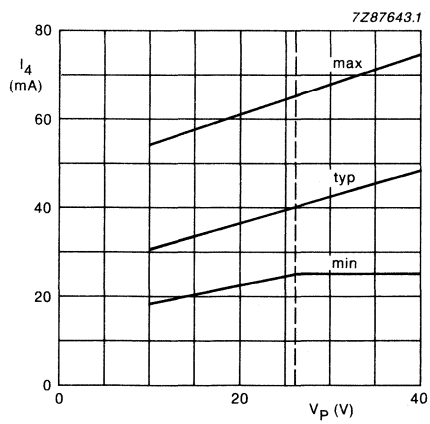


Fig. 3 Quiescent current I_4 as a function of supply voltage V_P.

* Non-repetitive duty factor maximum 3.3%.

CHARACTERISTICS

$V_P = V_{9-4} = 26$ V; $T_{amb} = 25$ °C; pins 2 and 4 externally connected to ground; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 9)	note 1	$V_P = V_{9-4}$	10	–	40	V
Supply voltage (pin 6)	note 1	V_{6-4}	–	–	60	V
Total supply current (pin 6 and pin 9)	note 2	$I_P = I_6 + I_9$	34	50	85	mA
Quiescent current (pin 4)	see Fig. 3	I_4	25	40	65	mA
Variation of quiescent current with temperature		ΔI_4	–	–0.04	–	mA/K
Output current						
Output current (pin 5) (peak-to-peak value)		$I_{5(p-p)}$	–	1.2	1.5	A
Output current flyback generator (pin 8)		$-I_8$	–	0.7	0.85	A
Output current flyback generator (pin 8)		I_8	–	0.6	0.75	A
Output voltage						
Peak voltage during flyback		V_{5-4M}	–	–	60	V
Saturation voltage to supply						
at $-I_5 = 0.75$ A		V_{6-5sat}	–	2.5	3.0	V
at $I_5 = 0.75$ A	note 3	V_{5-6sat}	–	2.5	3.0	V
at $-I_5 = 0.60$ A		V_{6-5sat}	–	2.2	2.7	V
at $I_5 = 0.60$ A	note 3	V_{5-6sat}	–	2.3	2.8	V
Saturation voltage to ground						
at $I_5 = 0.75$ A		V_{5-4sat}	–	2.3	2.7	V
at $I_5 = 0.60$ A		V_{5-4sat}	–	2.1	2.4	V
Flyback generator						
Saturation voltage						
at $-I_8 = 0.85$ A		V_{9-8sat}	–	1.6	2.1	V
at $I_8 = 0.75$ A	note 3	V_{8-9sat}	–	2.3	2.8	V
at $-I_8 = 0.70$ A		V_{9-8sat}	–	1.4	1.9	V
at $I_8 = 0.60$ A	note 3	V_{8-9sat}	–	2.2	2.7	V
Flyback generator active if:		V_{5-9}	4.0	–	–	V
Leakage current at pin 8		$-I_8$	–	5.0	100	μA
Input						
Input current (pin 1)	$I_5 = 0.75$ A	I_1	–	0.33	0.55	mA
Input voltage during scan (pin 1)	$I_5 = 0.75$ A	V_{1-2}	–	1.5	2.4	V
Input voltage during scan (pin 3) pins 1 and 3 not connected		V_{3-2}	0.8	–	V_P	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input (continued)						
Input current during scan (pin 3)						
pins 1 and 3 not connected		I_3	0.03	–	–	mA
pins 1 and 3 connected		I_3	–	–	0.21	mA
Input resistance (pin 3)		R_3	3.9	5.3	6.7	kΩ
Input voltage during flyback (pin 1)		V_{1-2}	–	–	250	mV
Input voltage during flyback (pin 3)		V_{3-2}	–	–	250	mV
Guard circuit						
Output voltage (pin 7)	note 4					
loaded with 100 kΩ		V_{7-2}	4.4	5.1	5.8	V
loaded with 0.5 mA		V_{7-2}	3.6	4.4	5.3	V
Internal series resistance of pin 7		R_{i7}	0.95	1.35	1.7	kΩ
Guard circuit active if V_{8-2} is lower than	note 5	V_{8-2}	–	–	1.8	V
General data						
Thermal protection becomes active if junction temperature exceeds		T_j	158	175	192	°C
Thermal resistance junction to mounting base		$R_{th\ j\text{-}mb}$	–	10	12	K/W
Open loop gain at 1 kHz	note 6	G_{ol}	–	42	–	dB
Frequency response (–3 dB)	note 7	f	–	40	–	kHz

Notes to the characteristics

1. The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 60 V.
2. When V_{5-4} = 13 V and no load at pin 5.
3. Duty factor maximum 3.3%.
4. Guard circuit is active.
5. During normal operation the voltage V_{8-2} may not be lower than 2.5 V.
6. R_{load} = 8 Ω; $I_{load(rms)}$ = 125 mA.
7. With 220 pF between pins 1 and 5.

APPLICATION INFORMATION

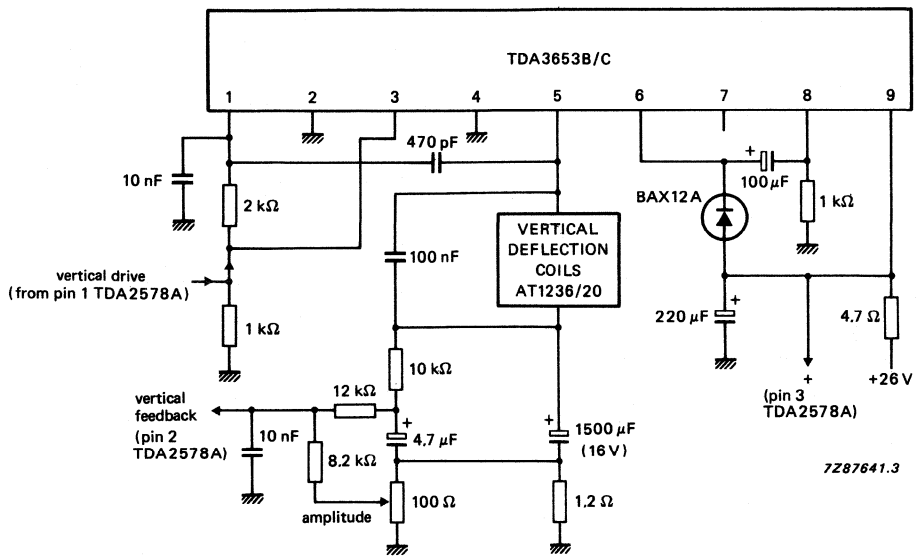


Fig. 4 Typical application circuit diagram of the TDA3653B/C (vertical output), when used in combination with the TDA2578A (see Fig. 5).

Note to deflection coils AT1236/20: L = 29 mH, R = 13.6 Ω; deflection current without overscan is 0.82 A peak-to-peak and EHT voltage is 25 kV.

APPLICATION INFORMATION (continued)

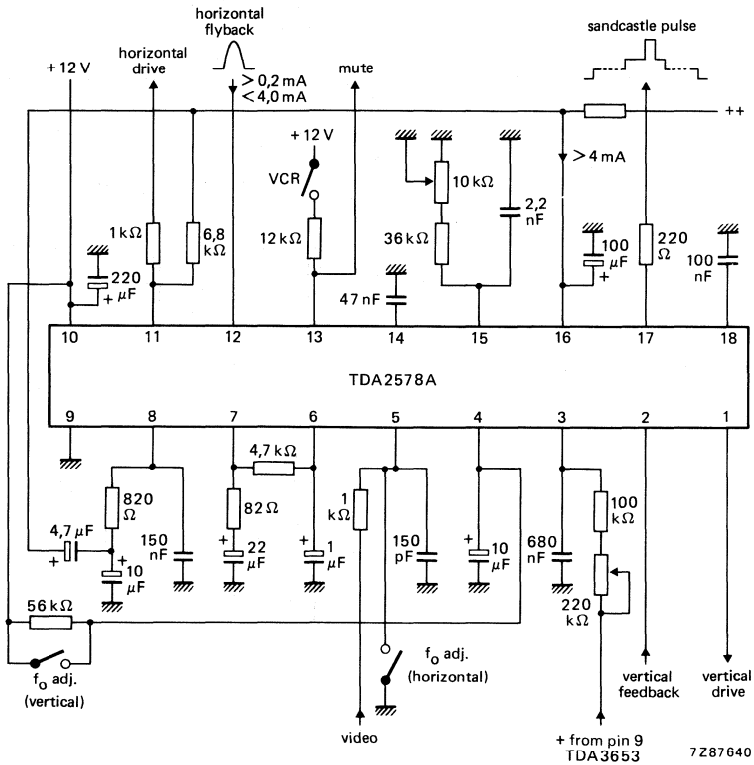
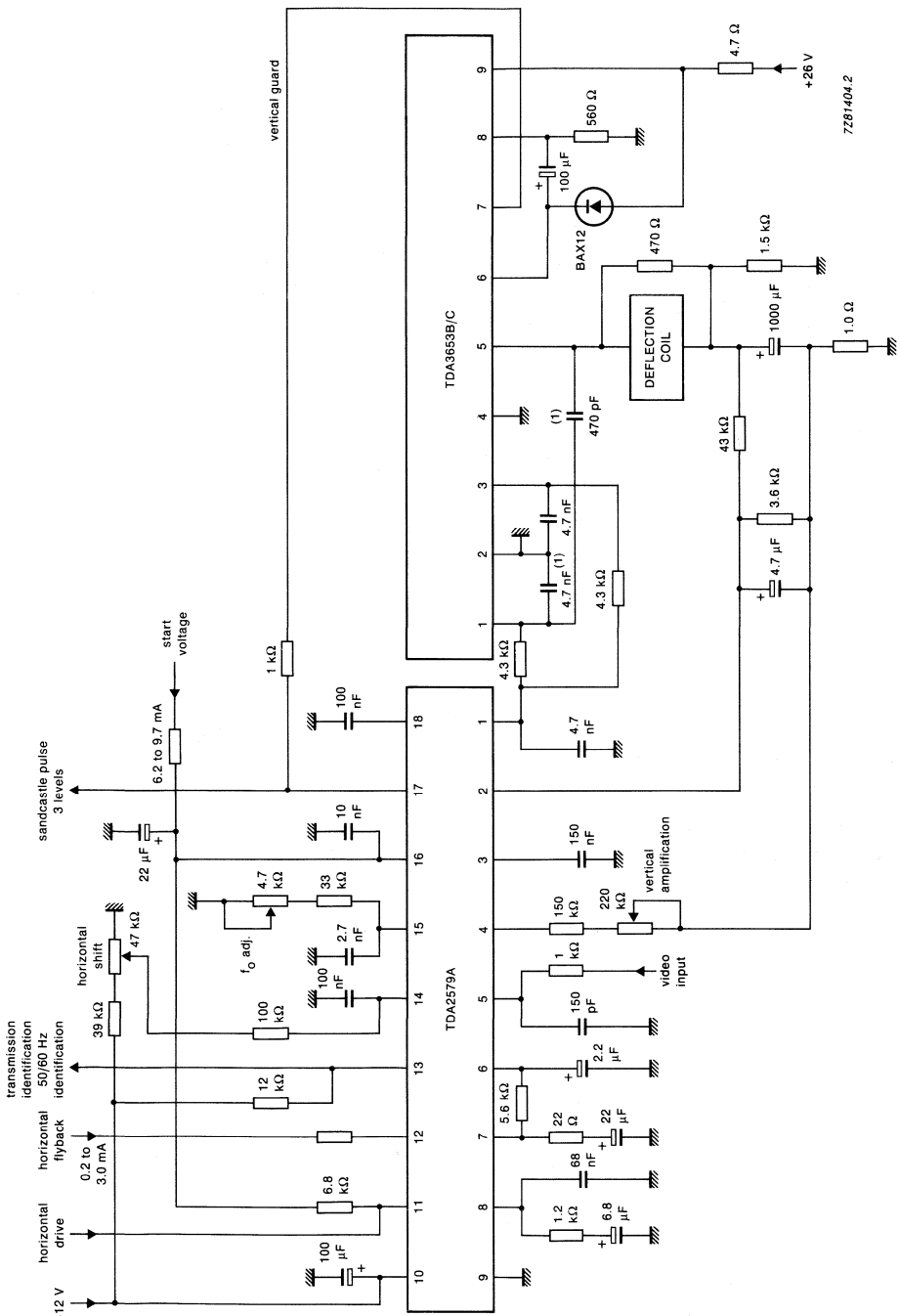


Fig. 5 Typical application circuit diagram; for combination of the TDA2578A with the TDA3653B/C (see Fig. 4).



(1) Dependent on PCB layout.

Fig.6 Application circuit diagram for combination with TDA2579A for 90° picture tube.

VERTICAL DEFLECTION AND GUARD CIRCUIT (110°)

GENERAL DESCRIPTION

The TDA3654 is a full performance vertical deflection output circuit for direct drive of the deflection coils and can be used for a wide range of 90° and 110° deflection systems.
A guard circuit is provided which blanks the picture tube screen in the absence of deflection current.

Features

- Direct drive to the deflection coils
- 90° and 110° deflection system
- Internal blanking guard circuit
- Internal voltage stabilizer

QUICK REFERENCE DATA

Output voltage	V_{5-2}	max.	60 V
Output current (peak-to-peak)	$I_{5(p-p)}$	max.	3 A
Supply voltage	V_{9-2}	max.	40 V
Guard circuit output voltage	V_{7-2}	max.	5,6 V
Operating ambient temperature range	T_{amb}		−25 to +60 °C
Storage temperature	T_{stg}		−55 to +150 °C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j-mb}$	3,5 to 4 K/W

PACKAGE OUTLINES

TDA3654 : 9-lead SIL; plastic power (SOT131).
TDA3654Q : 9-lead SIL bent to DIL; plastic power (SOT157).

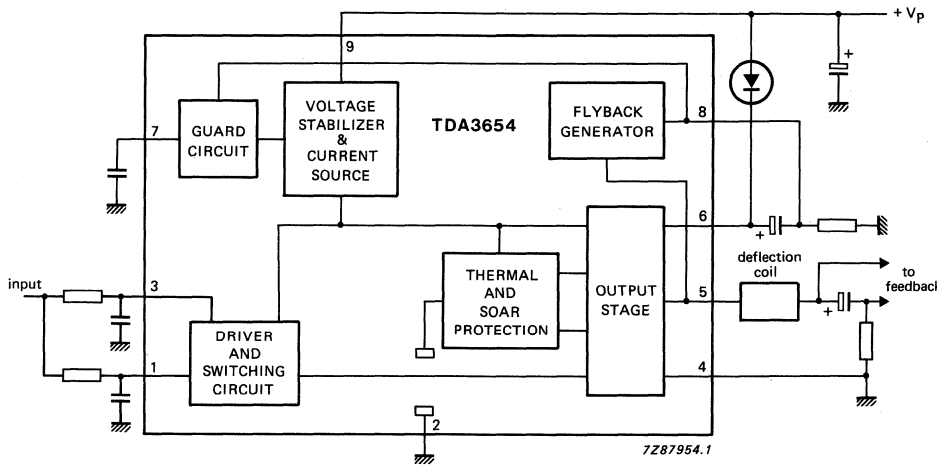


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Output stage and protection circuits

The output stage consists of two Darlington configurations in class B arrangement.
Each output transistor can deliver 1,5 A maximum and the V_{CEO} is 60 V.
Protection of the output stage is such that the operation of the transistors remains well within the SOAR area in all circumstances at the output pin, (pin 5). This is obtained by the cooperation of the thermal protection circuit, the current-voltage detector and the short circuit protection.
Special measures in the internal circuit layout give the output transistors extra solidity, this is illustrated in Fig. 5 where typical SOAR curves of the lower output transistor are given. The same curves also apply for the upper output device. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied to pin 3 which is the input of a switching circuit (pin 1 and 3 are connected via external resistors).
This switching circuit rapidly turns off the lower output stage when the flyback starts and it, therefore, allows a quick start of the flyback generator. The maximum required input signal for the maximum output current peak-to-peak value of 3 A is only 3 V, the sum of the currents in pins 1 and 3 is then maximum 1 mA.

Flyback generator

During scan, the capacitor between pins 6 and 8 is charged to a level which is dependent on the value of the resistor at pin 8 (see Fig. 1).
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage, the flyback generator is activated.
The supply voltage is then connected in series, via pin 8, with the voltage across the capacitor during the flyback period.
This implies that during scan the supply voltage can be reduced to the required scan voltage plus saturation voltage of the output transistors.
The amplitude of the flyback voltage can be chosen by changing the value of the external resistor at pin 8.
It should be noted that the application is chosen such that the lowest voltage at pin 8 is $> 1{,}5$ V, during normal operation.

Guard circuit

When there is no deflection current, for any reason, the voltage at pin 8 becomes less than 1 V, the guard circuit will produce a d.c. voltage at pin 7. This voltage can be used to blank the picture tube, so that the screen will not burn in.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V to drive the output stage, so the drive current is not affected by supply voltage variations.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134).
Pins 2 and 4 are externally connected to ground.

Voltages			
Output voltage	V_{5-4}	0 to 60	V
Supply voltage	V_{9-4}	0 to 40	V
Supply voltage output stage	V_{6-4}	0 to 60	V
Input voltage	V_{1-2}	0 to V_{9-4}	V
Input voltage switching circuit	V_{3-2}	0 to V_{9-4}	V
External voltage at pin 7	V_{7-2}	0 to 5,6	V
Currents			
Repetitive peak output current	$\pm I_{5RM}$	max. 1,5	A
Non-repetitive peak output current (note 1)	$\pm I_{5SM}$	max. 3	A
Repetitive peak output current of flyback generator	I_{8RM}	max. + 1,5 −1,6	A A
Non-repetitive peak output current of flyback generator (note 1)	$\pm I_{8SM}$	max. 3	A
Temperatures			
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to + 60	°C
Operating junction temperature range (the output current at pin 5 should not exceed 2.5A)	T_j	−25 to + 150	°C

CHARACTERISTICS

T_{amb} = 25 °C, supply voltage (V_{9-4}) = 26 V; unless otherwise stated; pin 1 externally connected to pin 3. Pins 2 and 4 externally connected to ground.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage, pin 9 (note 2)	V_{9-4}	10	–	40	V
Supply voltage output stage	V_{6-4}	–	–	60	V
Supply current, pins 6 and 9 (note 3)	I_6+I_9	35	55	85	mA
Quiescent current (note 4)	I_4	25	40	65	mA
Variation of quiescent current with temperature	TC	–	–0,04	–	mA/K
Output current					
Output current, pin 5 (peak-to-peak)	$I_{5(p-p)}$	–	2,5	3	A
Output current flyback generator, pin 8	$+I_{8(p-p)}$	–	1,25	1,5	A
	$-I_{8(p-p)}$	–	1,35	1,6	A
Output voltage					
Peak voltage during flyback	V_{5-4}	–	–	60	V
Saturation voltage to supply					
at I_5 = –1,5 A	$V_{6-5(sat)}$		2,5	3,2	V
at I_5 = 1,5 A (note 5)	$V_{5-6(sat)}$		2,5	3,2	V
at I_5 = –1,2 A	$V_{6-5(sat)}$		2,2	2,7	V
at I_5 = 1,2 A (note 5)	$V_{5-6(sat)}$		2,3	2,8	V
Saturation voltage to ground					
at I_5 = 1,2 A	$V_{5-4(sat)}$	–	2,2	2,7	V
at I_5 = 1,5 A	$V_{5-4(sat)}$	–	2,5	3,2	V
Flyback generator					
Saturation voltage					
at I_8 = –1,6 A	$V_{9-8(sat)}$	–	1,6	2,1	V
at I_8 = 1,5 A (note 5)	$V_{8-9(sat)}$	–	2,3	3	V
at I_8 = –1,3 A	$V_{9-8(sat)}$	–	1,4	1,9	V
at I_8 = 1,2 A (note 5)	$V_{8-9(sat)}$	–	2,2	2,7	V
Leakage current at pin 8	$-I_8$	–	5	100	μA
Flyback generator active if:	V_{5-9}	4	–	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Input					
Input current, pin 1, for I_5 = 1,5 A	I_1	–	0,33	0,55	mA
Input voltage during scan, pin 1	V_{1-2}	–	2,35	3	V
Input current, pin 3, during scan (note 6)	I_3	0,03	–	–	mA
Input voltage, pin 3, during scan (note 6)	V_{3-2}	0,8	–	V_{9-4}	V
Input voltage, pin 1, during flyback	V_{1-2}	–	–	250	mV
Input voltage, pin 3, during flyback	V_{3-2}	–	–	250	mV
Guard circuit					
Output voltage, pin 7 R_L = 100 kΩ (note 9)	V_{7-2}	4,1	4,5	5,8	V
Output voltage, pin 7 at I_L = 0,5 mA (note 9)	V_{7-2}	3,4	3,9	5,3	V
Internal series resistance of pin 7	Ri_7	0,95	1,35	1,7	kΩ
Guard circuit activates (note 7)	V_{8-2}	–	–	1,0	V
General data					
Thermal protection activation range	T_j	158	175	192	°C
Thermal resistance					
From junction to mounting base	$R_{th\ j\text{-}mb}$	–	3,5	4	K/W
Power dissipation	P_{tot}	–	see Fig. 3		
Open loop gain at 1 kHz; (note 8)	G_o	–	33	–	
Frequency response, –3 dB; (note 10)	f	–	60	–	kHz

Notes to the characteristics

1. Non-repetitive duty factor 3,3%.
2. The maximum supply voltage should be chosen so that during flyback the voltage at pin 5 does not exceed 60 V.
3. When V_{5-4} is 13 V and no load at pin 5.
4. See Fig. 4.
5. Duty cycle, d = 5% or d = 0,05.
6. When pin 3 is driven separately from pin 1.
7. During normal operation the voltage V_{8-2} may not be lower than 1,5 V.
8. $R_L = 8\ \Omega$; $I_L = 125$ mA (r.m.s.).
9. If guard circuit is active.
10. With a 22 pF capacitor between pins 1 and 5.

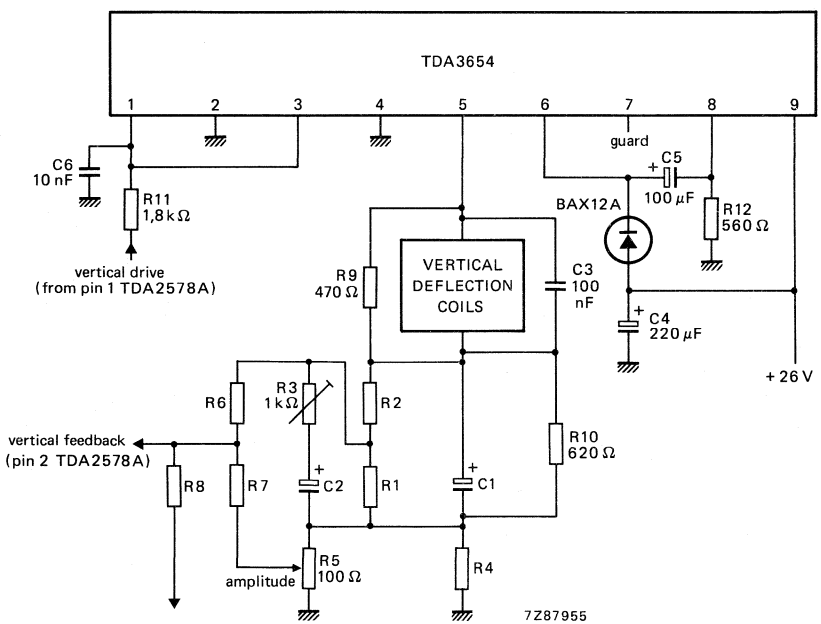


Fig. 2 Application diagram.

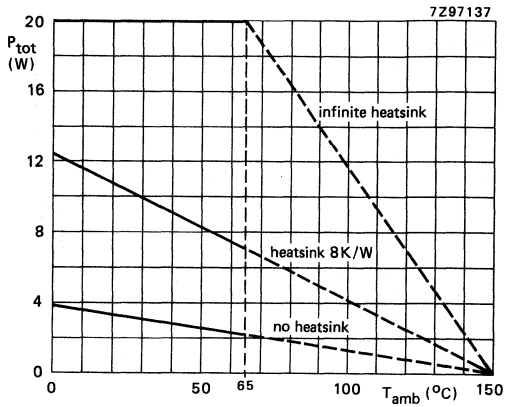


Fig. 3 Power derating curve.

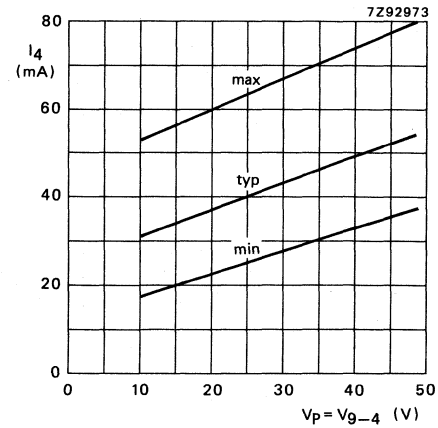
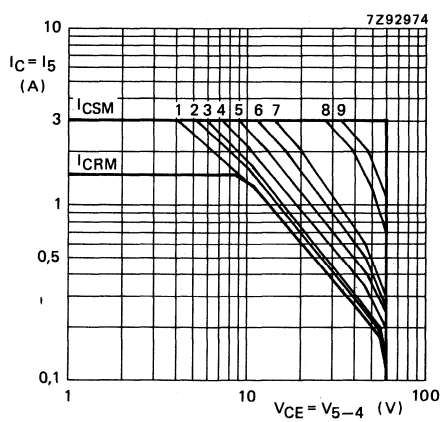


Fig. 4 Quiescent current as a function of the supply voltage.

curve	t_p	δ	peak junction temperature
1	d.c.	–	150 °C
2	10 ms	0,5	150 °C
3	10 ms	0,25	150 °C
4	1 ms	0,5	150 °C
5	1 ms	0,25	150 °C
6	1 ms	0,05	150 °C
7	1 ms	0,05	180 °C
8	0,2 ms	0,1	150 °C
9	0,2 ms	0,1	180 °C



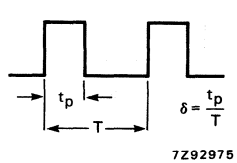


Fig. 5 Typical SOAR of lower output transistor.

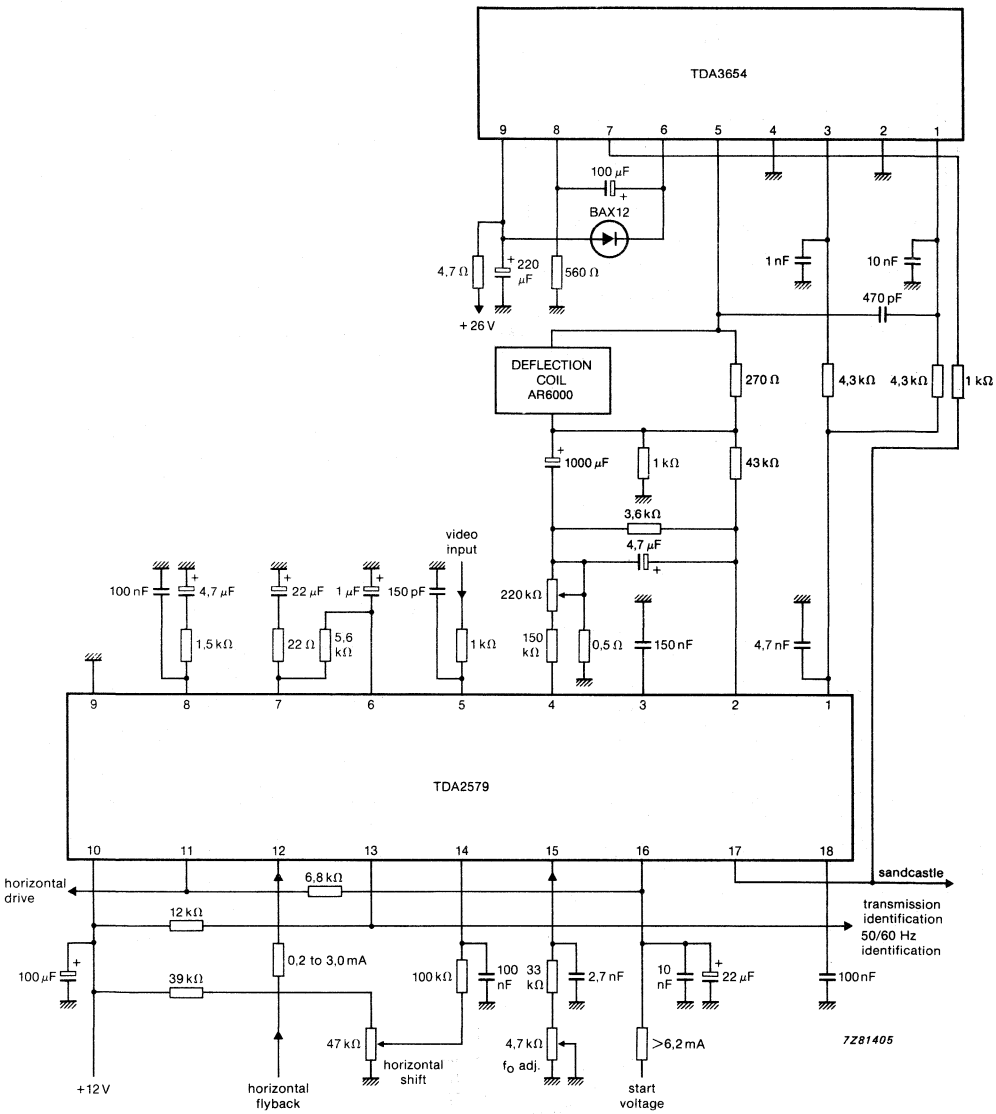


Fig. 6 Application diagram in combination with TDA2579.

PAL/NTSC/SECAM SYNCHRONIZATION PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3755 is a monolithic integrated circuit for PAL/NTSC SECAM synchronization processing in VHS video recorders.

Features

- Adaptive sync separator
- Internal vertical sync pulse integrator
- Composite sync and vertical pulse output
- Current controlled oscillator (CCO) with 320/321 times horizontal frequency
- Horizontal phase detector with current output
- Video identification and mute circuit
- Burst gating pulse output (externally adjustable phase relationship)
- Test-picture output
- Subcarrier frequency output switched in phase in accordance with VHS standard
- Fast phase correction of subcarrier frequency
- Selection input to force PAL or NTSC function
- Still picture input

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-15}$	typ.	10 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	24 mA
Sync separator			
Sync pulse input voltage (peak-to-peak value)	$V_{3-15(p-p)}$	typ.	300 mV
Sync pulse output voltage (peak-to-peak value)	$V_{1-15(p-p)}$	min.	7,3 V
Vertical sync pulse			
Output voltage (peak-to-peak value)	$V_{18-15(p-p)}$	min.	2,7 V
Phase detector			
Catching range	Δf	min.	± 3,0 %
Oscillator			
Oscillator frequency			
PAL	f_{osc}	typ.	5,02 MHz
NTSC	f_{osc}	typ.	5,04 MHz
Output frequency			
PAL	f_o	typ.	627 kHz
NTSC	f_o	typ.	629 kHz
Output sinewave (peak-to-peak value)	$V_{8-15(p-p)}$	typ.	3 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

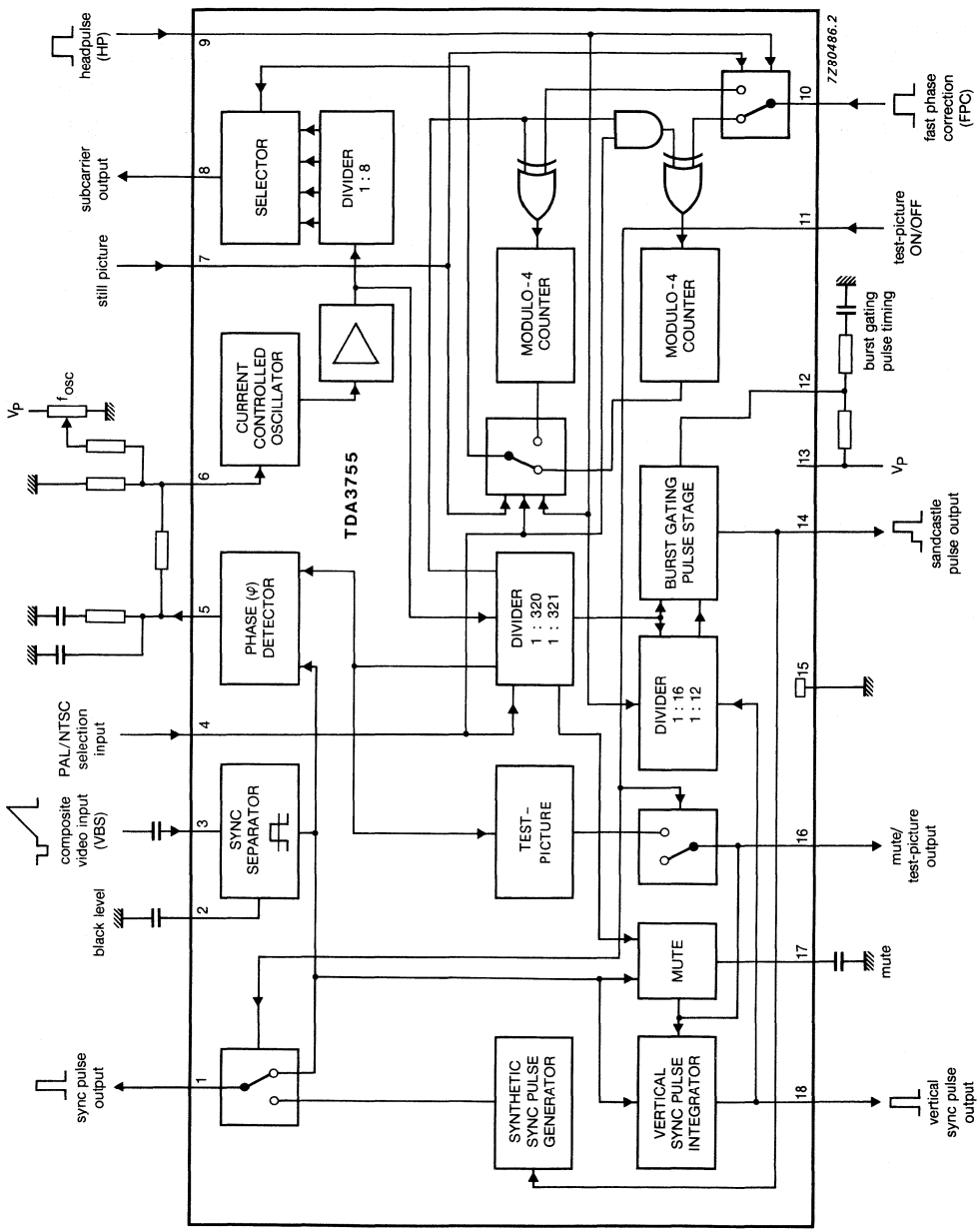


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-15}$	max.	13,2	V
Voltage range at pins 2, 3, 4, 7, 9, 10, 11, 17 to pin 15 (ground)	V_{n-15}		0 to V_P	V
Voltage range at pin 12	V_{12-15}	min.	0	V
Voltage range at pin 6	V_{6-15}	max.	8	V
Currents				
at pins 1, 5, 8, 14, 16, 18	$\pm I_n$	max.	5	mA
at pin 6	$-I_6$	max.	1	mA
at pin 12	I_{12}	max.	2	mA
Total power dissipation	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-15}$	9,6	–	13,2	V
Supply current	$I_P = I_{13}$	–	24	–	mA
Sync separator (pin 3)					
Colour composite video input voltage (note 1) (peak-to-peak value)	$V_{3-15(p-p)}$	–	1	–	V
Sync pulse amplitude (peak-to-peak value)	$V_{3-15(p-p)}$	75	–	600	mV
Slicing level, relative to sync pulse amplitude (note 2)		–	50	–	%
Internal resistance of video source	R_G	–	–	1	kΩ
Sync output voltage HIGH at $-I_1$ = 1 mA	V_{1-15}	7,8	–	–	V
Sync output voltage LOW at I_1 = 1 mA	V_{1-15}	–	–	0,5	V
Delay between signal at input pin 3 and sync pulse at output pin 1	t_d	–	0,2	–	μs
Vertical sync pulse (pin 18; note 3)					
Output voltage HIGH at $-I_{18}$ = 1 mA	V_{18-15}	2,7	–	5,0	V
Output voltage LOW at I_{18} = 1,6 mA	V_{18-15}	–	–	0,5	V
Duration of HIGH state of internally generated output pulse	t_p	–	190	–	μs
Delay between leading edge of input signal at pin 3 and leading edge of output pulse at pin 18	t_d	32	–	64	μs
Selection input (pin 4)					
Input voltage for NTSC state	V_{4-15}	–	–	0,3	V
Input current at V_{4-15} = 0 V	$-I_4$	–	–	20	μA
Input voltage for PAL state pin 4 open circuit or	V_{4-15}	2	–	–	V

parameter	symbol	min.	typ.	max.	unit
Test picture/mute/synthetic sync pulse					
Minimum voltage at pin 11 for test picture mode **active** (note 4)	V_{11-15}	4,8	–	–	V
Maximum voltage at pin 11 for test picture mode **inactive**	V_{11-15}	–	–	3,8	V
Output voltage at pin 16					
at test picture "black" or at mute	V_{16-15}	–	2,75	–	V
at test picture "white"	V_{16-15}	–	4,50	–	V
at "in sync condition"	V_{16-15}	–	–	0,5	V
Input current (pin 11)	$-I_{11}$	–	–	25	μA
Oscillator/phase detector					
Oscillator frequency (note 5)					
PAL	f_{osc}	–	5,02	–	MHz
NTSC	f_{osc}	–	5,04	–	MHz
Oscillator conversion gain	k_o	–	16,13	–	MHz/mA
D.C. control voltage	V_{6-15}	–	2,1	–	V
Input current for f = 5,016 MHz	$-I_{16}$	–	310	–	μA
Holding range (note 6)	Δf	± 3,2	–	–	%
Catching range (note 6)	Δf	± 3,0	–	–	%
Control loop gain	k_v	–	380 x 10^3	–	s^{-1}
Output of lower subcarrier (note 7) (peak-to-peak value)	$V_{8-15(p-p)}$	–	3	–	V
Output current	I_8	–	–	2	mA
D.C. output voltage	V_{8-15}	–	3,1	–	V
2nd harmonic suppression without switching	α_{2nd}	20	–	–	dB
Switching position prior to centre of sync pulse (pin 3)	t_s	–	2	–	μs
Output peak current of phase detector during sync pulse	$\pm I_5$	–	3,78	–	mA
Output voltage range (note 8)	V_{5-15}	1,4	–	2,8	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse (pin 14; note 9)					
Output voltage HIGH (note 10) at $-I_{14}$ = 1 mA	V_{14-15}	7,8	–	–	V
Output voltage INTERMEDIATE at $-I_{14}$ = 1 mA	V_{14-15}	2,3	3,0	3,7	V
Output voltage LOW at I_{14} = 1 mA	V_{14-15}	–	–	0,5	V
Lower part is starting prior to the centre of sync pulse at pin 3 and ending with the upper part	t_{14-3}	–	2,6	–	μs
Fast phase correction/head pulse					
Threshold voltage for fast phase correction (note 11)	V_{10-15}	–	7,2	–	V
Input current	$-I_{10}$	–	–	20	μA
Threshold voltage of head pulse input	V_{9-15}	–	1,4	–	V
Input current	$-I_9$	–	–	20	μA
D.C. input voltage	V_{7-15}	–	5,6	–	V
Input resistance	R_{7-15}	3	–	–	kΩ
Subcarrier phase switching (note 12)					
Phase switching of subcarrier phase in accordance with head pulse if	V_{7-15}	–	5,6*	–	V
LOW state of still picture input	V_{7-15}	–	–	0,5	V
Continuous phase switching regardless of head pulse if	V_{7-15}	–	V_P	–	V

* Or not connected.

Notes to characteristics

1. The sync separator input signal is shown in Fig. 2.

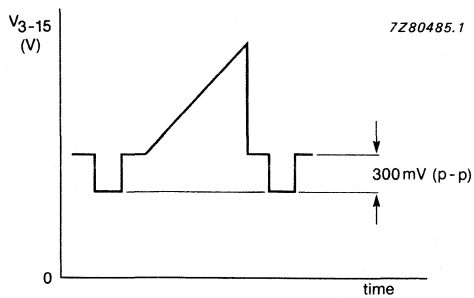
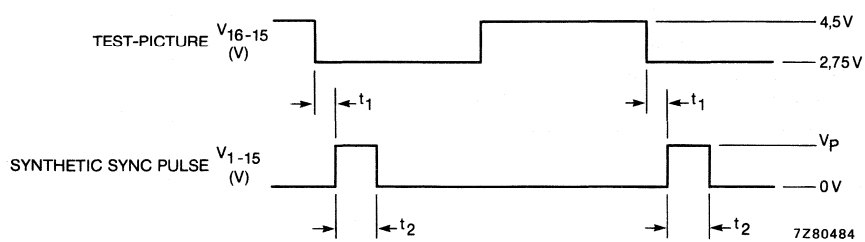


Fig. 2 Colour composite video input signal at pin 3.

2. The black level and the top sync level are detected internally and stored in capacitors at pin 2 and pin 3 respectively.
3. The vertical sync pulse output is disabled by mute.
4. In test picture mode the synthetic sync pulse is fed to output pin 1 and the vertical pulse consists of an uninterrupted block pulse of 192 μs triggering at every transition of head pulse (HP) at pin 9. The timing of test picture and synthetic sync pulse is shown in Fig. 3.



Where: The value of t_1 is dependent upon adjustment of the burst gating pulse delay.
Time t_2 is the burst gating pulse duration.

Fig. 3 Timing of test picture and synthetic sync pulse.

5. Oscillator adjustment during test picture mode made only, at $V_{11-15} > 4{,}8$ V, $V_{7-15} = 0$ V and $V_{4-15} > 2$ V or open circuit; measurement is $f_{osc}/8$ at output pin 8.
6. The holding range and catching range are both determined by the resistor connected between pin 5 and pin 6.
7. The phase of the lower subcarrier is switched in accordance with the VHS standard. PNP emitter follower, internal resistive load of 10 kΩ (typ.) to V_P.
8. The output voltage at pin 5 is disabled during test picture mode.

Notes to characteristics (continued)

9. The burst gating pulse is superimposed on an uninterrupted horizontal pulse. It is suppressed 16 times starting with every transition of the head pulse at pin 9. If a vertical pulse is detected during that time the burst gating pulses are additionally suppressed until line 12 and line 324 respectively. In any event the number of suppressed burst gating pulses is even.
10. The timing of the upper part of the sandcastle pulse is determined by the components connected to pin 12 (Fig. 4) and is independent of supply voltage variations.
11. The fast phase correction pulses have to be in the burst gating reference pulse. For any HIGH to LOW transitions of the correction pulse the phase is corrected by -90^{o} if the head pulse input is LOW and by $+90^{o}$ if the head pulse input is HIGH.
12. Subcarrier phase switching is detailed in Table 1.
    Subcarrier is 40,000 x f_H for NTSC state and 40,125 x f_H for PAL state.

Table 1 Subcarrier phase switching

still picture input	PAL		NTSC	
	HP = HIGH	HP = LOW	HP = HIGH	HP = LOW
HIGH	-90^{o}	-90^{o}	-90^{o}	-90^{o}
not connected	0^{o}	-90^{o}	$+90^{o}$	-90^{o}
LOW	0^{o}	0^{o}	$+90^{o}$	$+90^{o}$

APPLICATION INFORMATION

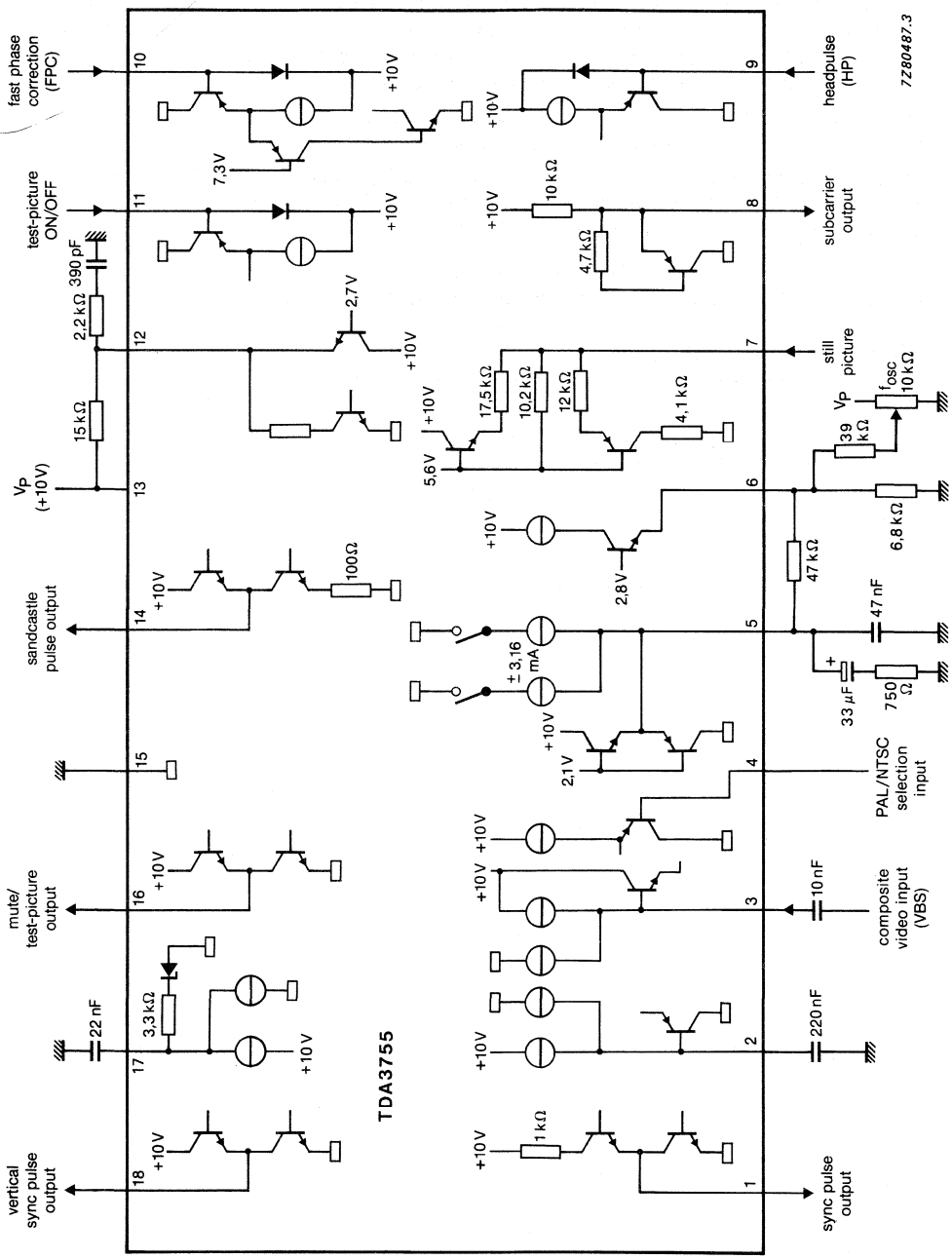


Fig. 4 Application circuit diagram.

BAND SELECTOR AND WINDOW DETECTOR

GENERAL DESCRIPTION

The TDA3791 is a monolithic integrated circuit intended for application in search-tuning systems for video recorders. It is designed to select one out of four tuners, each representing a particular band. Band selection tuning is indicated by a variable voltage V_{AFC}.

Features

- Voltage window detector
- Band switch selector
- 4 short-circuit protected band switches
- Muting circuit
- Delay circuit
- Short-circuit protection circuit
- Power-on reset

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	12 V
Supply current (pin 8)	$I_P = I_8$		
unloaded band switches ON		typ.	25 mA
all band switches OFF		typ.	12 mA
Power dissipation	P_{tot}	max.	1,8 W
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature range	T_{amb}	0 to 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38).

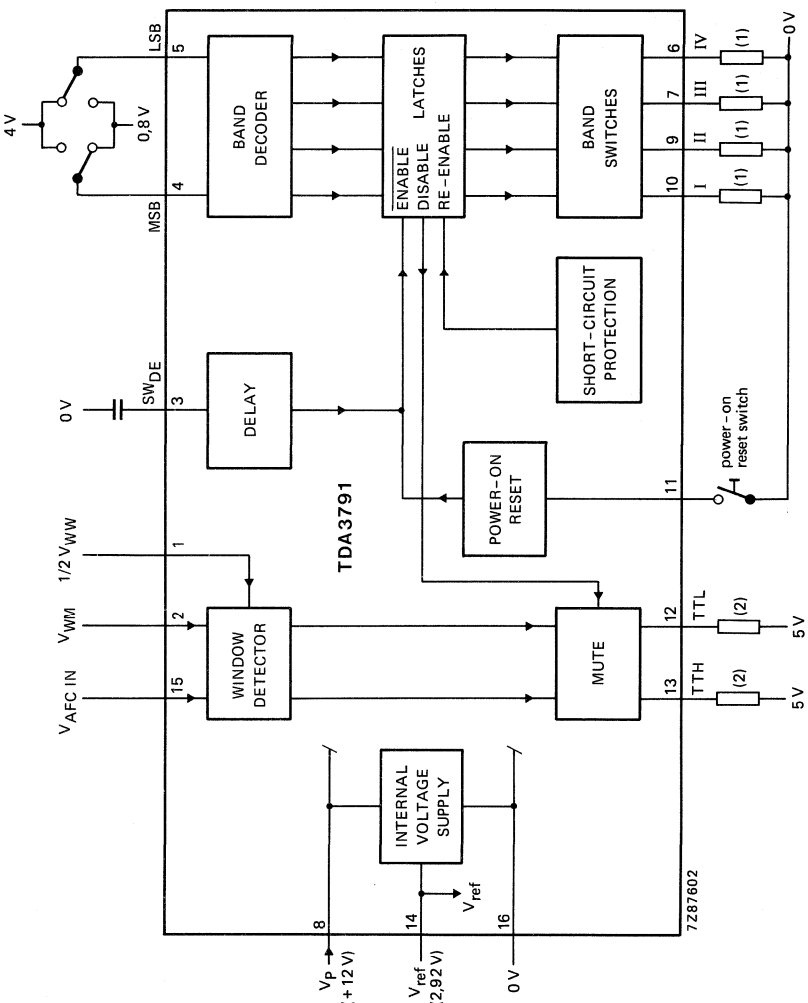


Fig. 1 Block diagram.

(1) $R = \frac{10\ V}{35\ mA}$. (2) $R = \frac{5\ V}{2\ mA}$.

FUNCTIONAL DESCRIPTION

Voltage window detector (see Table 1)

The voltage window is dependent upon two inputs; V_{WM} (pin 2) and $1/2V_{WW}$ (pin 1), which represent the centre of the window and the (window width)/2 respectively.

The voltage window range is from $V_{WM} - 1/2V_{WW}$ to $V_{WM} + 1/2V_{WW}$. A variable input voltage $V_{AFC\ IN}$ (pin 15) is compared with these window edges.

Table 1 Truth table; window detector

inputs	outputs	
$V_{AFC\ IN} = V_{15-16}$; $V_{WM} = V_{2-16}$; $V_{WW} = V_{1-16}$	V_{12-16}	V_{13-16}
$V_{AFC\ IN} < V_{WM} - 1/2V_{WW}$	HIGH	LOW
$V_{WM} - 1/2V_{WW} < V_{AFC\ IN} < V_{WM} + 1/2V_{WW}$	HIGH	HIGH
$V_{AFC\ IN} > V_{WM} + 1/2V_{WW}$	LOW	HIGH

Where: V_{12-16} = tuning too low (TTL); V_{13-16} = tuning too high (TTH).

During transitions of the outputs (V_{12-16} and V_{13-16}), a hysteresis value of approximately 20 mV is applied at the window edges.

Band-switch selector (see Table 2)

Selection of the band switches is determined by the input voltage levels of MSB (pin 4) and LSB (pin 5).

- If MSB or LSB $>$ 4 V, the input is HIGH
- If MSB or LSB $<$ 0,8 V, the input is LOW.

The band switches are selected as confirmed by Table 2.

Table 2 Truth table; band switch selector

MSB (V_{4-16})	LSB (V_{5-16})	switch	HIGH output
HIGH	HIGH	I	V_{10-16}
HIGH	LOW	II	V_{9-16}
LOW	HIGH	III	V_{7-16}
LOW	LOW	IV	V_{6-16}

Short-circuit protected band switches

A selected band switch has a minimum output voltage of $V_P - 0{,}3$ V provided the current is not more than 35 mA (I_{10}, I_9, I_7, I_6). If the output voltage at pins 10, 9, 7 or 6 is less than 9 V a short-circuit condition exists, and the output current will not be more than 80 mA. In this event the band switch is switched off, after an externally determined delay.

Muting

The muting circuit is active when a selected band switch is switched off. Both outputs TTL (pin 12) and TTH (pin 13) will then be LOW.

FUNCTIONAL DESCRIPTION (continued)

Delay circuit

After selection of a band switch, it will be in a conducting state. If after selection and a delay, the output voltage has not reached 9 V, the band is switched off. This delay is determined by an external capacitor on output SW_{DE} (pin 3).

Short-circuit protection

The short-circuit protection of each switch is provided by a flip-flop. If the condition of a band switch $V_O < 9$ V is detected, its flip-flop will be set and the band switch is switched off.

In the event of an incidental short-circuit to a band switch output, the band switch can be reset by applying 0 V to the power-on reset input (pin 11) or 0 V to the switch delay output SW_{DE} (pin 3).

Power-on reset

Before the voltage supply reaches 9,6 V, the short-circuit protection flip-flops are reset to enable the selection of a band switch.

The power-on reset circuit also supplies the voltage level for short-circuit detection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2 V
Total power dissipation	P_{tot}	see Fig. 2	
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

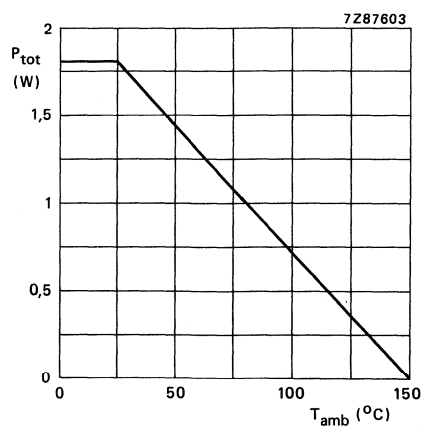


Fig. 2 Power derating curve.

CHARACTERISTICS

$V_P = V_{8-16} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 8)	$V_P = V_{8-16}$	10	12	13,2	V
Supply current (pin 8)					
unloaded band switches ON	$I_P = I_8$	18	25	38	mA
all band switches OFF	$I_P = I_8$	9	12	16	mA
Voltage range					
$1/2V_{WW}$ (pin 1)	V_{1-16}	0,1	–	4,5	V
V_{WM} (pin 2)	V_{2-16}	1,8	–	10,5	V
$V_{WM} + 1/2V_{WW}$ at $V_{8-16} - 1,4$ V	$V_{2-16} \pm V_{1-16}$	1,7	–	10,6	V
$V_{AFC\ IN}$ (pin 15)	V_{15-16}	0,5	–	11,5	V
Input current					
$1/2V_{WW}$ (pin 1)	$-I_1$	–	–	2	μA
V_{WM} (pin 2)	I_2	–	–	0,2	μA
$V_{AFC\ IN}$ (pin 15)	I_{15}	–	0,2	0,4	μA
Hysteresis voltage V_{AFC}*	ΔV_{15-16}	–	20	50	mV
Delta current at $V_{AFC\ IN}$*	ΔI_{15}	–	–	25	nA
Temperature coefficient $I_{AFC\ IN}$	$TC(I_{15})$	–	–0,42	–	nA/°C
Temperature coefficient I_{WM}	$TC(I_2)$	–	–0,27	–	nA/°C
Deviation of applied voltage (pin 1)					
at $V_{1-16} = 100$ mV	ΔV_{1-16}	–35	–	+35	mV
at $V_{1-16} = 4,0$ V; $V_{2-16} = 6$ V	ΔV_{1-16}	–200	–	+200	mV
Input current (pin 4)					
at MSB $< 0,8$ V	I_4	–	–	0,1	μA
at MSB > 4 V	I_4	–	–	1,0	μA
Input current (pin 5)					
at LSB > 4 V	I_5	–	–	1,0	μA
at LSB $< 0,8$ V	I_5	–	–	0,1	μA
Voltage level (pin 4)					
at MSB HIGH	V_{4-16}	4	–	–	V
at MSB LOW	V_{4-16}	–	–	0,8	V
Voltage level (pin 5)					
at LSB HIGH	V_{5-16}	4	–	–	V
at LSB LOW	V_{5-16}	–	–	0,8	V
Short-circuit current of band switches I, II, III, IV (pins 10, 9, 7, 6)	$-I_{10, 9, 7, 6}$	35	50	80	mA
Voltage drop of band switches I, II, III, IV (pins 10, 9, 7, 6) at $I_{o(max)} = 35$ mA; $V_P = 10$ V	$V_{10, 9, 7, 6-16}$	–	–	0,3	V

* During switching of outputs V_{12-16} and/or V_{13-16}.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Voltage level short-circuit detection at 0,75V_P	$V_{10, 9, 7, 6\text{-}16}$	8,0	9,0	9,5	V
Output voltage (pin 13) TTH at I_{13} = 2 mA (LOW)	$V_{13\text{-}16}$	–	–	0,3	V
Output voltage (pin 12) TTL at I_{12} = 2 mA (LOW)	$V_{12\text{-}16}$	–	–	0,3	V
Leakage current (pin 13) TTH at $V_{13\text{-}16}$ = 13,2 V	I_{13}	–	–	10	μA
Leakage current (pin 12) TTH at $V_{12\text{-}16}$ = 13,2 V	I_{12}	–	–	10	μA
Output current (pin 3) SW_{DE} at $V_{3\text{-}16}$ = 6 V	$-I_3$	5	12	20	μA
Maximum value of delay capacitor	C_3	–	–	40	nF
Maximum delay time at ± C_3 (nF)/(I_3/10) ms	t_d	–	–	50	ms
Power-on-reset voltage	$V_{8\text{-}16}$	6	–	9,6	V
Leakage current unswitched band switches at $V_{10, 9, 7, 6\text{-}16}$ = −12 V	$I_{10, 9, 7, 6}$	–	–	5	μA

STEREO/DUAL TV SOUND DECODER CIRCUIT

GENERAL DESCRIPTION

The TDA3803A is a stereo/dual TV sound decoder circuit with static switching for processing two AF signals in TV and VCR equipment. The LOW/HIGH static switching signals control the AF output selector. Two operational amplifiers perform bandpass filtering of the identification signals.

Features

- Amplification of the two AF input signals by integrated operational amplifiers
- Low distortion stereo de-matrix
- All operational amplifiers offset compensated
- De-emphasis with operational amplifiers, preferably applied to the output terminals
- Two output ports each with two channels for headphones and loudspeakers
- Dual sound information at one port, each port individually switchable from sound I to sound II and sound II to sound I
- Mute function; while mute is active, it is possible to connect an external mono AF input signal to pin 10 appearing at pins 20 to 23.
- Identification without additional signals (horizontal etc.)

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-12}$	typ.	12 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	28 mA
Pilot carrier amplifier gain control range	ΔG_v	>	40 dB
AF input signals; at G_v = 0 dB (r.m.s. value)	$V_{i(rms)}$	=	1 V
LED output current	I_{LED}	typ.	12 mA
Weighted signal-to-noise ratio of the a.f. signal switches (CCIR468/2)	(S+N)/N	⩾	60 dB
Crosstalk in stereo mode	α_S	>	40 dB
Crosstalk in dual sound mode	α_{DS}	>	60 dB

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

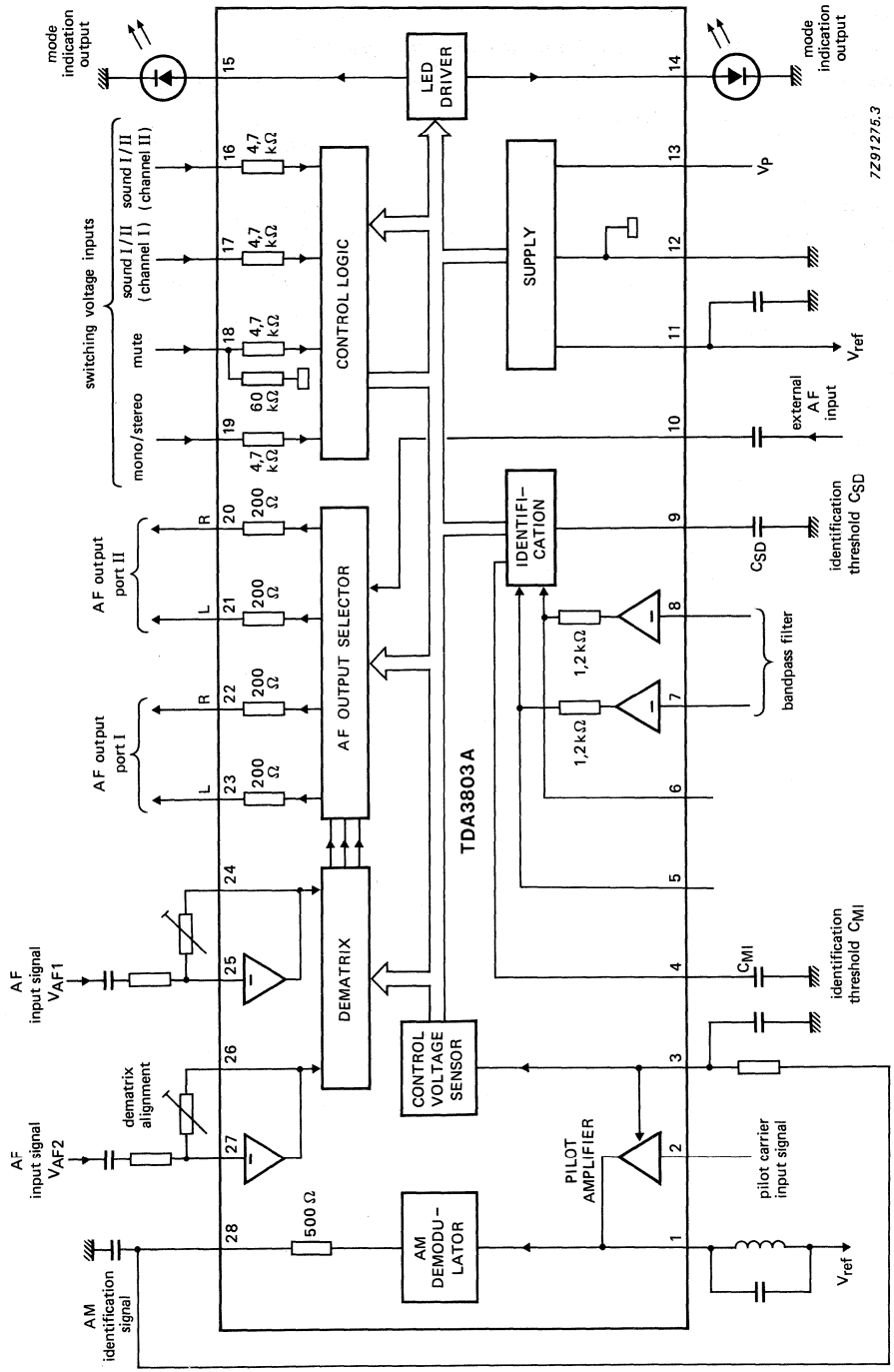


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-12}$	max.	14 V
Voltages with respect to pin 12 (ground) pins 25; 27 and 28	$V_{25;27;28-12}$	max.	V_P
Voltages			
pin 1 to pin 10	V_{n-12}	max.	V_P
pin 14 to pin 19	V_{n-12}	max.	V_P
Currents			
pin 11	I_{11}	max.	3 mA
pins 20; 21; 22; 23	$I_{20;21;22;23}$	max.	10 mA
pin 28	$-I_{28}$	max.	3 mA
Total power dissipation	P_{tot}	max.	1,5 W
Storage temperature range	T_{stg}		−25 to +125 °C
Operating ambient temperature range	T_{amb}		0 to +70 °C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; overall voltage gain (G_v) = 1; ($R_S = R_R$); measured in Fig. 2 with a 1 kHz signal. AF input AF2 = AF1 = 0,5 V, pilot carrier input signal $V_{2\text{-}12(rms)}$ = 16 mV, m = 0,5 and with adjusted de-matrix circuit; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13\text{-}12}$	10,8	12	13,2	V
Supply current (without LED current)	$I_P = I_{13}$	–	28	35	mA
Reference voltage (pin 11)	V_{ref}	–	6	–	V
Input resistance (dynamic)	$R_{11\text{-}12}$	–	4	–	kΩ
AF part					
Amplification	G_v	–40	–	18	dB
Input signal at G_v = 1	$V_{AF1} = V_{AF2}$	–	–	1	V
Mono AF input signal (pin 10)*					
Input signal	$V_{10\text{-}12}$	–	–	2	V
DC input voltage level	$V_{10\text{-}12}$	–	6	–	V
Input resistance	$R_{10\text{-}12}$		16	–	kΩ
Stereo mode AF output port I pin 22: right pin 23: left					
AF output port II pin 20: right pin 21: left					
Output signal (THD ⩽ 0,5%)					
port I ($V_{23\text{-}12} = V_{22\text{-}12}$)	V_{oI}	–	–	2	V
port II ($V_{21\text{-}12} = V_{20\text{-}12}$)	V_{oII}	–	–	2	V
Weighted signal-to-noise ratio of the AF signal switches (in accordance with CCIR468/2)	(S+N)/N		65	–	dB
Unweighted signal-to-noise	(S+N)/N	60	–	–	dB
Total harmonic distortion ($V_{20;21;22;23\text{-}12}$ = 0,5 V; G_v = 1)	THD	–	0,05	–	%
Crosstalk attenuation (selective)					
stereo mode (f_1 = 1 kHz; f_2 = 400 Hz)	α_S	40	–	–	dB
dual sound mode (f = 250 Hz to 12,5 kHz)	α_{DS}	60	–	–	dB

* An input signal at pin 10 appears at pins 20 to 23 if the mute input (pin 18) is activated ($V_{18\text{-}12} \geqslant 2$ V).

parameter	symbol	min.	typ.	max.	unit
DC input voltage level at pins 25 and 27	$V_{25;27\text{-}12}$	–	6	–	V
DC output voltage level at pins 20; 21; 22 and 23	$V_{n\text{-}12}$	–	6	–	V
Output resistance at pins 20; 21; 22 and 23	$V_{n\text{-}12}$	–	200	–	Ω
Identification part					
Pilot carrier amplifier					
input signal (pin 2)	$V_{2\text{-}12}$	5	–	–	mV
gain control range	ΔG_v	40	–	–	dB
controlled output signal (pin 1) (peak-to-peak value)	$V_{1\text{-}12(p\text{-}p)}$	–	300	–	mV
Input resistance (pin 2)	$R_{2\text{-}12}$	–	60	–	kΩ
Output resistance (pin 1)	$R_{1\text{-}12}$	1	–	–	MΩ
DC input voltage level (pin 2) applied externally (see Fig. 2)	$V_{2\text{-}12}$	–	6	–	V
DC output voltage level (pin 28)					
without gain control	$V_{28\text{-}12}$	–	6	–	V
with gain control	$V_{28\text{-}12}$	–	7,9	–	V
Identification signal (pin 28) (peak-to-peak value)	$V_{28\text{-}12(p\text{-}p)}$	–	2,0	–	V
Filter operational amplifiers open loop gain	G_o	78	–	–	dB
Identification frequency evaluation					
No identification signal (lower threshold)	$V_{4\text{-}12}$	–	–	2,5	V
Identification signal (upper threshold)	$V_{4\text{-}12}$	4,7	–	–	V
Stereo transmission (lower threshold)	$V_{9\text{-}12}$	–	–	2,5	V
Dual sound transmission (upper threshold)	$V_{9\text{-}12}$	4,7	–	–	V
Control logic part					
Mute input voltage (pin 18)					
mute OFF	$V_{18\text{-}12}$	–	–	0,8	V
mute ON (see the remarks to pin 10)	$V_{18\text{-}12}$	2	–	–	V
Switching stereo/mono and sound I/sound II					
Stereo transmission					
switching voltage to pin 19 (pin 17 and 16 not affected)					
output ports I and II mono	$V_{19\text{-}12}$	–	–	0,8	V
output ports I and II stereo	$V_{19\text{-}12}$	2	–	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Control logic part (continued)					
Mono transmission both output ports I and II mono					
Dual sound transmission					
switching voltage to pin 16 (pin 19 and 17 not affected)					
output port II sound I	$V_{16\text{-}12}$	2	–	–	V
output port II sound II	$V_{16\text{-}12}$	–	–	0,8	V
switching voltage to pin 17 (pin 16 and 19 not affected)					
output port I sound I	$V_{17\text{-}12}$	–	–	0,8	V
output port I sound II	$V_{17\text{-}12}$	2	–	–	V
Mode indication (pins 14 and 15; see also Table 1)					
Output current	$-I_{14;\ 15}$	9	12	15	mA
Output voltage (note 2)	$V_{14;\ 15\text{-}12}$	0	–	8	V
Stereo/mono transmission: LED indication is valid for the transmission mode					
Dual sound transmission: LED indication is valid for port I					

Table 1 Mode indication (note 1)

transmission mode	LED pin 15	LED pin 14
mono	OFF	OFF
stereo:		
stereo selection; $V_{19\text{-}12} \geqslant 2$ V	ON	ON
mono selection; $V_{19\text{-}12} \leqslant 0{,}8$ V	ON	ON
dual sound:		
sound I selection; $V_{17\text{-}12} \leqslant 0{,}8$ V	ON	OFF
sound II selection; $V_{17\text{-}12} \geqslant 2$ V	OFF	ON

Notes to the characteristics

1. With mute (pin 18) ON both LEDs (pin 14 and 15) are switched OFF.
2. Pin 14 and 15 are also suitable as output switches to control TDA3810.
   At LED OFF and $I_{14,\ 15} \leqslant 100\ \mu A$, then $V_{14,\ 15\text{-}12} \leqslant 200$ mV.

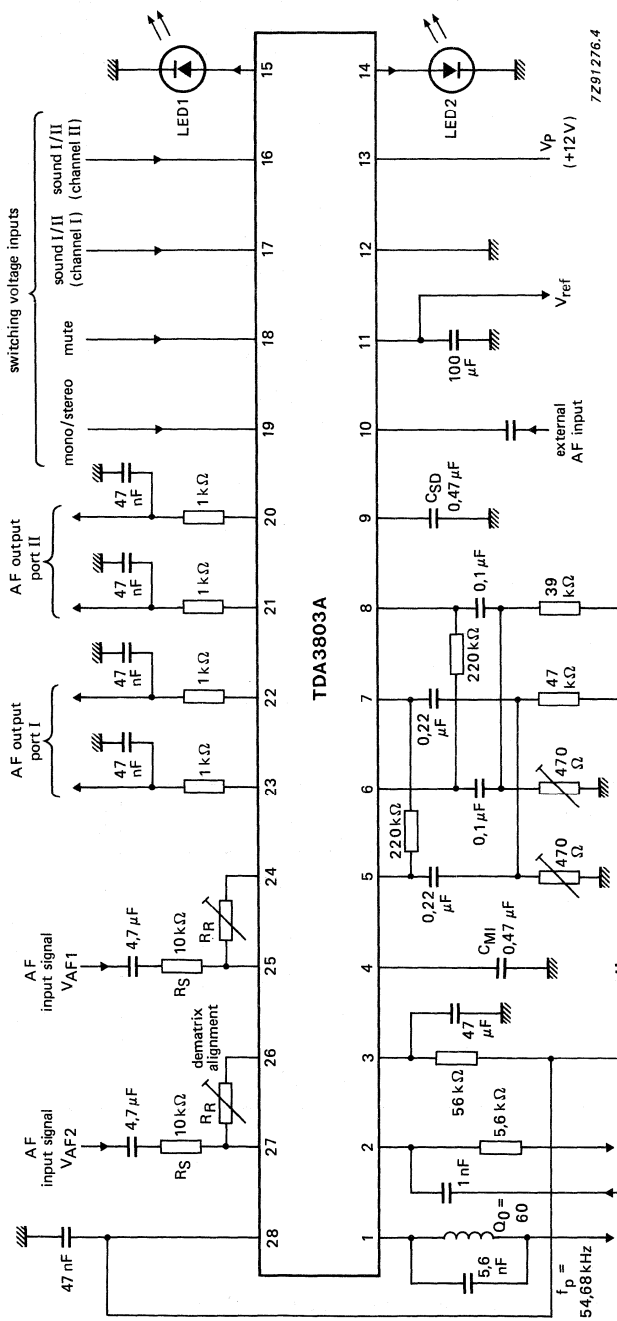


Fig. 2a Application diagram and test circuit; external components.

APPLICATION INFORMATION (continued)

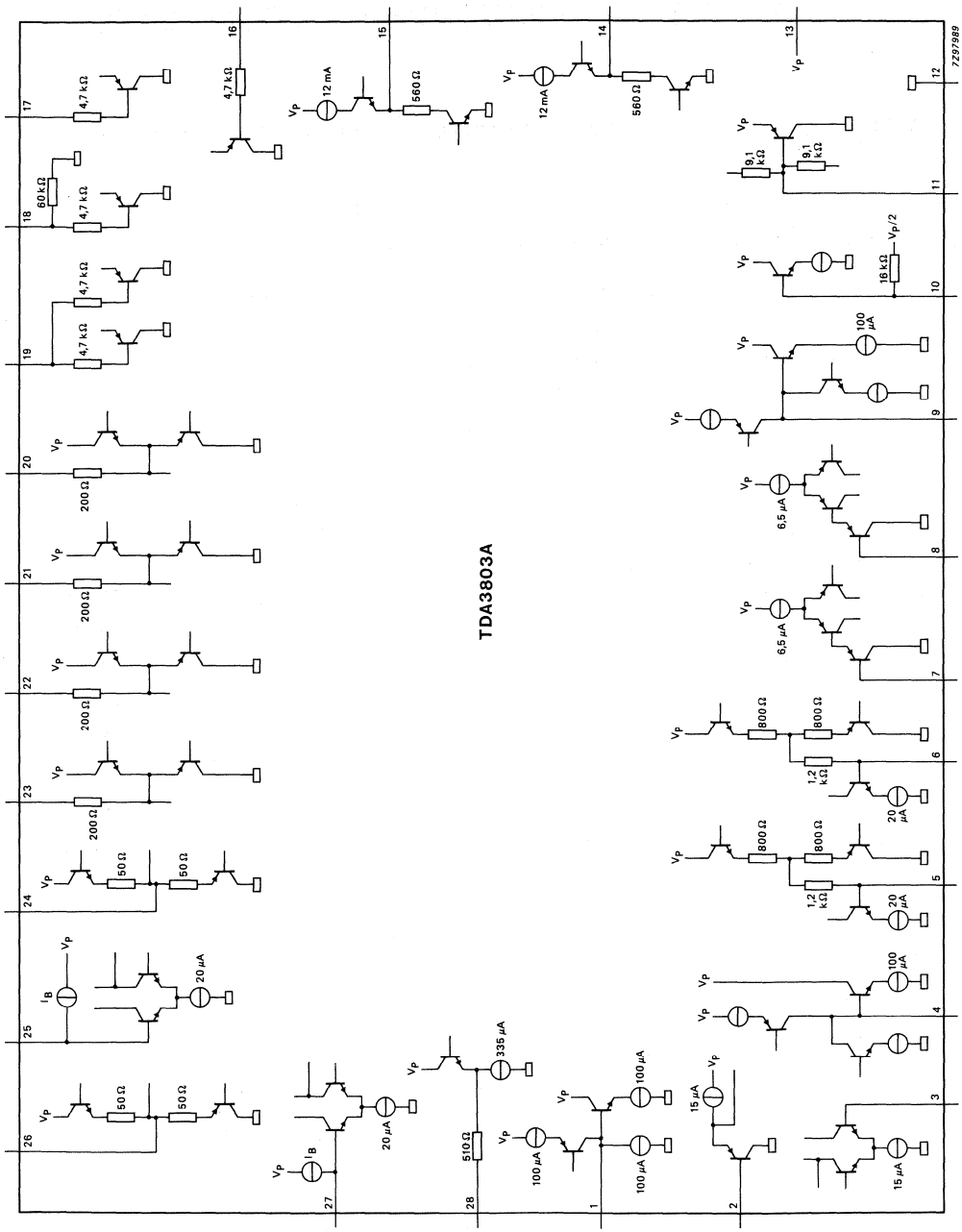


Fig. 2b Application diagram and test circuit; part of internal circuitry.

SPATIAL, STEREO AND PSEUDO-STEREO SOUND CIRCUIT

The TDA3810 integrated circuit provides spatial, stereo and pseudo-stereo sound for radio and television equipment.

Features

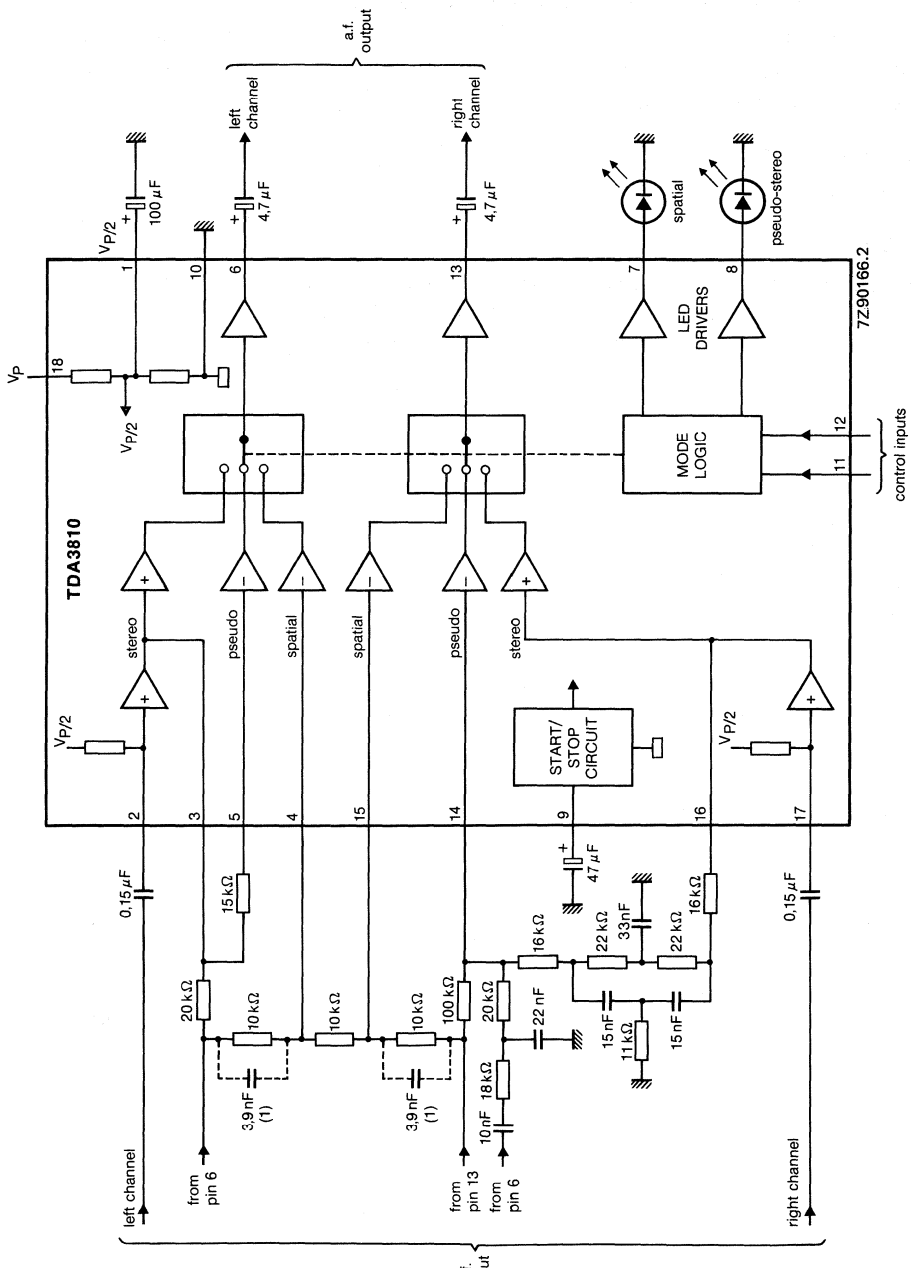
- Three switched functions: spatial (widened stereo image)
  stereo
  pseudo-stereo (artificial stereo from a mono source)
- Offset compensated operational amplifiers to reduce switch noise
- LED driver outputs to facilitate indication of selected operating mode
- Start/stop circuit to reduce switch noise and to prevent LED-flicker
- TTL-compatible control inputs

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_P	typ.	12	V
Supply current (LEDs off)	I_P	typ.	6	mA
Operating ambient temperature range	T_{amb}	0 to	+70	°C
Input signal (r.m.s. value)	$V_{i(rms)}$	<	2	V
Total harmonic distortion (stereo)	THD	typ.	0,1	%
Channel separation (stereo)	α	typ.	70	dB
Gain (stereo)	G_v	typ.	0	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Used in spatial mode for correction of high frequency only (optimal performance).

Fig. 1 Block diagram/test circuit showing external components; for control inputs to pins 11 and 12 see truth table.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_P	max.	18 V
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; test circuit Fig. 1 stereo mode (pin 11 to ground) unless otherwise specified. Output load: $R_{6\text{-}10,13\text{-}10} \geqslant 4{,}7$ kΩ; $C_{6\text{-}10,13\text{-}10} \leqslant 150$ pF.

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 18)	V_P	4,5	–	16,5	V
Supply current	I_P	–	6	12	mA
Reference voltage	V_S	5,3	6	6,7	V
Input voltage (pin 2 or 17) THD = 0,2% (stereo mode)	$V_{i(rms)}$	–	–	2	V
Input resistance (pin 2 or 17)	R_i	50	75	–	kΩ
Voltage gain V_o/V_i	G_v	–	0	–	dB
Channel separation (R/L)	α	60	70	–	dB
Total harmonic distortion f = 40 to 16 000 Hz; $V_{o(rms)}$ = 1 V	THD	–	0,1	–	%
Power supply ripple rejection	RR	–	50	–	dB
Noise output voltage (unweighted) left and right output	$V_{n(rms)}$	–	10	–	μV
SPATIAL MODE (pins 11 and 12 HIGH) Antiphase crosstalk	α	–	50	–	%
Voltage gain	G_v	1,4	2,4	3,4	dB

PSEUDO-STEREO MODE

The quality and strength of the pseudo-stereo effect is determined by external filter components.

parameter	symbol	min.	typ.	max.	unit
CONTROL INPUTS (pins 11 and 12)					
Input resistance	R_i	70	120	–	kΩ
Switching current	$-I_i$	–	35	100	μA
LED DRIVERS (pins 7 and 8)					
Output current for LED	$-I_o$	10	12	15	mA
Forward voltage	V_F	–	–	6	V

Truth table

mode	control input state		LED spatial pin 7	LED pseudo pin 8
	pin 11	pin 12		
Mono pseudo-stereo	HIGH	LOW	off	on
Spatial stereo	HIGH	HIGH	on	off
Stereo	LOW	X	off	off

LOW = 0 to 0,8 V (the less positive voltage)
HIGH = 2 V to 5,5 V (the more positive voltage)
X = don't care

SINGLE FM TV-SOUND DEMODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA3825 is a single FM demodulator system with external AF input and mute.

Features

- Supply voltage range from 4.5 V to 13.2 V
- AC coupled AF stage
- Multiple input AF operational amplifier with offset compensation
- External AF input
- High AF output voltage with low distortion
- AF gain of 0 dB without external components
- Frequency response can be determined by external components
- High ripple rejection
- Low switching noise between AF and mute

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Supply current (pin 11)						
	V_P = 5.0 V	I_P	–	16	–	mA
	V_P = 12 V	I_P	–	18	–	mA
FM demodulator						
AF output voltage (pin 5) (RMS value)	Δf = 50 kHz; Q_B = 11	V_{5-1}	–	0.5	–	V
Signal plus weighted-noise to weighted-noise ratio		(S + W)/W	65	70	–	dB
Total harmonic distortion		THD	–	0.3	0.5	%
Source selector						
AF output voltage (pin 12) (RMS value)	THD $\leqslant$ 0.1%; V_u = 6 dB	V_{12-1}	–	1.0	–	V

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

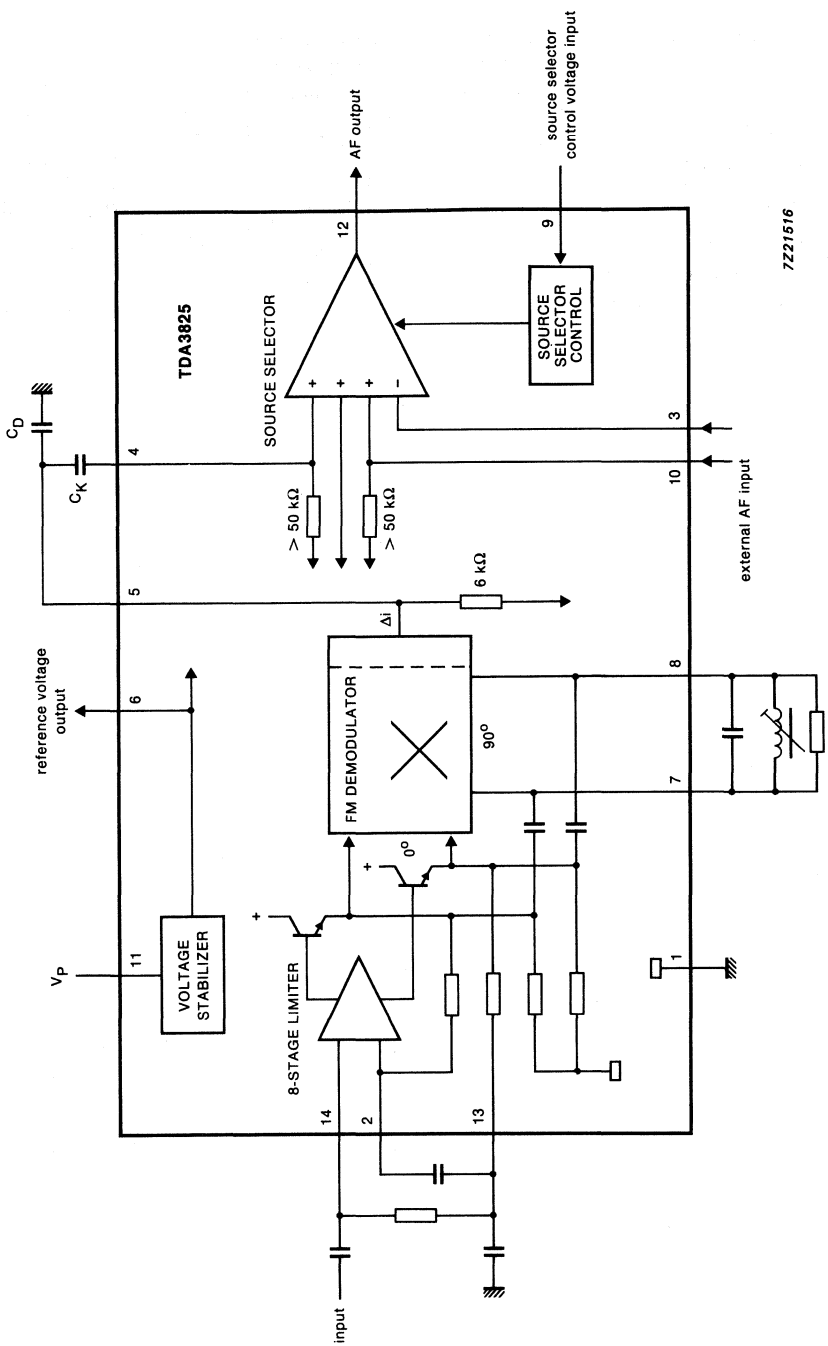


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 11)		V_P	4.5	13.2	V
External DC load resistance		R_L	5	–	kΩ
Total power dissipation		P_{tot}	–	400	mW
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; V_i = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; all parameters were measured with the test circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Total current consumption		I_{tot}	–	16	20	mA
Limiting amplifier						
Input voltage (pin 14) (RMS value)		V_{14-1}	–	–	200	mV
	3 dB signal reduction	V_{14-1}	–	–	50	μV
DC voltages						
pin 2		V_{2-1}	–	2	–	V
pin 13		V_{13-1}	–	2	–	V
pin 14		V_{14-1}	–	2	–	V
Input resistance		R_{14-13}	15	–	–	kΩ
Input capacitance		C_{14-13}	–	–	6	pF
FM demodulator						
DC voltages						
pin 7		V_{7-1}	–	3.2	–	V
pin 8		V_{8-1}	–	3.2	–	V
AF output voltage (pin 5) (RMS value)	Q_B = 11	V_{5-1}	–	0.5	–	V
AM suppression	f_{AM} = 400 Hz; m = 0.3; V_i = 500 μV(rms)	α_{AM}	50	–	–	dB
Total harmonic distortion		THD	–	0.3	0.5	%
Output impedance (pin 5)		$\lvert Z_{5-1} \rvert$	–	6	–	kΩ
Signal plus weighted-noise to weighted-noise ratio	in accordance with DIN4505; CCIR468-3	(S + W)/W	65	70	–	dB
Signal plus noise-to-noise ratio	B_{noise} = 20 kHz	(S + N)/N	75	80	–	dB
Residual RF signal (pin 5) (RMS value)	2 x f_o without de-emphasis	V_{5-1}	–	30	–	mV
Ripple rejection	f_R = 70 Hz; V_R = 100 mV(p-p)	α_R	40	45	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Source selector (pin 12)						
Open loop gain		G_{ol}	50	60	–	dB
Noise output voltage (RMS value)	B_{noise} = 20 kHz	V_{12-1}	–	20	–	μV
Slew rate		$\frac{\Delta V_{12-1}}{\Delta t}$	2	–	–	V/μs
Maximum AF output voltage (RMS value)	THD ≤ 0.1%; G_v = 6 dB	V_{12-1}	1.1	–	–	V
Input impedance						
(pin 4)		$\|Z_{4-1}\|$	50	–	–	kΩ
(pin 10)		$\|Z_{10-1}\|$	50	–	–	kΩ
−1 dB small signal bandwidth		B_{af}	100	–	–	kHz
DC output current		I_{12}	–	–	1	mA
Output load capacitance		C_L	–	–	500	pF
Feedback resistor						
(pin 3 to pin 6)		R_{3-6}	–	–	10	kΩ
(pin 3 to pin 12)		R_{3-12}	0	–	–	Ω
DC output voltage		V_{12-1}	–	2.27	–	V
AF suppression for mute		α_{mute}	70	76	–	dB
Crosstalk attenuation		$\alpha_{4/10}$	64	70	–	dB
Offset voltage between any two source selector positions		V_{12-6}	–	–	50	mV
Source selector control	see Fig.3					
Source coltrol voltage (pin 9)						
Mute active						
input voltage		V_{9-1}	0	–	1/3 V_P−1	V
input current		I_9	10	–	500	μA
Input 1 active (pin 4)						
input voltage		V_{9-1}	1/3 V_P	–	2/3 V_P−0.7	V
input current		I_9	−200	–	+200	μA
Input 2 active (pin 10)						
input voltage		V_{9-1}	2/3 V_P + 0.7	–	V_P	V
input current		I_9	−600	–	−40	μA
Input voltage at pin 9 for I_9 = 0 μA		V_{9-1}	–	$\frac{V_P-0.7}{2}$	–	V
Reference source (pin 6)						
Reference voltage input		V_{ref}	2.17	2.27	2.37	V
Output current		$\|I_6\|$	–	250	–	μA

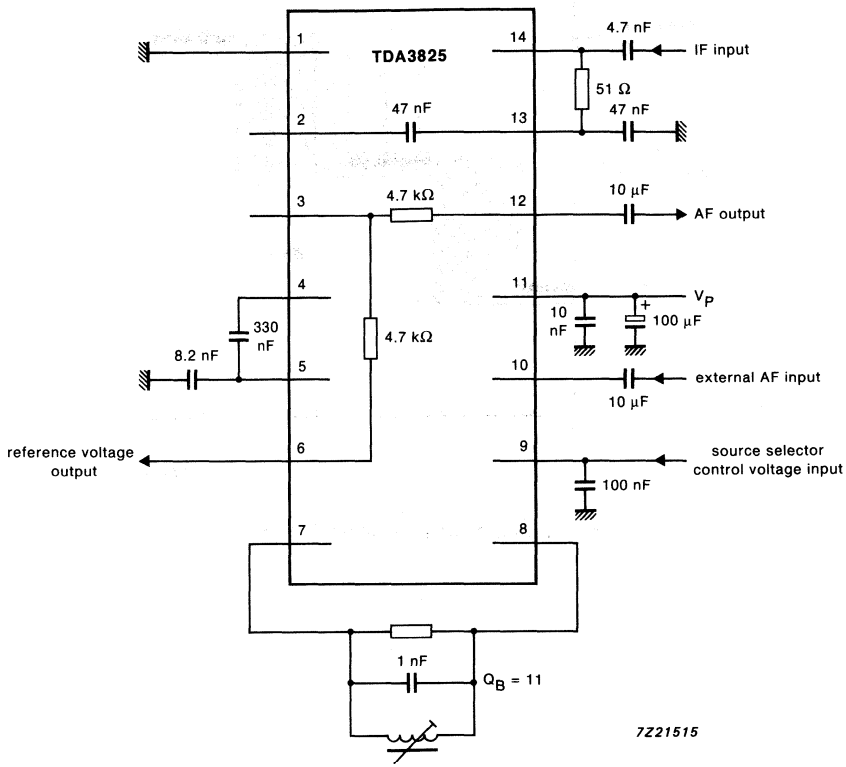


Fig. 2 Test circuit.

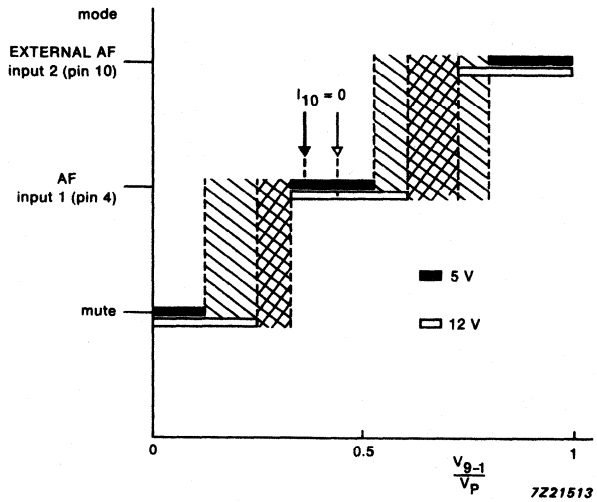


Fig. 3 Source selector logic diagram.

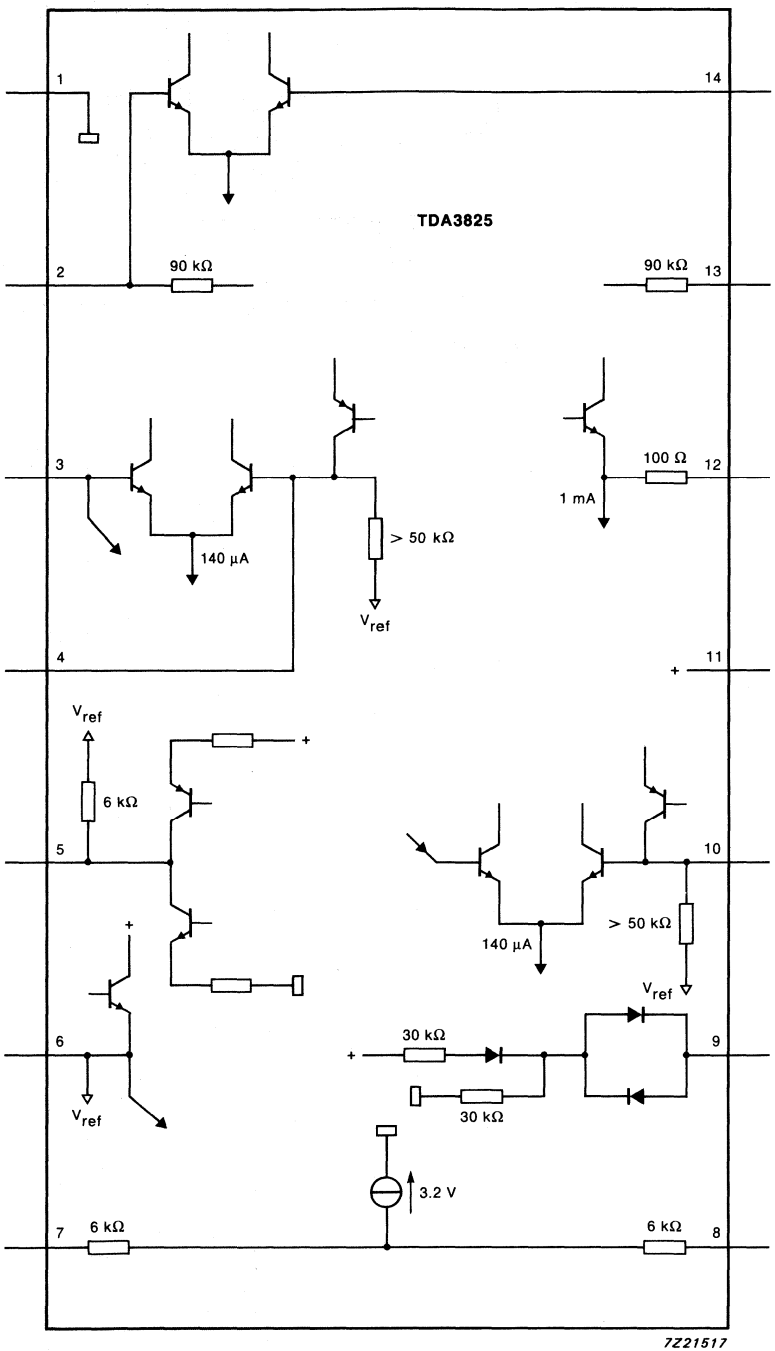


Fig. 4 Input/output loading diagram.

APPLICATION INFORMATION

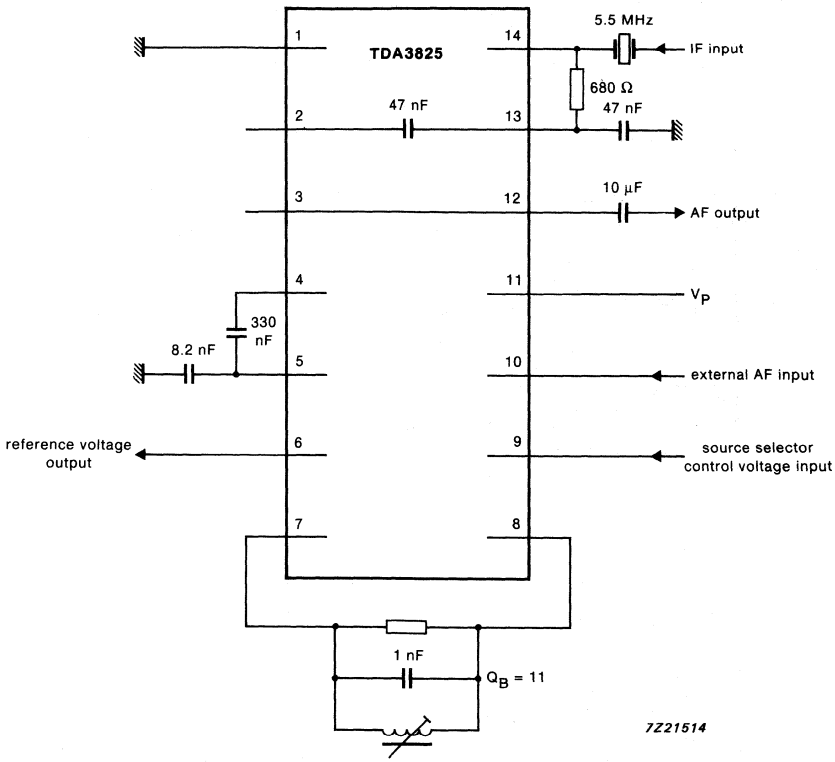


Fig. 5 Application diagram.

SINGLE FM TV-SOUND DEMODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA3826 is a single FM demodulator system with mute and 6 dB AF amplifier.

Features

- Supply voltage range from 4.5 V to 13.2 V
- AC coupled AF stage
- AF operational amplifier output with offset compensated input stage
- High AF output voltage with low distortion
- High ripple rejection
- Low switching noise between AF and mute

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Supply current (pin 11)						
	V_P = 5.0 V	I_P	–	16	–	mA
	V_P = 12 V	I_P	–	18	–	mA
FM demodulator						
AF output voltage (pin 5) (RMS value)	Δf = 50 kHz; Q_B = 11	V_{5-1}	–	0.5	–	V
Signal plus weighted-noise to weighted-noise ratio		(S + W)/W	65	70	–	dB
Total harmonic distortion		THD	–	0.3	–	%
AF switch						
AF output voltage (pin 12) (RMS value)	THD $\leqslant$ 0.1%; G_V = 6 dB	V_{12-1}	–	1.0	–	V

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

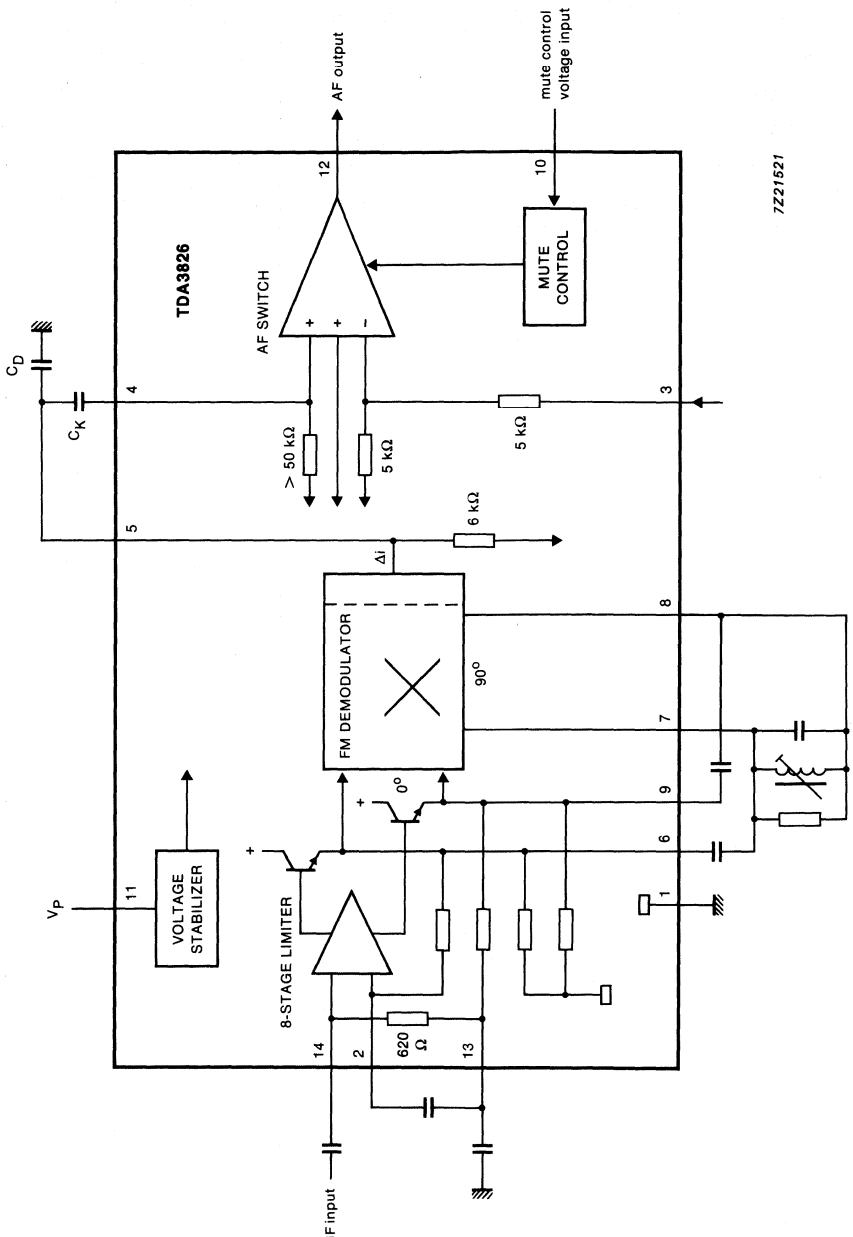


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 11)		V_P	4.5	13.2	V
External DC load resistance		R_L	5	–	kΩ
Total power dissipation		P_{tot}	–	400	mW
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; V_i = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; all parameters were measured with the test circuit of Fig. 2; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)		V_P	4.5	5.0	13.2	V
Total current consumption		I_{tot}	–	16	20	mA
Limiting amplifier						
Input voltage (pin 14) (RMS value)		V_{14-1}	–	–	200	mV
	3 dB signal reduction	V_{14-1}	–	–	50	μV
DC voltages						
pin 2		V_{2-1}	–	2	–	V
pin 13		V_{13-1}	–	2	–	V
pin 14		V_{14-1}	–	2	–	V
Input resistance		R_{14-13}	–	620	–	Ω
FM demodulator						
DC voltages						
pin 7		V_{7-1}	–	3.2	–	V
pin 8		V_{8-1}	–	3.2	–	V
AF output voltage (pin 5) (RMS value)	Q_B = 11	V_{5-1}	–	0.5	–	V
AM suppression	f_{AM} = 400 Hz; m = 0.3; V_i = 500 μV(rms)	α_{AM}	50	–	–	dB
Total harmonic distortion		THD	–	0.3	–	%
Output impedance (pin 5)		$\lvert Z_{5-1}\rvert$	–	6	–	kΩ
Signal plus weighted-noise to weighted-noise ratio	in accordance with DIN4505; CCIR468-3	(S + W)/W	65	70	–	dB
Signal plus noise-to-noise ratio	B_{noise} = 20 kHz	(S + N)/N	75	80	–	dB
Residual RF signal (pin 5) (RMS value)	2 x f_o without de-emphasis	V_{5-1}	–	30	–	mV
Ripple rejection	f_R = 70 Hz; V_R = 100 mV(p-p)	α_R	40	45	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
AF switch (pin 12)						
Open loop gain		G_{ol}	50	60	–	dB
Noise output voltage (RMS value)	B_{noise} = 20 kHz	V_{12-1}	–	20	–	μV
Slew rate		$\frac{\Delta V_{12-1}}{\Delta t}$	2	–	–	V/μs
Maximum AF output voltage (RMS value)	THD ⩽ 0.1%; G_v = 6 dB	V_{12-1}	1.1	–	–	V
Input impedance (pin 4)		$\lvert Z_{4-1}\rvert$	50	–	–	kΩ
(pin 10)		$\lvert Z_{10-1}\rvert$	50	–	–	kΩ
−1 dB small signal bandwidth		B_{af}	100	–	–	kHz
DC output current		I_{12}	–	–	1	mA
Output load capacitance		C_L	–	–	500	pF
Feedback resistor (pin 3 to pin 12)		R_{3-12}	0	–	–	Ω
DC output voltage		V_{12-1}	–	2.27	–	V
AF suppression in case of mute		α_{mute}	70	76	–	dB
Mute control	see Fig. 3					
Mute control voltage (pin 10)						
Input (pin 4) active						
input voltage		V_{10-1}	1/3 V_P	–	2/3 V_P−0.7	V
input current		I_{10}	−200	–	+200	μA
Mute active						
input voltage		V_{10-1}	0	–	1/3 V_P−1	V
input current		I_{10}	10	–	500	μA
input voltage		V_{10-1}	2/3 V_P + 0.7	–	V_P	V
input current		I_{10}	−600	–	−40	μA
Input voltage at pin 10 for I_{10} = 0 μA		V_{10-1}	–	$\frac{V_P-0.7}{2}$	–	V

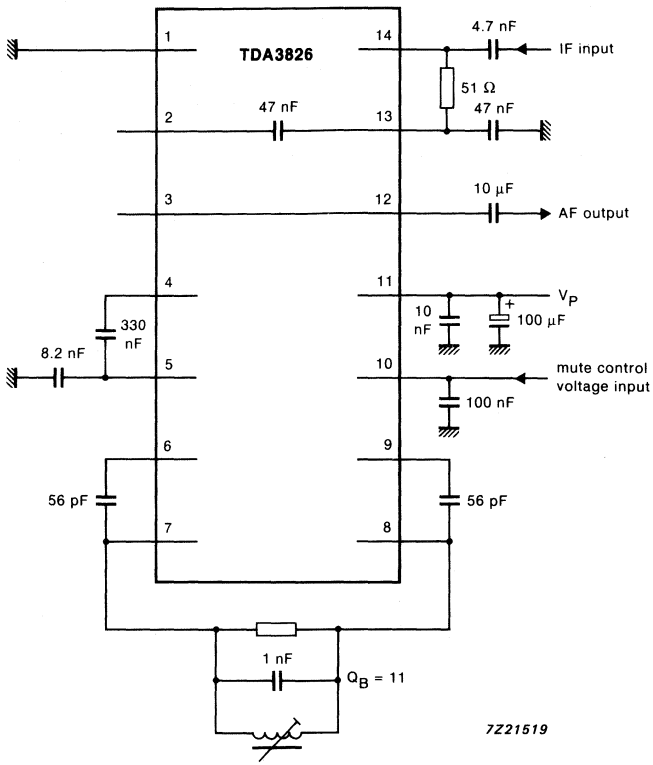


Fig. 2 Test circuit.

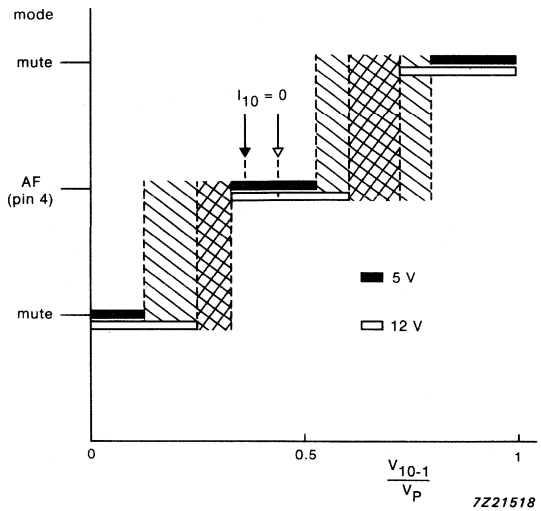


Fig. 3 Mute control logic diagram.

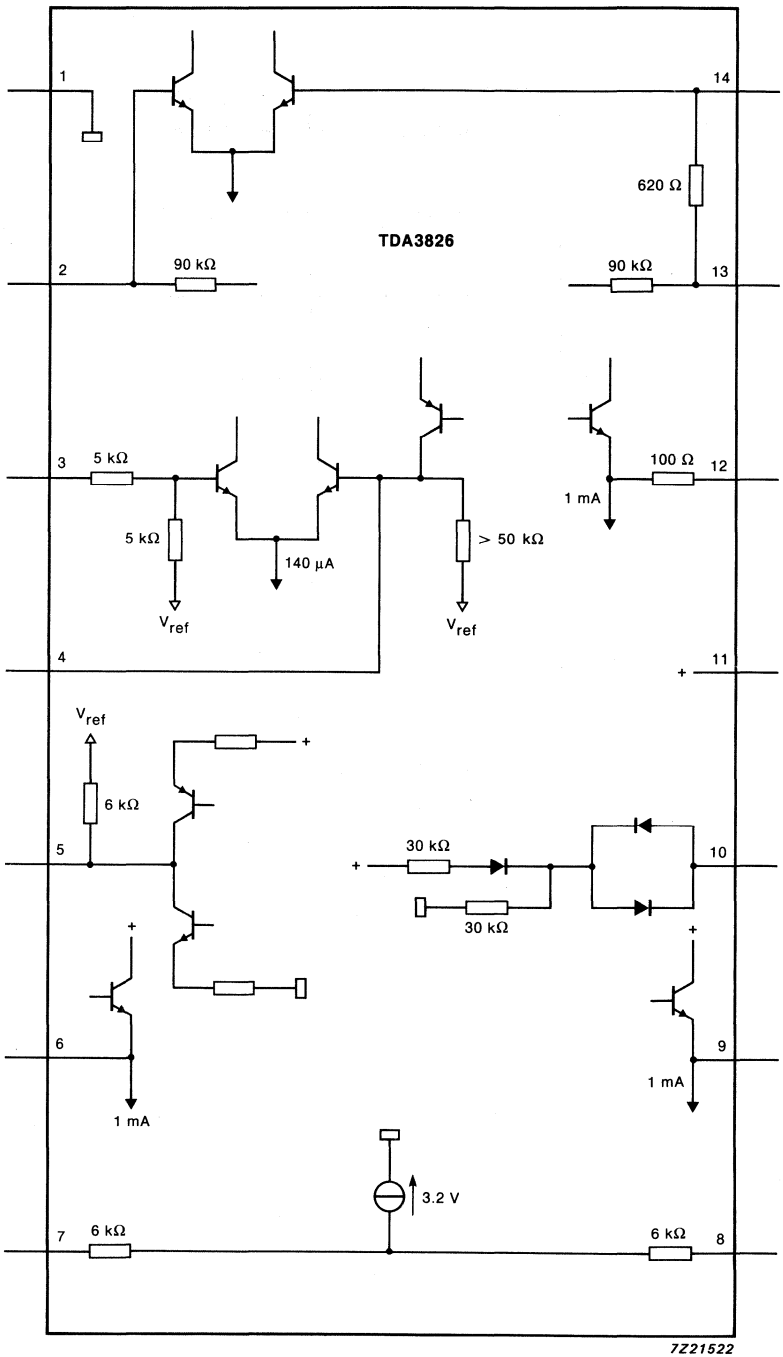


Fig. 4 Input/output loading diagram.

APPLICATION INFORMATION

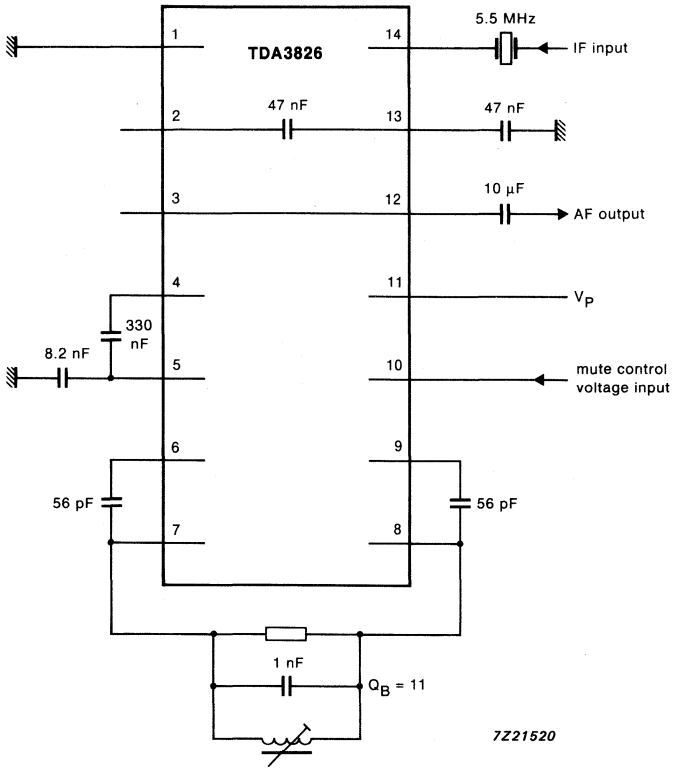


Fig. 5 Application diagram.

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA3827

TV-sound demodulator circuit with SCART switches and AF control

FEATURES

- Wide supply voltage range from 4.5 V to 13.2 V
- Wide frequency range from 4 to 12 MHz
- High ripple rejection
- High precision and temperature compensated FM-demodulator output
- Multiple-input AF operational amplifiers with offset compensation
- SCART AF input / AF output (low impedance)
- External AF input
- High-level AF output voltage with low distortion
- External selection of the source selector AF gain
- Low switching noise between AF and mute
- Wide volume-control range

GENERAL DESCRIPTION

The TDA3827 contains a single FM demodulator with SCART switches, a mute function and volume control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 18)		4.5	5.0	13.2	V
I_P	supply current (pin 18)	V_P = 5 V	–	26	–	mA
		V_P = 12 V	–	28	–	mA
(S+N)/N	signal to weighted noise		73	78	–	dB
$V_{5(rms)}$	FM demodulator output voltage (RMS value)	Δf = 50 kHz; f_{mod} = 1 kHz; Q_L = 20	450	500	550	mV
$V_{13(rms)}$	SCART output signal (RMS value)		–	1.0	–	V
G_v	volume control range		80	85	–	dB
$V_{17(rms)}$	AF output signal (RMS value)	Δf = 50 kHz; f_{mod} = 1 kHz; Q_L = 20	–	1.0	–	V
THD	total harmonic distortion (pin 17)		–	0.5	–	%

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3827	18	DIL	plastic	SOT102

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

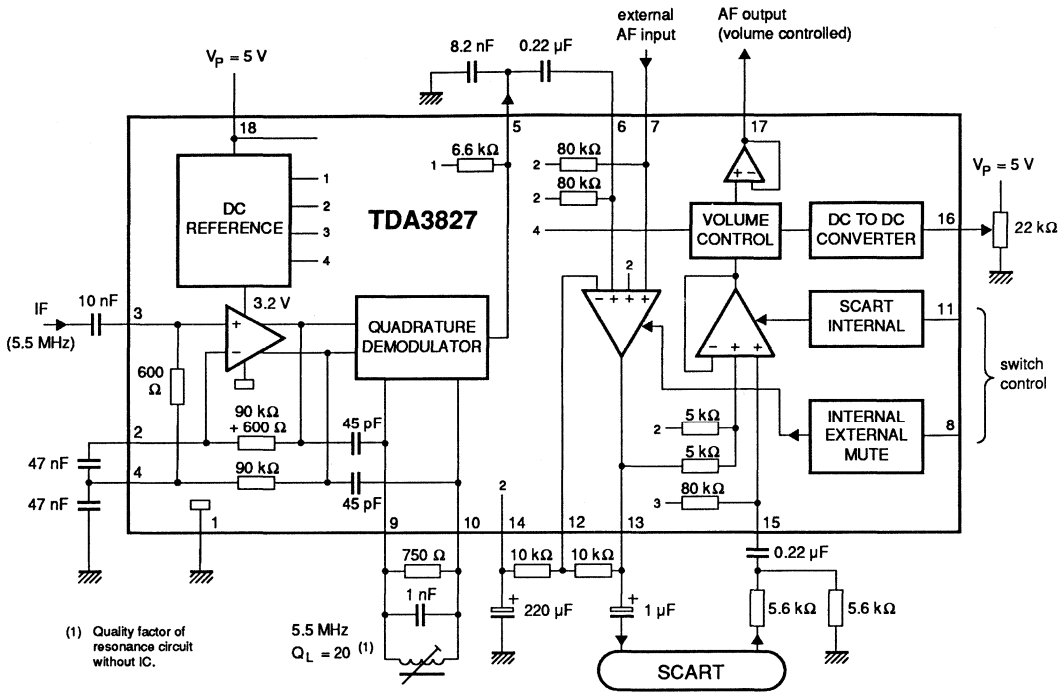


Fig.1 Block diagram.

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

PIN CONFIGURATION

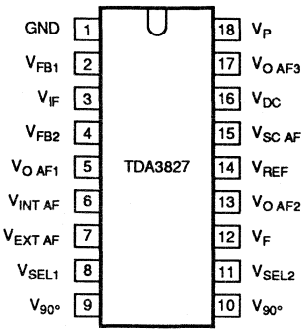


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_{FB1}	2	limiter amplifier feedback
V_{IF}	3	FM IF input signal
V_{FB2}	4	limiter amplifier feedback
$V_{O\ AF1}$	5	AF output signal
$V_{INT\ AF}$	6	internal AF input signal
$V_{EXT\ AF}$	7	external AF input signal
V_{SEL1}	8	selection voltage for internal / external AF input and mute
$V_{90°}$	9	quadrature demodulator
$V_{90°}$	10	tuned circuit reference
V_{SEL2}	11	selection voltage for internal / external or SCART audio
V_F	12	source selector feedback
$V_{O\ AF2}$	13	output signal to SCART
V_{REF}	14	reference voltage
$V_{SC\ AF}$	15	input signal from SCART
V_{DC}	16	DC volume control voltage
$V_{O\ AF3}$	17	AF output signal from volume control
V_P	18	supply voltage

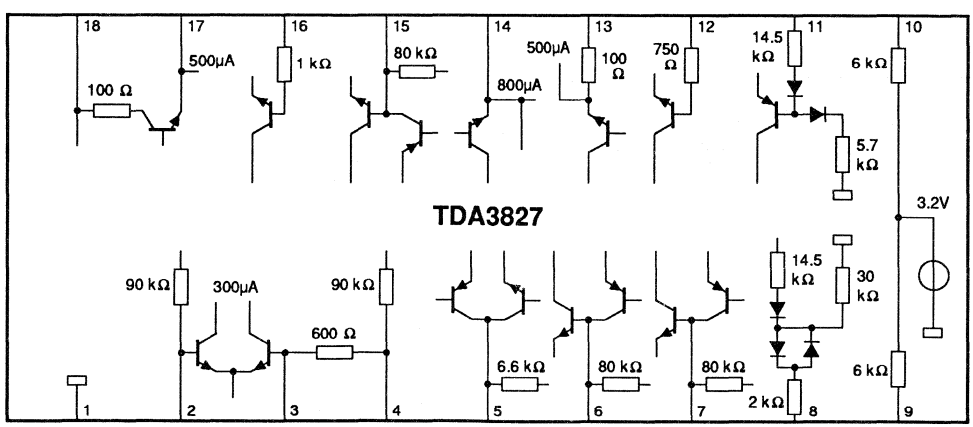


Fig.3 Internal circuits.

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)	–0.5	V_P + 6.8	V
V_{ext}	external voltage (pins 2 to 10, 12 to 15 and 17)	–0.3	V_P – 0.7	V
	external voltage at pin 11	–0.3	13.2	V
	external voltage at pin 16	–0.3	V_P	V
R_L	external DC load resistance (pin 13 and pin 17)	5.0	–	kΩ
C_L	capacitive output load (pin 13 and pin 17)	–	1500	pF
P_{tot}	total power dissipation	–	450	mW
T_{stg}	storage temperature range	–40	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
V_{ESD}	ESD-protection (note 1)	± 2000	–	V

Note to the limiting values

1. Measured with a 100 pF capacitor in series with a 1.5 kΩ resistor.

CHARACTERISTICS

All voltages are measured to GND (pin 1); V_P = 5 V; V_{IF} = 10 mV; f_o = 5.5 MHz; f_{AF} = 1 kHz; Δf = 50 kHz; T_{amb} = 25 °C; measured in test circuit of Fig.4.; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 18)		4.5	5.0	13.2	V
I_P	supply current (pin 18)	V_P = 5.0 V	–	26	30	mA
		V_P = 12.0 V	–	28	32	mA
V_{14}	reference voltage		2.2	2.3	2.4	V
I_{14}	output current		–	± 250	–	μA
IF limiting amplifier						
$V_{i(rms)}$	input signal at pin 3 (RMS value)		–	–	200	mV
		3 dB below nominal AF level at pin 5	–	30	50	μV
R_{3-1}	input resistance		–	600	–	Ω
$V_{2,3,4}$	DC voltage		–	2.1	–	V

TV-sound demodulator circuit with SCART switches and AF control

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator (Q_L = 20)						
$V_{5(rms)}$	AF-output signal (RMS value)		450	500	550	mV
	residual $2f_o$-signal (RMS value)	without de-emphasis	–	–	30	mV
TC	temperature coefficient (pin 5)		–	1	2	mV/K
α_{AM}	AM suppression	f_{AM} = 400 Hz, m = 0.3, $V_{i(rms)}$ = 500 µV; Fig.8	50	62	–	dB
THD	total harmonic distortion	see Fig.8	–	0.3	0.5	%
Z_o	output impedance (pin 5)		–	6.6	–	kΩ
B_{AF1}	small signal bandwidth (pin 5)	at –1 dB; without de-emphasis	100	–	–	kHz
(S+N)/N	signal to weighted noise ratio	CCIR468-3, DIN45405; see Fig.8	73	78	–	dB
RR	ripple rejection	f_R = 70 Hz, V_R = 100 $mV_{(p-p)}$	30	35	–	dB
$V_{9,10}$	DC voltage		–	3.2	–	V
Source selector						
$V_{i\ 6,7(rms)}$	input signal (RMS value)		–	500	1000	mV
$Z_{6,7}$	input impedance		50	80	–	kΩ
G_o	open loop gain		–	60	–	dB
$G_{13/6,7}$	gain	see Fig.4	–	0	–	dB
	gain (typical application)	see Fig.1	–	6	–	dB
V_{13}	DC voltage		–	2.3	–	V
I_{13}	DC output current		–	–	1.0	mA
Z_{13}	output impedance dynamic		–	–	10	Ω
C_L	capacitive output load (pin 13)		–	–	1500	pF
$V_{13(rms)}$	output signal (RMS value)	handling THD < 0.1 %	–	1.0	1.1	V
	noise voltage (RMS value)	B_{noise} = 20 kHz	–	20	–	µV
B_{AF2}	small signal bandwidth	at –1 dB	100	–	–	kHz
dV/dt	slew rate (pin 13)		1	–	–	V/µs
ΔV_{13}	offset-voltage between any two source selector positions		–	5	20	mV
α_{mute}	AF suppression at mute		80	90	–	dB
$\alpha_{7/6}$	crosstalk attenuation		70	76	–	dB

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Source selector control (see Fig.5)						
V_8	voltage for internal selection of AF-input (pin 6)		1/3 V_P	–	2/3 V_P –0.7	V
I_8	selection input current		–	–	200	µA
V_8	voltage for external selection of AF-input (pin 7)		2/3 V_P +0.7	–	V_P	V
I_8	selection input current		40	–	600	µA
V_8	voltage for mute active		0	–	1/3 V_P – 1	V
I_8	input current		–10	–	–500	µA
SCART switch and level control						
$V_{15(rms)}$	AC input signal (RMS value)		–	500	1000	mV
Z_{15}	input impedance		50	80	–	kΩ
$G_{17\text{-}15}$	voltage gain	V_{16} = 4.1 V	–1.5	0	+ 1.5	dB
G_{max}	maximum voltage gain	V_{16} = 5.0 V	+ 4.0	+ 5.0	+ 6.0	dB
ΔG_V	volume control range	see Fig.7	80	86	–	dB
V_{17}	DC voltage		–	2.3	–	V
I_{17}	DC output current		–	–	–1	mA
Z_{17}	dynamic output impedance		–	–	10	Ω
C_L	capacitive output load (pin 17)		–	–	1500	pF
$V_{17(rms)}$	output signal (RMS value)	THD ≤ 1 %	–	1.0	1.1	V
	noise voltage (RMS value)	B_{noise} = 20 kHz	–	100	–	µV
B_{AF3}	small signal bandwidth (pin 17)	at –3 dB	50	100	–	kHz
THD	distortion (pin 17)	at maximum gain	–	0.5	1.0	%
ΔV_{17}	offset voltage between internal and SCART		–	5	20	mV
V_{16}	control voltage	minimum gain –80 dB; see Fig.7	0.7	1.0	–	V
I_{16}	control current		–	–	50	µA
$\alpha_{6,7/15}$	crosstalk attenuation between IF-stage and control-stage	IF sound modulated; SCART switch on; source-selector on position input 1	80	90	–	dB
SCART switch control (see Fig.6)						
V_{11}	voltage for internal active		0	–	4/5 V_P –3	V
I_{11}	current		0	–	–100	µA
V_{11}	voltage for SCART active		4/5 V_P –1	–	13.2	V
I_{11}	current		$\frac{V_{11} - 1.4}{20.000}$	–	700	µA

TV-sound demodulator circuit with SCART switches and AF control

TDA3827

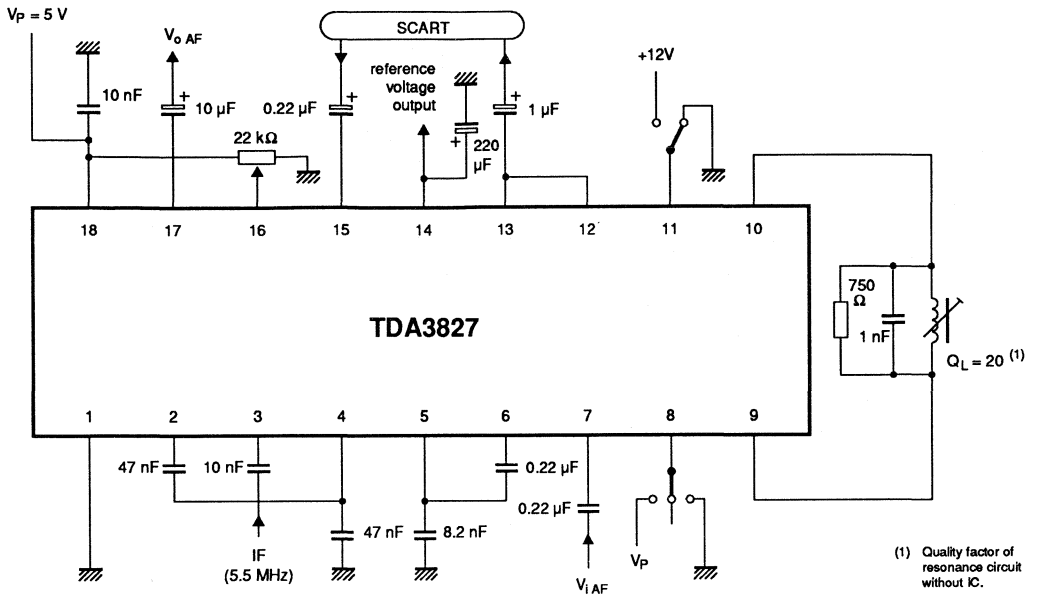


Fig.4 Test circuit.

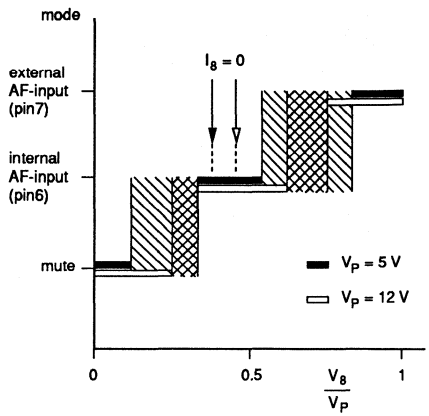


Fig.5 Source selector switching levels.

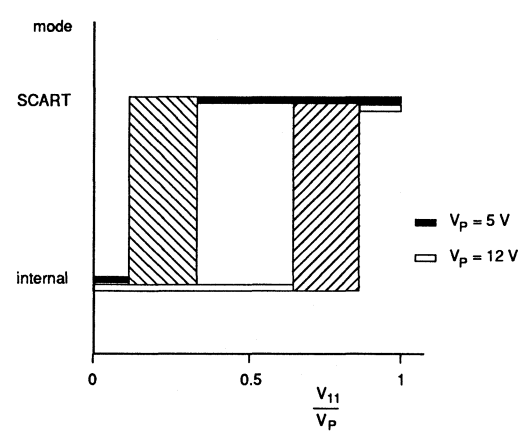


Fig.6 SCART switching levels.

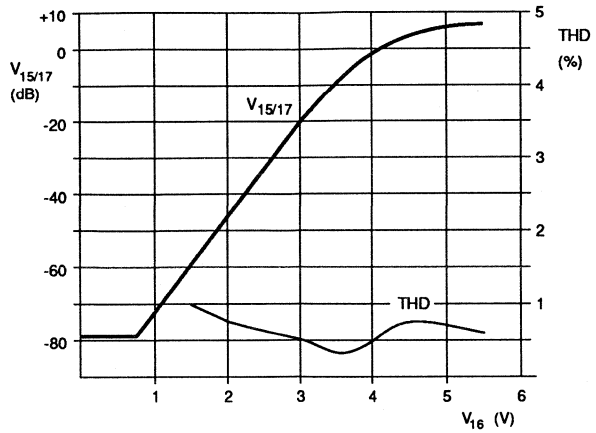


Fig.7 Volume control diagram.

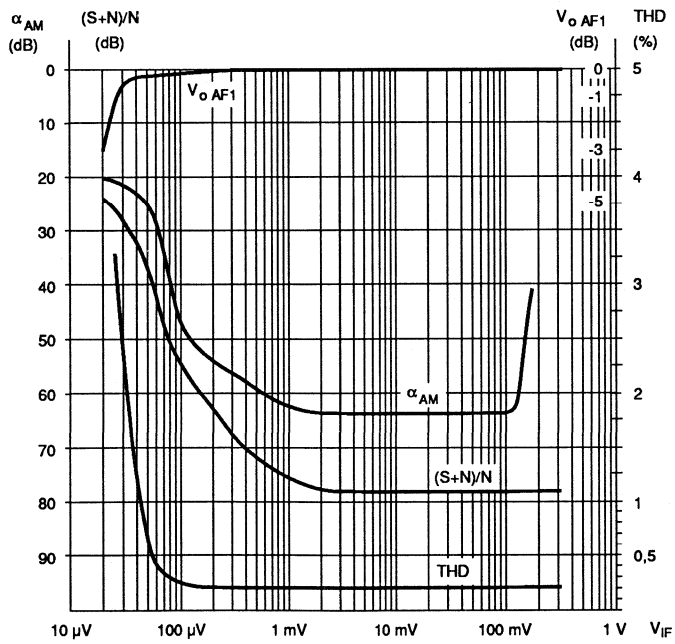


Fig.8 AF output voltage at pin 5, THD, (S+N)/N in accordance with to CCIR468-3 and AM suppression α_{AM} as functions of IF input voltage V_{IF} at pin 3.

Data sheet	
status	Preliminary specification
date of issue	January 1991

TDA3833

BTSC-stereo / SAP / DBX decoder and DBX expander

FEATURES

- DBX decoder, MPX decoder and SAP decoder on chip
- Extensive switching possibilities for the AF outputs and the extra headphone output
- Stereo and SAP signal available simultaneously
- Reliable stereo/SAP identification by means of the noise detector
- Integrated filters
- DAC control possible for most alignments
- Few external components
- Low power consumption (200 mW)
- +5 V supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 32)	-	5	-	V
I_P	supply current	-	42	-	mA
V_i	input signal, 100% modulated, mono (RMS value, pin 1)	-	100	-	mV
V_o	AF output signal (RMS value, pins 7, 23 and 24)	- -	550	-	mV
S/N(W)	signal-to-noise ratio, weighted	-	50	-	dB
S/N	signal-to-noise ratio (RMS)	-	60	-	dB
α_{CH}	stereo channel separation	-	26	-	dB
α_{CR}	crosstalk attenuation	-	60	-	dB
THD	total harmonic distortion	-	0.2	-	%

GENERAL DESCRIPTION

The TDA3833 is a sound processor for stereo/second audio programme (SAP) baseband signals in accordance with the BTSC standard for television receivers and video tape recorders.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3833	32	shrink DIL	plastic	SOT232

BTSC-stereo / SAP / DBX decoder and DBX expander

TDA3833

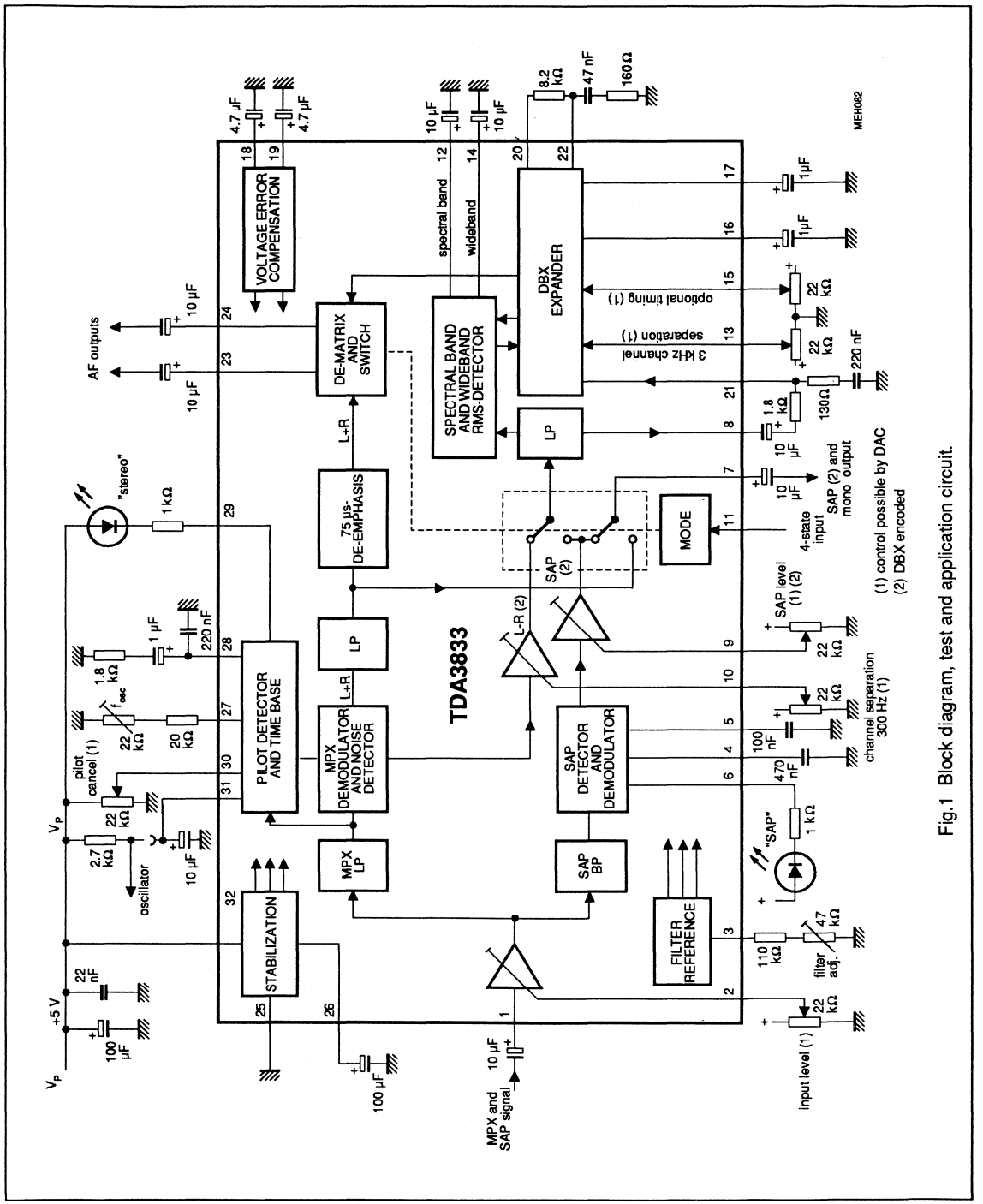


Fig.1 Block diagram, test and application circuit.

BTSC-stereo / SAP / DBX decoder and DBX expander

TDA3833

PINNING

SYMBOL	PIN	DESCRIPTION
V_i	1	composite input signal (MPX/SAP)
ILV	2	input level control
f_{ref}	3	adjustment of filter reference
C_{SAP}	4	SAP identity smoothing capacitor
C_{ND}	5	SAP noise detector smoothing capacitor
SAPI	6	SAP indicator output (sink)
$V_{o\ HP}$	7	SAP/mono headphone output
$V_{o\ SAP}$	8	output signal SAP/(L – R) without DBX
SAPLV	9	SAP level control
LRLV	10	(L – R) level control
MODE	11	4-state mode control
$C1_{SPB}$	12	spectral band timing capacitor
DBXLV	13	DBX spectral adjust
$C1_{WB}$	14	wideband timing capacitor
DBXT	15	DBX timing adjust
$C2_{SPB}$	16	spectral RMS-detector smoothing capacitor
$C2_{WB}$	17	wideband RMS-detector smoothing capacitor
$C1_{DC}$	18	DC decoupling capacitor 1 for offset compensation
$C2_{DC}$	19	DC decoupling capacitor 2 for offset compensation
EMPH1	20	time constant for variable emphasis
DBXIN	21	DBX signal input
EMPH2	22	time constant for variable emphasis
V_{oAF1}	23	AF output signal right/SAP or mono
V_{oAF2}	24	AF output signal left/SAP or mono
GND	25	ground (0 V)
C_{ref}	26	smoothing capacitor for internal reference voltage
VCO	27	VCO free running frequency adjustment
LOOP	28	phase detector loop filter
STERI	29	stereo indicator output (sink)
PILOT	30	pilot cancel adjustment
C_{pil}	31	pilot detector smoothing capacitor, VCO/4 output
V_P	32	+5 V supply voltage

PIN CONFIGURATION

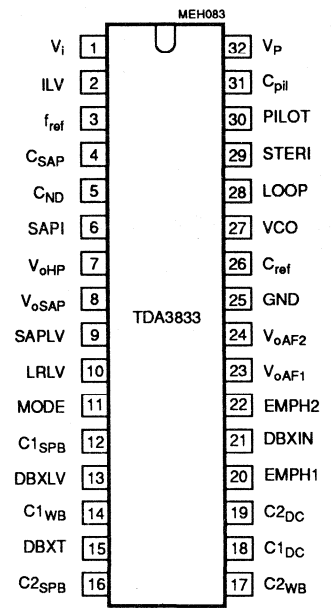


Fig.2 Pin configuration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 32)	0	8	V
V_1	composite input voltage	0	V_P	V
V_{11}	MODE input voltage	0	8	V
$I_{7, 23, 24}$	output current (AF outputs)	0	5	mA
$I_{6, 29}$	output current (indication outputs)	0	5	mA
P_{tot}	total power dissipation	0	500	mW
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling* for all pins	-	±4000	V

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; for MPX: Δf = 25 kHz for L+R (100% modulation); f_{mod} = 1 kHz; and for SAP: Δf = 10 kHz; f_{mod} = 1 kHz, unless otherwise specified. Measurements taken in Fig.1 including all adjustments.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 32)		4.75	5	5.35	V
I_P	supply current		-	42	-	mA
V_n	DC input/output voltage at pins 1, 7, 8, 18, 19, 21, 23 and 24		-	$V_P/2$	-	V
MODE select 4-state input see Table 1						
V_{11}	input voltage for mono/SAP		0	-	$V_P/2-1$	V
	input voltage for SAP		$V_P/2-0.4$	-	$V_P/2+0.4$	V
	input voltage for stereo		$V_P/2+1$	-	V_P	V
	input voltage for mono		$V_P+1.4$	-	8	V
I_{11}	input current for mono/SAP		-	-	15	µA
	input current for SAP		-	-	15	µA
	input current for stereo		-	-	5	µA
	input current for mono	V_{11} = 7.2 V	-	-	300	µA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite input, pin 1						
R_i	input resistance on pin 1		14	20	26	kΩ
V_i	input signal on pin 1 (RMS value)	note 1				
	L+R (all other signals according to BTSC system specification)		70	100	140	mV
	pilot threshold for MPX	stereo on	-	-	16	mV
		stereo off	5	-	-	mV
	hysteresis of threshold	MPX	-	2.5	-	dB
	pilot threshold for SAP	SAP on	-	-	37	mV
		SAP off	16	-	-	mV
	hysteresis of threshold	SAP	-	2	-	dB
G_v	gain control range	dependent on V_2	±5	±7.5	-	dB
V_2	control voltage range		-	1 to 4	-	V
I_2	input current pin 2	$V_2 = V_P/2$	-	-	5	µA
Voltage controlled oscillator (VCO), pin 27						
f_{VCO}	nominal VCO frequency ($4f_H$)	note 2	-	62.94	-	kHz
Δf_{29}	capture range	nominal pilot	-	-	1	kHz
TC	temperature coefficient		-	-	50	10^{-6}/K
Stereo indication output, pin 29						
V_{29}	output voltage range	stereo present	-	-	0.5	V
		stereo not present	V_P–0.5	-	V_P	V
I_{29}	output current active LOW	stereo present	3	-	-	mA
SAP/Mono output, pin 7						
V_o	output signal (RMS value, pin 7)	note 3	-	550	-	mV
	output signal headroom	mono	-	9.5	-	dB
R_7	output resistance		-	100	200	Ω
R_L	load resistance		10	-	-	kΩ
C_L	load capacitance		-	-	500	pF
THD	total harmonic distortion	SAP signal	-	0.5	-	%
		mono signal	-	0.2	-	%
B	frequency response 50 to 10000 Hz	mono, external 75 µs de-emphasis	–3	-	-	dB
S/N(W)	weighted signal-to-noise ratio (CCIR 468-3)	mono, external 75 µs de-emphasis	-	50	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SAP indication output, pin 6						
V_6	output voltage range	SAP present	-	-	0.5	V
		SAP not present	V_P–0.5	-	V_P	V
I_6	output current active LOW	SAP present	3	-	-	mA
Audio outputs, pins 23 and 24						
V_o	output signal (RMS value, pins 23, 24)	note 3	-	550	-	mV
	output signal headroom		-	9.5	-	dB
$\Delta V_{L,R}$	output signal difference between L and R	f = 250 to 6300 Hz	-	-	3	dB
ΔV_o	output signal difference after switching from L or R to SAP	f = 250 to 6300 Hz	-	-	3	dB
$\Delta V_{23, 24}$	DC offset voltage after switching	stereo/mono/SAP	-	-	±100	mV
$R_{23, 24}$	output resistance		-	200	300	Ω
R_L	load resistance		10	-	-	kΩ
C_L	load capacitance		-	-	500	pF
THD	total harmonic distortion	L and R signal	-	0.2	-	%
		SAP signal	-	0.5	-	%
B	L and R frequency response	f = 50 to 10000 Hz	–3	-	-	dB
		12 kHz related to 1 kHz	-	–3	-	dB
	SAP frequency response	f = 50 to 8000 Hz	–3	-	-	dB
S/N(W)	weighted signal-to-noise ratio	L+R signal; CCIR 468-3	-	50	-	dB
S/N	unweighted signal-to-noise ratio (RMS value)	L + R signal; f = 20 to 20000 Hz	-	60	-	dB
α_{CR}	crosstalk	L or R into SAP	50	63	-	dB
		SAP into L or R	50	70	-	dB
α_{CH}	channel separation (according to DBX requirements)	f = 100 to 5000 Hz				
		10% 75 µs equivalent input modulation	20	26	-	dB
		1 to 100% 75 µs equivalent input modulation	15	20	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DBX section						
V_9	SAP level control voltage range		-	1 to 4	-	V
V_{10}	(L–R) level control voltage range		-	1 to 4	-	V
V_{13}	spectral band level control voltage range		-	1.8 to 3.2	-	V
$I_{9, 10, 13}$	input current	$V_I = 0.5\ V_P$	-	-	5	µA
S_1	spectral RMS-detector release rate		343	381	419	dB/s
I_{12}	timing current for nominal release rate of spectral RMS-detector	note 4	-	22.5	-	µA
	current adjustment range		-	11 to 45	-	µA
S_2	wideband RMS-detector release rate		112.5	125	137.5	dB/s
I_{14}	timing current for nominal release rate of wideband RMS-detector	note 4 0.33 I_{12}	-	7.5	-	µA
	current adjustment range		-	4 to 15	-	µA
V_{15}	timing adjustment		-	1.5 to 3.8	-	V

Notes to the characteristics

1. Requirements for the MPX/SAP input signal to ensure correct system performance:
   a. Maximum variation of MPX/SAP signal under operating conditions: to be found (1 dB).
   b. 3 dB bandwidth ≥130 kHz (Δf = 25 kHz).
   c. THD (L + R, Δf = 25 kHz, f_{mod} = 1 kHz): 0.2%.
   d. S/N(W), weighted in accordance to CCIR468-3 (L+R, Δf = 25 kHz for sound carrier f_{mod} = 1 kHz, 75 µs de-emphasis; with critical picture modulation): S/N(W) > 44 dB; with sync only: S/N(W) > 54 dB.
   e. Spectral spurious attenuation: 40 dB (mainly n x f_H ; L + R, Δf = 25 kHz for sound carrier, f_{mod} = 1 kHz, 50 Hz to 100 kHz, no de-emphasis).
   f. Maximum white noise level (unweighted, 200 Hz to 100 kHz) to avoid malfunctioning of the identification circuits: 500 mV (RMS).
2. Adjustable on pin 27, measurement (f_H) on pin 7 with a 2.7 kΩ resistor connected between V_P and pin 31.
3. Can also be aligned to 600 mV (RMS), then identification threshold and AF output headroom will be decreased by 1.6 dB.
4. I_{12} and I_{14} can be measured via an ammeter connected to 4 V (3.5 to 4.1 V).

Table 1 MODE select, 4-state terminal pin 11

MODE	V_{11} (V_P = 5 V) (V)	SAP carrier	AF outputs pin 23	AF outputs pin 24	SAP/mono output pin 7
mono	8	on	mono	mono	SAP without DBX
stereo	V_P	on	right	left	SAP without DBX
SAP	$V_P/2$	on	SAP	SAP	mono
mono/SAP	0	on	SAP	mono	SAP without DBX
mono	8	off	mono	mono	mono
stereo	V_P	off	right	left	mono
SAP	$V_P/2$	off	right	left	mono
mono/SAP	0	off	mute	mono	mono

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	April 1991

TDA3840

TV IF amplifier and demodulator with TV signal identification

FEATURES

- Low supply voltage range, from 5.0 V to 8.0 V
- Low power dissipation, 200 mW at 5 V
- High supply ripple rejection
- Wide IF bandwidth of 80 MHz
- Synchronous demodulator with low differential phase and gain
- Additional video buffer with a wide bandwidth of 10 MHz
- Video off switch
- Peak sync AGC
- Adjustable take-over point (TOP); positive AGC slope
- Switching to fast AGC dependent on TV identification
- Alignment free AFC detector with integrated phase shift
- ESD protection
- TV signal identification
- Options: tracking of reference circuit

GENERAL DESCRIPTION

The TDA3840 is a bipolar integrated circuit for vision IF-signal processing in TV and VTRs, designed for a supply voltage range from 5.0 V to 8.0 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)		4.75	5.0	8.8	V
I_P	supply current (pin 15)	V_P = 5.0 V	–	42	–	mA
$V_{1\text{-}20(rms)}$	IF input signal for nominal video output voltage at pin 14 (RMS value)	f = 38.9 MHz	–	70	–	μV
	minimum IF input signal for TV signal identification at pin 6 (RMS value)	maximum G_v	–	20	40	μV
V_o	video output signal (pin 12)	buffered	–	2.0	–	V
G_v	IF voltage gain control range		–	66	–	dB
S/N	signal-to-noise ratio	$V_{1\text{-}20}$ = 10 mV	55	60	–	dB
V_8	AFC output voltage swing		–	4.0	–	V
S_{AFC}	AFC steepness (pin 8)		–	2	–	μA/kHz
RR	supply voltage ripple rejection (pin 12)		30	35	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3840	20	DIL	plastic	SOT146
TDA3840T	20	mini-pack	plastic	SO20L; SOT163A

TV IF amplifier and demodulator with TV signal identification

TDA3840

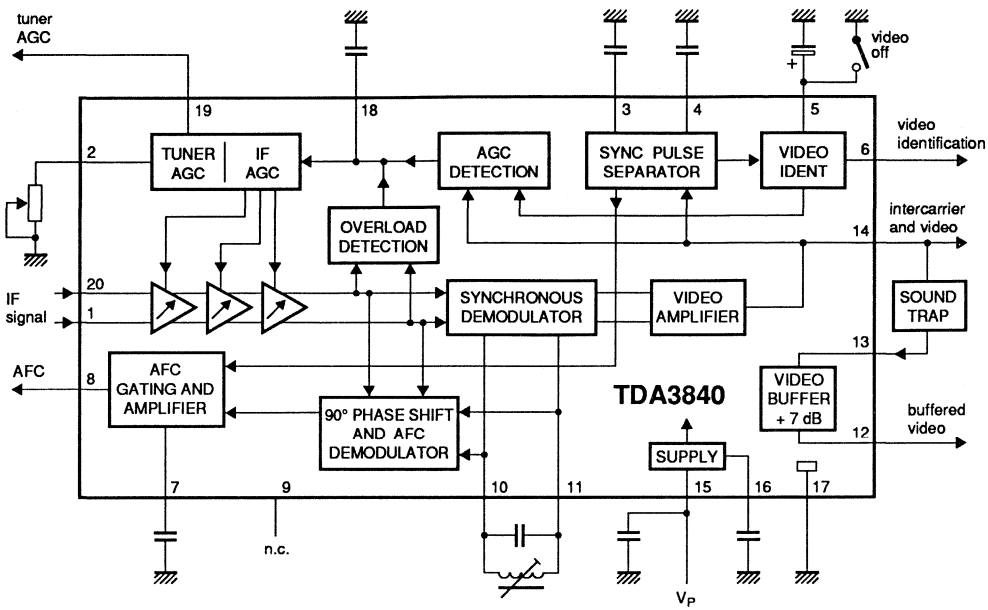


Fig.1 Block diagram.

PIN CONFIGURATION

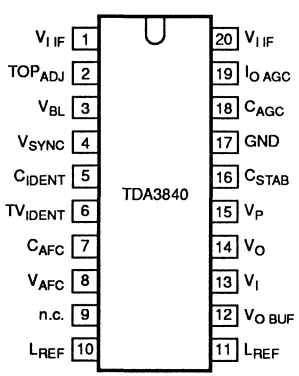


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{I\,IF}$	1	IF input (balanced)
TOP_{ADJ}	2	tuner AGC take-over point adjustment
V_{BL}	3	black level voltage
V_{SYNC}	4	sync pulse amplitude voltage
C_{IDENT}	5	identification capacitor
TV_{IDENT}	6	video identification output
C_{AFC}	7	AFC capacitor
V_{AFC}	8	AFC output signal
n.c.	9	not connected
L_{REF}	10	LC reference tuned circuit
L_{REF}	11	LC reference tuned circuit
$V_{O\,BUF}$	12	buffered video output signal
V_I	13	video input signal for buffer
V_O	14	video output signal with intercarrier signal
V_P	15	supply voltage
C_{STAB}	16	supply voltage stabilization
GND	17	ground
C_{AGC}	18	AGC capacitor
$I_{O\,AGC}$	19	tuner AGC output signal
$V_{I\,IF}$	20	IF input (balanced)

TV IF amplifier and demodulator with TV signal identification

TDA3840

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

1. 3-stage gain controlled IF amplifier
2. Overload detector
3. Reference amplifier
4. Carrier signal reference limiter
5. Video demodulator
6. Video amplifier
7. Video buffer amplifier
8. AGC detector
9. IF and tuner AGC (with adjustable TOP)
10. Sync pulse separator
11. Video identification
12. 90° phase shift and AFC demodulator
13. AFC gating, AFC amplifier and AFC switch
14. Voltage stabilizer

1. 3-stage gain controlled IF amplifier (pins 1 and 20)

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Gain control is achieved by current divider stages. The emitter feedback resistors are optimized for low noise and signal handling capability.

2. Overload detector

The overload detector is fed from the output of the third IF amplifier. As soon as the IF voltage exceeds the overload threshold in the detector, its output current reduces the IF amplification by discharging the AGC capacitor.

3. Reference amplifier

For passive video carrier regeneration an integrated differential amplifier with resistive load allows capacitive coupling of the resonant circuit for notch and tracking functions.

4. Carrier signal reference limiter

A limiter stage after the reference amplifier eliminates amplitude modulation. Its output is fed to the video demodulator.

5. Video demodulator

The video demodulator receives both the limited reference carrier signal and the IF signal. The video signal can also be switched off.

6. Video amplifier

The video amplifier is an operational amplifier with internal feedback and wide bandwidth.

7. Video buffer amplifier

The video buffer amplifier is an operational amplifier with internal feedback, wide bandwidth and frequency compensation; gain and input impedance are adapted to operate with a ceramic sound trap. The load for the sound trap is an integrated resistive divider.

8. AGC detector

The peak sync AGC detector generates a fast current pulse to discharge the AGC capacitor (gain reduction). This minimizes the video signal distortion.

To filter out the sound carrier the video signal is fed through low pass filters. After the low pass filters the video signal with attenuated sound carrier, is fed to the AGC detector. The charging current of the AGC capacitor is optimized for minimum distortion of the video signal. With positive modulation the charging current is very low and consequently the AGC time constant is large. When the video identification circuit does not detect a video signal, the charging current is increased.

9. IF and tuner AGC

The voltage on the AGC capacitor is used to control the gain of the three IF amplifier stages and to supply the tuner AGC current (open-collector). The tuner AGC TOP potentiometer at pin 2 adjusts the IF signal level from the tuner. To stabilize the IF output voltage of the tuner, IF slip (= variation of IF gain over the total tuner range) is kept at a minimum.

10. Sync pulse separator

The sync pulse separator supplies two internally-used pulses using the bandwidth limited video signal. These are the composite sync for the AFC detector and the vertical sync for the video identification output. The bandwidth is limited to reduce the noise and increase the identification sensitivity.

11. Video identification

An analog integrator monitors the duty cycle of the vertical sync pulses to identify the video signal. The integrator output is fed to a window comparator which has an open collector output stage to provide the video ident signal. The complete circuit operates in combination with the sync separator and is optimized for high sensitivity.

12. 90° phase shift and AFC demodulator

The AFC demodulator needs a 90° phase-shifted carrier. The output of the carrier signal reference limiter is fed to an active 90° phase-shift circuit. The 90° (lead) phase-shifted carrier and the IF signal are fed to the AFC demodulator. The demodulated signal and the IF signal are fed to the AFC gating stage.

13. AFC gating, AFC amplifier and AFC switch

With negative modulated video IF signals the output of the AFC detector is gated by composite sync pulses to prevent video modulation on the AFC output. The gated signal is integrated by an AFC capacitor. The AFC amplifier converts the capacitor voltage to an AFC current (open collector sink/source output). The AFC function can be externally switched off for test purposes. For high-performance signal handling the AFC signal can be used to track the resonant circuit as shown in Fig.11.

14. Voltage stabilizer

An integrated bandgap voltage stabilizer generates an internal supply voltage of 4 V. A decoupling capacitor reduces noise and supply voltage ripple.

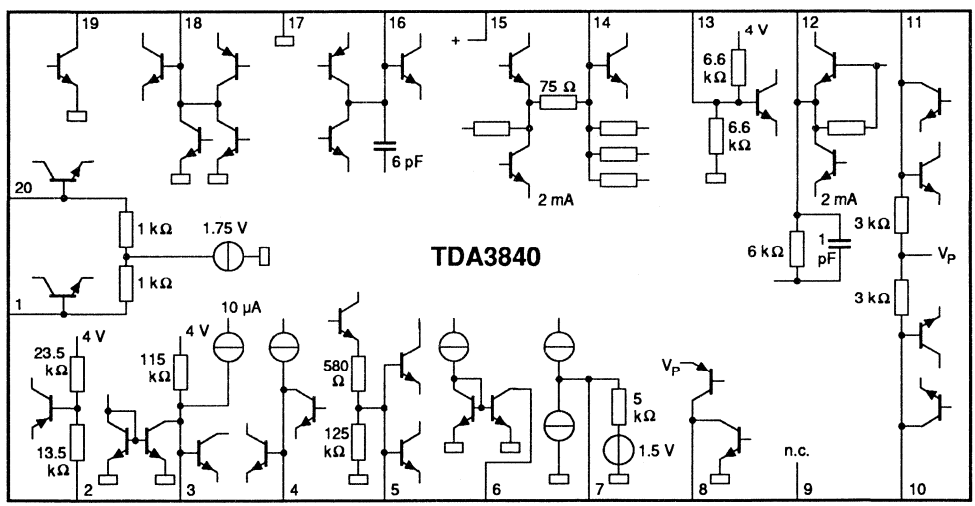


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage at pin 15: SOT146	–	8.8	V
	SOT163A	–	6.0	V
V_{19}	tuner AGC voltage	–	13.2	V
V_8	permissible voltage at AFC output	–	V_P	V
I_{15}	supply current	–	55	mA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
V_{ESD}	ESD sensitivity	–	± 300	V

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C; f_{VC} = 38.9 MHz; all voltages are measured to GND (pin 17); measured in test circuit of Fig.4.; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)	DIL-package	4.75	5.0	8.8	V
		SO-package	4.75	5.0	6.0	V
I_P	supply current (pin 15)	V_P = 5.0 V	–	42	–	mA
RR	ripple rejection (pin 12)		30	35	–	dB
IF amplifier						
B	bandwidth	–3 dB	–	80	–	MHz
R_I	input resistance (pins 1 and 20)		–	2	–	kΩ
C_I	input capacitance (pins 1 and 20)		–	1.5	–	pF
$V_{1\text{-}20(rms)}$	IF input signal (RMS value)	video output –1 dB	–	70	–	μV
	maximum IF input signal	minimum G_v; note 1	100	–	–	mV
G_v	gain control range		63	66	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF AGC						
I_{18}	leakage current AGC capacitor		–	–	1	μA
	charging current AGC capacitor	with video identification	–	13	–	μA
	charging current AGC capacitor	without video identification	–	35	–	μA
I_{18M}	discharging peak current capacitor		–	2	–	mA
t_1	response time of IF input signal change	50 dB increasing step	–	1	–	ms
		50 dB decreasing step	–	150	–	ms
Tuner AGC (note 2)						
$V_{1\text{-}20(rms)}$	lower IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R2 = 22 kΩ	–	–	1	mV
	upper IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R2 = 0 Ω	50	–	–	mV
	TOP variation	60 K temperature range	–	2	3	dB
I_{19}	tuner AGC output current	V_{19} = 0.5 V	1	2	–	mA
Synchronous demodulator and video amplifier (note 3)						
V_{14}	composite video output signal		0.9	1.0	1.1	V
	sync level voltage		–	1.5	–	V
	zero carrier level voltage		–	2.6	–	V
I_{14}	output current	DC and AC	–	–	± 1.0	mA
R_{14}	output resistance		–	75	–	Ω
B	video bandwidth at –1 dB (pin 14)	$C_{load} \leq 20$ pF	7	8	–	MHz
V_{14}	upper video clipping level		–	3.6	–	V
	lower video clipping level		–	0.3	–	V
Buffered video output signal (see Fig.6)						
G	gain of video buffer		6.5	7.0	–	dB
V_{12}	sync level clamping voltage		–	1.35	–	V
	upper video clipping level		–	4.25	–	V
	lower video clipping level		–	0.3	–	V
I_{12}	output current	DC and AC	–	–	± 1.0	mA
R_{12}	output resistance		–	–	10	Ω
B	video bandwidth at –1 dB (pin 12)	$C_{load} \leq 20$ pF	–	10	–	MHz
R_I	input resistance (pin 13)		–	3.3	–	kΩ
C_I	input capacitance (pin 13)		–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall video performance (see Fig.6)						
V_o	video output signal (pin 12)	negative modulation; note 3	–	2	–	V
B	video bandwidth at –2 dB (pin 12)	$C_{load} \leq 20$ pF	7	8	–	MHz
S/N	signal-to-noise ratio (see Fig.7)	V_{1-20} = 10 mV;note 4	55	60	–	dB
α_1	intermodulation for blue (note 5)	f = 1.1 MHz f = 3.3 MHz	56 62	58 –	– –	dB dB
α_2	intermodulation for yellow (note 5)	f = 1.1 MHz f = 3.3 MHz	53 60	56 –	– –	dB dB
α_3	signal harmonic suppression		–	26	–	dB
V_5	video switch off voltage	note 6	–	–	1	V
α_4	attenuation of video signal (pin 14)	video signal switched off	50	60	–	dB
ΔG	differential gain	EBU test line 330	–	2	–	%
$\Delta\Phi$	differential phase	EBU test line 330	–	2	–	deg
$\Delta V/V$	variation of video output signal (pin 14)	gain control 50 dB; $V_{1-20(rms)}$ = 0.3 to 100 mV	–	–	0.5	dB
V_{res1}	residual vision carrier (pin 12)		–	1	–	mV
V_{res2}	residual second harmonic of the vision carrier (pin 12)		–	1	–	mV
Video identification						
$V_{1-20(rms)}$	minimum IF input signal for TV identification at pin 14 (RMS value)	maximum G_v	–	20	40	µV
V_6	video identification voltage (signal unidentified)	$V_{1-20} = < 40\ \mu V_{rms}$ I_6 = 0.5 mA	–	–	0.4	V
	video identification voltage (signal identified)	$V_{1-20} = \geq 40\ \mu V_{rms}$ $I_6 = -1\ \mu A$	4.5	–	–	V
T_{sync}/T_{field}	vertical pulse duty cycle		4.5	8	16	$\times 10^{-3}$
C/N	carrier-to-noise ratio (pin 1 and pin 20)	note 7	–	8	–	dB
I_5	allowed leakage current		–	–	3	µA
α_5	sync pulse suppression for correct TV signal identification		–	–	70	%
t_d	delay time of mute output signal		–	100	150	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC (see Fig.9 and Fig.10); note 8						
I_8	AFC source current output		0.16	0.19	0.22	mA
	AFC sink current output		0.16	0.19	0.22	mA
V_8	upper output voltage		4.3	–	4.7	V
	lower output voltage		0.3	–	0.7	V
S	control steepness	QB = 40; $V_{1\text{-}20(rms)}$ = 10 mV	–	2	–	μA/kHz
I_7	leakage current at AFC gating		–	–	± 1	μA

Notes to the characteristics

1. The video signal is still gain-controlled, $V_{14(p\text{-}p)}$ = 1 V, but intermodulation figures are degraded.
2. The starting point of tuner AGC can be adjusted by the resistor at pin 2. Fig.5 shows the AGC characteristic.
3. IF input signals are RMS values measured at TOP sync (standard B/G) and with a vision carrier of 38.9 MHz (see Fig.4). The IF input signal is fed from 50 Ω via a 1:1 transformer, DSB, to pins 1 and 20. With a 10 mV_{RMS} IF input signal, the residual vision carrier is:
   = 10 % for white (standard B/G).
4. In the test circuit of Fig.4, measured and weighted according to CCIR Recommendation 567:

$$S/N = \frac{V_{14\ (black\ to\ white)}}{V_{14\ noise}\ (RMS,\ black)}$$

5. Intermodulation figures are defined as follows:

$$\alpha_1 = 20 \times \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6 \text{ dB}$$

and

$$\alpha_2 = 20 \times \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$$

6. When V_5 < 1 V (short-circuited identification capacitor at pin 5) the video output signal at pin 14 is switched off. V_{14} shifts to "zero carrier level ("ultra white" (2.6V) for negative modulation).
   During normal operation the capacitor at pin 5 should not be loaded ($|I_5| \leq 3$ μA).
7. The C/N at the IF input (pins 1 and 20) for TV identification is defined as the RMS sync level of the vision IF signal input, relative to the RMS value of a superimposed white noise signal, with a bandwidth limited to 5 MHz.
8. The values for the AFC measurements depend on the Q_B of the reference circuit at pins 10 and 11. The internal phase shift is matched to a vision carrier of 38.9 MHz. The AFC function can be switched off for test purposes when pin 7 is connected to ground (V_7 = 0 V).

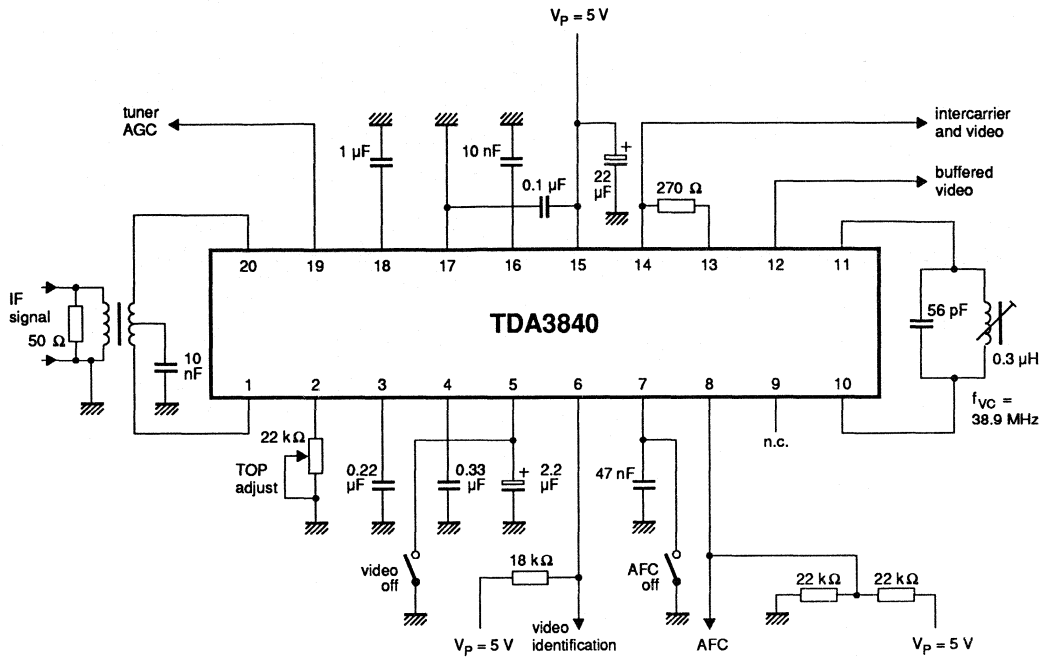


Fig.4 Test circuit.

TV IF amplifier and demodulator with TV signal identification

TDA3840

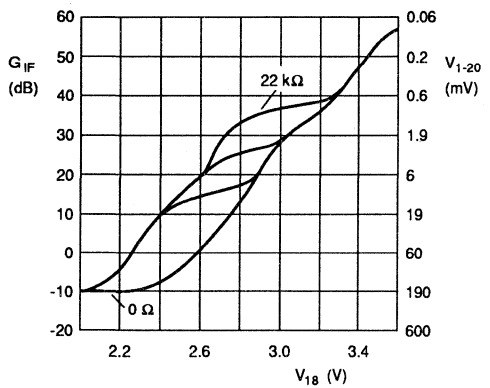


Fig.5 AGC characteristics with different values of R2.

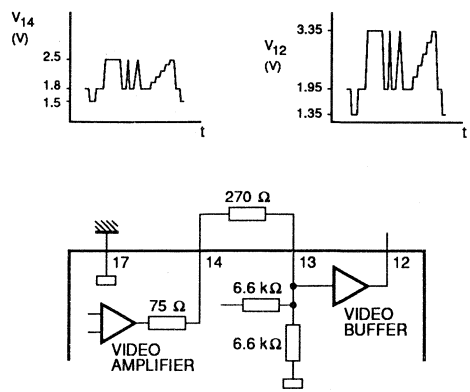


Fig.6 Video waveforms at intercarrier (pin 14) and buffered video (pin 12) outputs.

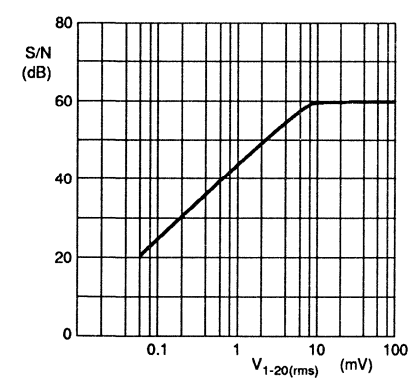
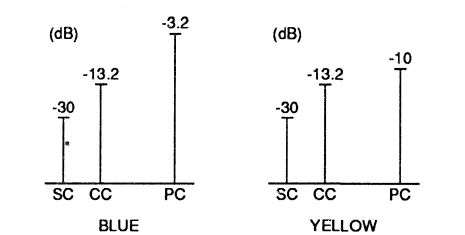


Fig.7 Signal-to-noise ratio as a function of IF input voltage (RMS value) at pins 1 and 20.



SC = sound carrier level
CC = chrominance carrier level
PC = picture carrier level
} with respect to TOP sync level.

Sound trap attenuation: 17 dB.

Fig.8 Input conditions for intermodulation measurements.

APPLICATION INFORMATION

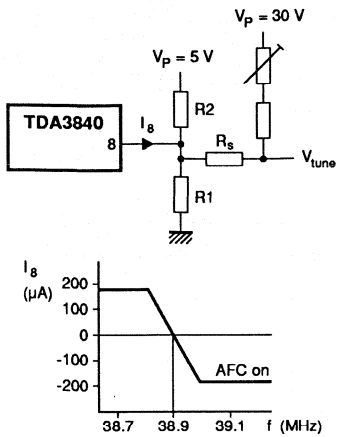


Fig.9 AFC interfacing for analog tuning systems and AFC characteristic.

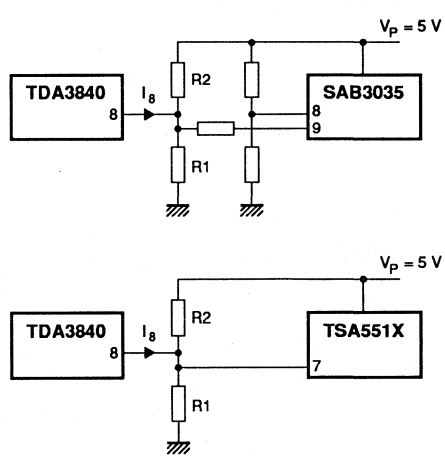


Fig.10 AFC interfacing for μP controlled systems.

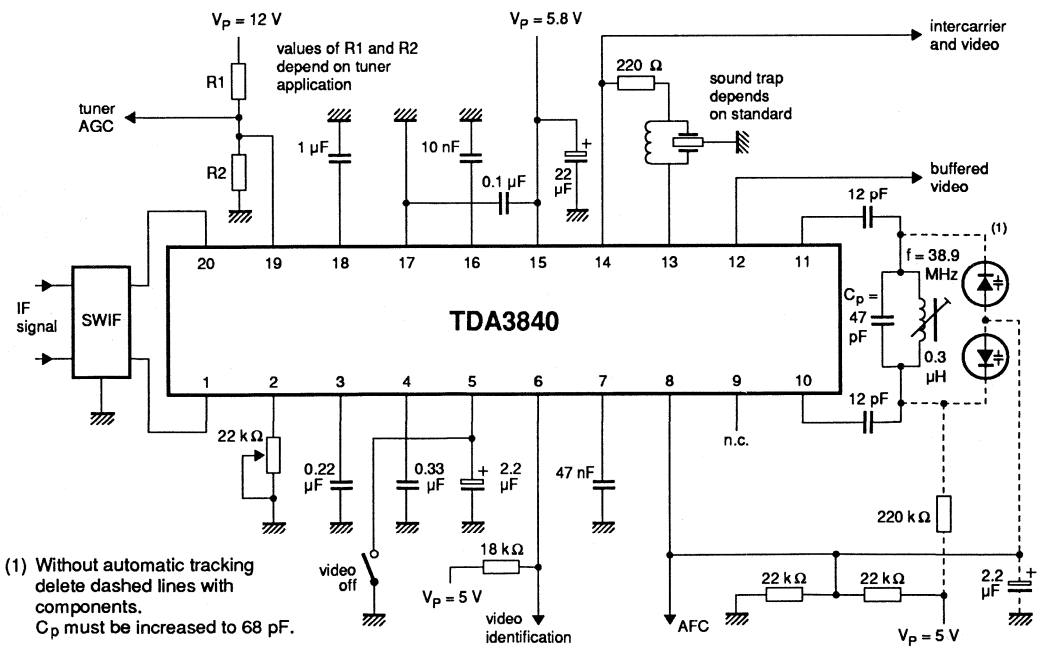


Fig.11 Application circuit with automatic tracking function and notch filter (dashed lines).

APPLICATION INFORMATION (continued)

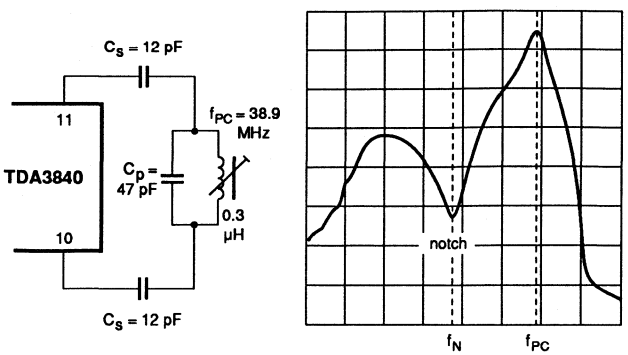


Fig.12 Reference circuit with notch filter for improved pulse response and better signal linearity.

Note to Fig.12

Recommended for reception of data signals e.g. in Teletext. Values in combination with SAW filter OFW G 1956 (Siemens). Curve shows combined frequency response of SAW filter and reference circuit.

For different standards C_s and C_p are calculated as follows:

$$C_s = 2\,C_p\left\{\frac{f_{PC}^2}{f_N^2} - 1\right\}$$

SOUND-IF CIRCUIT FOR TV AM-SOUND STANDARD L AND L'

GENERAL DESCRIPTION

The TDA3843 performs the AM-sound demodulation for the L- and L'- standard.

Features

- 5 to 8 V power supply and an alternative 12 V power supply
- Low power consumption (200 mW) at 5 V supply voltage
- New AC-coupled wideband IF-amplifier (high dynamic ranges, less intermodulation)
- In-phase wideband AM demodulator without external reference circuit
- Reduced THD figures even for low AF frequencies (typical 1%)
- Stabilizer circuit for ripple rejection and constant output signals
- All pins are ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)	V_{P1}	4.5	5	8.8	V
Supply voltage (pin 11)	V_{P2}	10.8	12	13.2	V
Supply current	$I_{11, 14-13}$	–	40	48	mA
Minimum IF input (RMS value)	V_{1-16}	–	70	100	μV
IF control range	ΔG_V	60	63	–	dB
AF output signal (RMS value)	V_{6-13}	–	550	–	mV
Signal plus weighted-noise to weighted-noise ratio (CCIR 468-3)	S+W/W	50	56	–	dB

PACKAGE OUTLINE

16-lead DIL; plastic (opposite bent leads) (SOT38WBE)

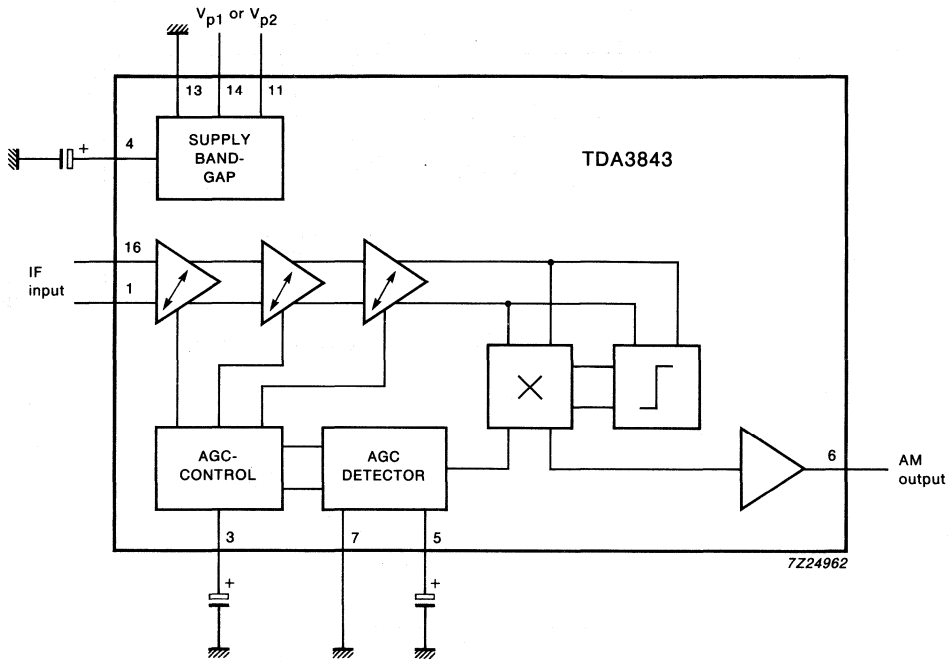


Fig.1 Block diagram.

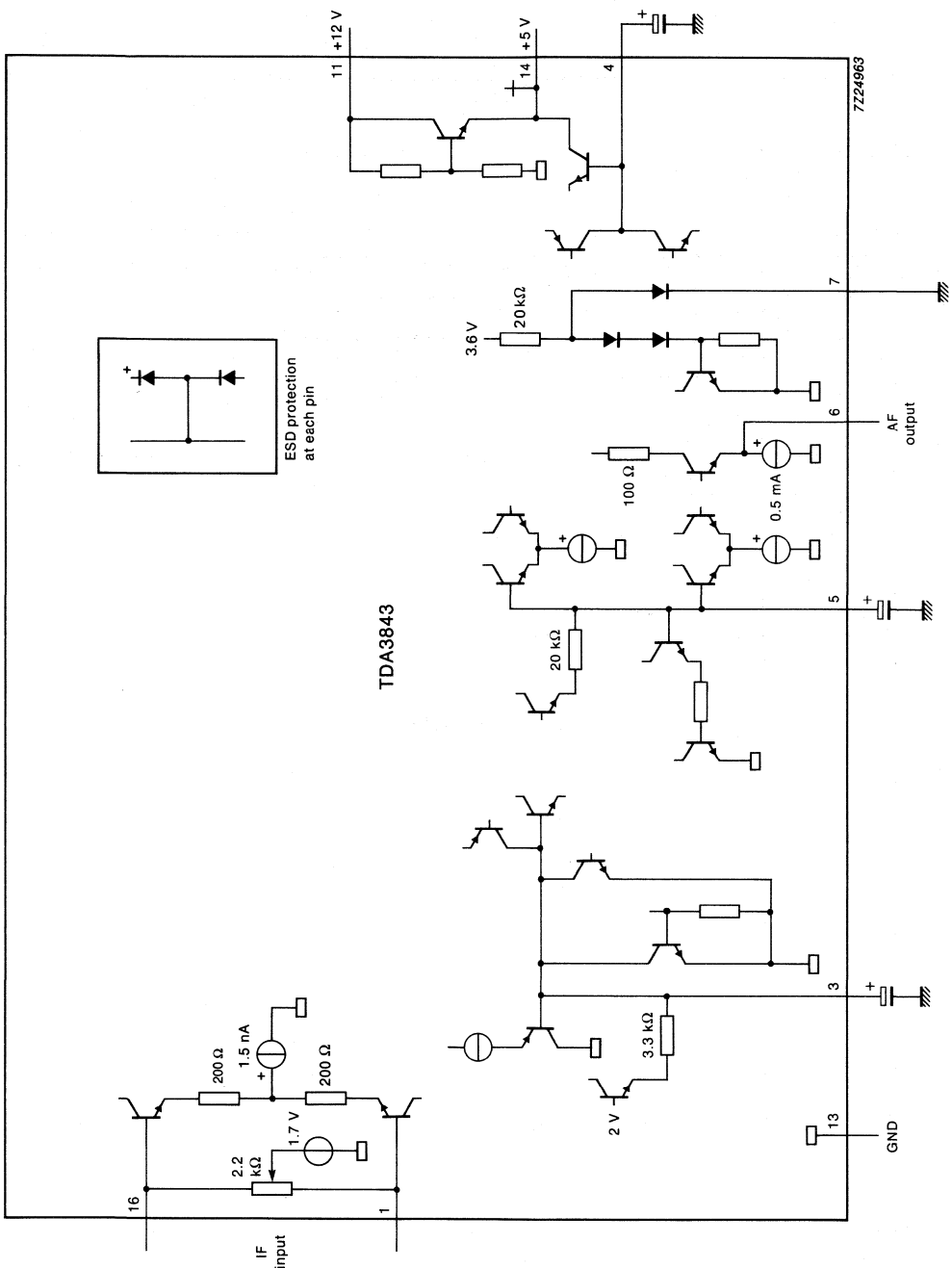


Fig.2 Input/output loading diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 14)	V_{P1}	4.5	8.8	V
Supply voltage (pin 11)	V_{P2}	10.8	13.2	V
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Storage temperature range	T_{stg}	−25	+ 125	°C
Total power dissipation at V_{P2}	P_{tot}	–	635	mW

CHARACTERISTICS

V_{P1} = 5 V (see note 1); T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Current consumption		I_{11}	–	40	48	mA
IF amplifier						
Input resistance		$R_{1\text{-}16}$	–	2	–	kΩ
Input capacitance		$C_{1\text{-}16}$	–	2.5	–	pF
Minimum IF input signal (RMS value)	note 2	$V_{1\text{-}16}$	–	70	100	μV
Maximum IF input signal (RMS value)	note 3	$V_{1\text{-}16}$	70	100	–	mV
Gain control range			60	63	–	dB
IF bandwidth	−3 dB		50	70	–	MHz
DC potential		$V_{1/16\text{-}3}$	–	1.7	–	V
AM demodulator	note 4					
AF output signal (RMS value)		$V_{6\text{-}13}$	440	550	660	mV
AF bandwidth	−3 dB, note 5	$V_{6\text{-}13}$	0.02	–	>100	kHz
Total harmonic distortion		THD	–	1	2	%
Signal plus weighted-noise to weighted-noise ratio (CCIR 468-3)	note 6	S+W/W	50	56	–	dB
DC potential		$V_{6\text{-}13}$	–	1.8	–	V
Output resistance	emitter follower with 0.5 mA bias current	R_6	–	200	–	Ω
Allowable AC output current (peak-to-peak value)	note 7	$\pm I_6$	–	–	0.3	mA
Allowable DC output current		$-I_6$	–	–	1	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Ripple rejection	$V_{ripple} < 200$ mV (peak-to-peak), 50 to 100 Hz, measured at 70 Hz					
AF signal output	$\alpha RR = V_{ripple}$ on V_P/V_{ripple} on V_O	αRR	30	40	–	dB
IF filter						
Proposal for sound carrier filter for L-standard	Fig.5					

Notes to the characteristics

1. Using the power supply voltage range V_{P1} = 5 to 8 V, the performance will not essentially change. Using the power supply voltage range, V_{P2} = 12 V, the performance will be comparable with the performance at V_{P1} = 5 to 8 V. The unused power supply pin must not be connected.
2. Start of gain control (low IF input signal) at –3 dB AF signal reduction at pin 6.
3. End of gain control (high IF input signal) at + 1 dB AF signal expansion at pin 6.
4. Sound carrier = 32.4 MHz modulated with f = 1 kHz and a modulation depth m = 80%. IF input signal $V_{1\text{-}16}$ = 10 mV (RMS value).
5. A maximum value of 100 kHz is guaranteed, but, typically a maximum value of 700 kHz is found.
6. The capacitor at pin 4 may be omitted, but then the S+W/W figure will be degraded by up to 8 dB in the IF voltage range 1 mV up to 100 mV.
7. If a higher AC output current is required, an external resistor must be connected from the output to ground. This is to increase the bias current of the emitter follower (note, the maximum allowable DC output current).

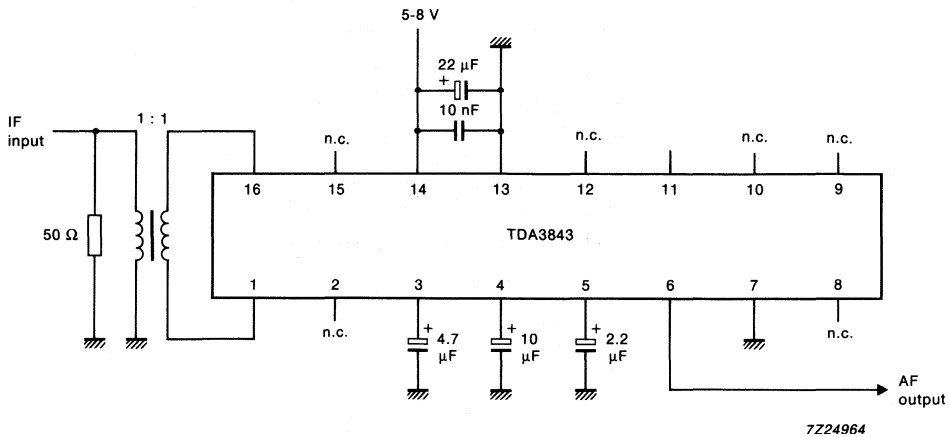


Fig.3 Test circuit, 5 V supply.

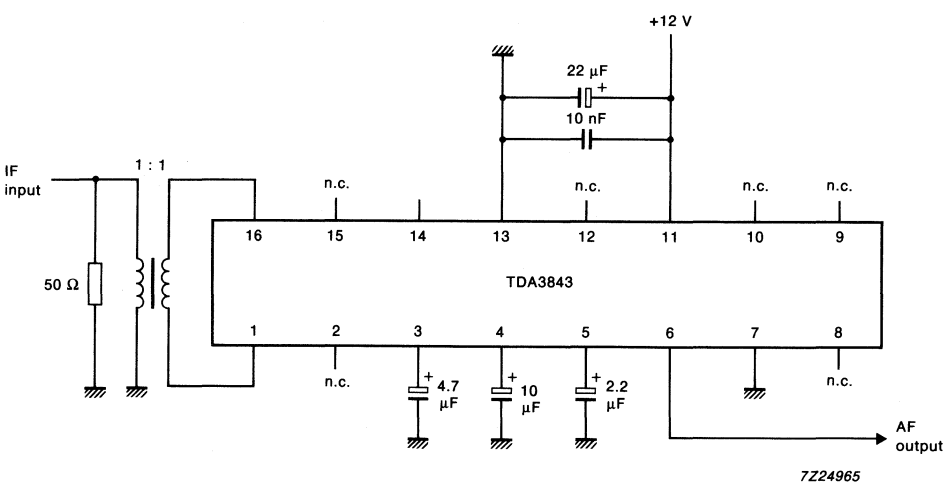
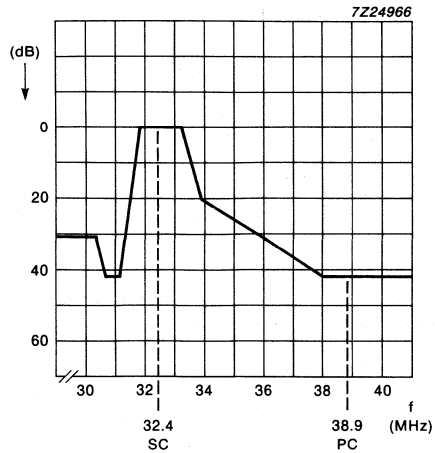


Fig.4 Test circuit, 12 V supply.



Where SC = sound carrier and PC = picture carrier.

Fig.5 AM IF filter for standard L.

QUASI-SPLIT-SOUND CIRCUIT AND AM DEMODULATOR

The TDA3845 is a quasi-split-sound IF circuit which is designed to give high performance television FM/AM sound.

Features

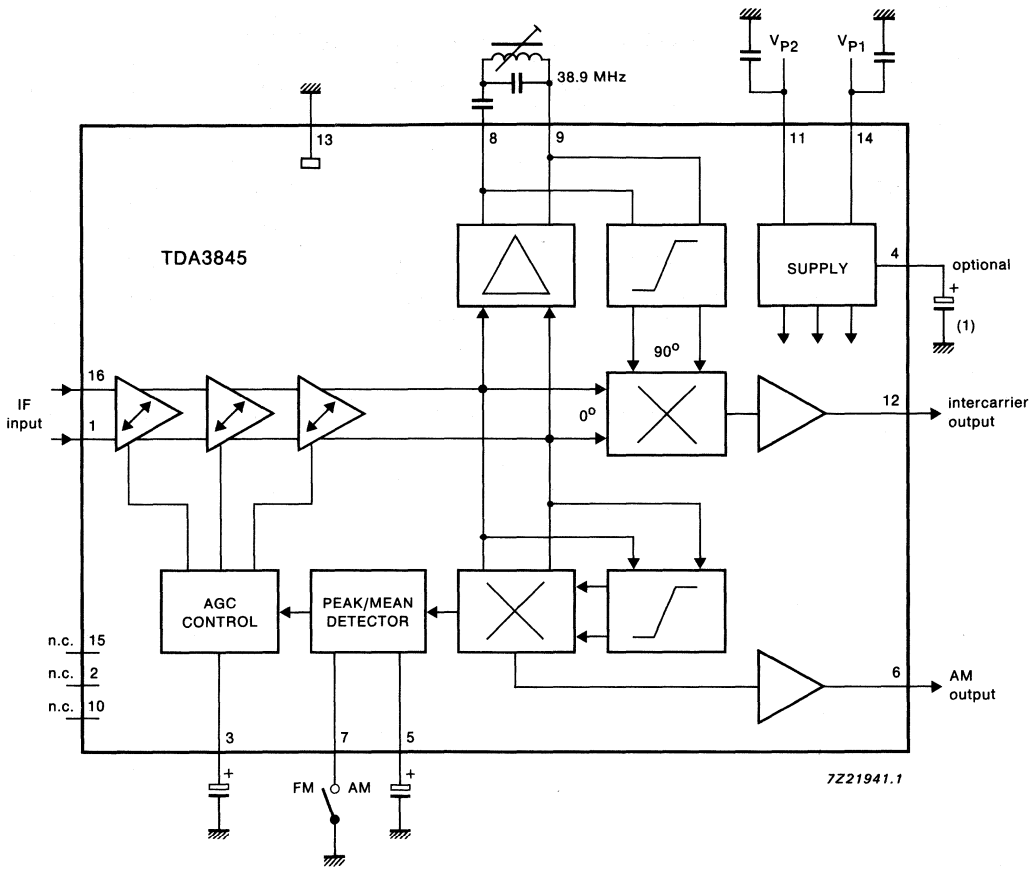
- Power supply from 5 V (200 mW) to 8 V source as well as an alternative 12 V source
- Gain controlled wideband IF amplifier (AC coupled with three stages)
- High precision internal 90° phase shifter for quadrature demodulator
- Amplitude detector for gain control which operates as a peak detector for FM sound and as a mean level detector for AM sound (switchable)
- Inphase wideband synchronous demodulator for AM detection
- Stabilizer circuit for ripple rejection and constant output signals
- ESD protection for all pins
- Suitable for all FM standards and L standard
- NICAM compatible

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 14		V_{P1}	4.5	5.0	8.8	V
or pin 11		V_{P2}	10.8	12.0	13.2	V
Supply current		I_P	–	40	–	mA
Minimum IF input voltage (RMS value)		$V_{1\text{-}16(rms)}$	–	70	100	μV
IF control range			60	63	–	dB
Intercarrier output voltage 5.5 MHz (RMS value)		$V_{12\text{-}13(rms)}$	70	100	–	mV
Signal-to-weighted-noise ratio (relative to 1 kHz; 50 kHz deviation)						
at 5.5 MHz for 2T/20T		(S + W)/W	–	60	–	dB
at 5.742 MHz for 2T/20T		(S + W)/W	–	58	–	dB
AF output voltage AM (RMS value)		$V_{6\text{-}13(rms)}$	440	550	660	mV
Signal-to-weighted-noise ratio; AM mode		(S + W)/W	–	56	–	dB
Total harmonic distortion (AM mode)		THD	–	1	2	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).



(1) See note 10 to the characteristics.

Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
pin 14		V_{P1}	4.5	8.8	V
or pin 11		V_{P2}	10.8	13.2	V
Storage temperature range		T_{stg}	−25	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C
Total power dissipation at V_{P2}		P_{tot}	−	635	mW

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1} = 5 V (see note 11); all measurements are with respect to ground (pin 13) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
pin 14		V_{P1}	4.5	5.0	8.8	V
or pin 11		V_{P2}	10.8	12.0	13.2	V
Total current consumption		I_{tot}	−	40	48	mA
IF amplifier						
Input resistance		$R_{1\text{-}16}$	−	2	−	kΩ
Input capacitance		$C_{1\text{-}16}$	−	2.5	−	pF
Minimum IF input voltage (RMS value)	note 1	$V_{1\text{-}16(rms)}$	−	70	100	μV
Maximum IF input voltage (RMS value)	note 2	$V_{1\text{-}16(rms)}$	70	100	−	mV
Gain control range		ΔG	60	63	−	dB
Gain control voltage range		$G_{v3\text{-}16}$	1.5	−	3.0	V
IF bandwidth	−3 dB	B_{IF}	50	70	−	MHz
DC potential		$V_{1\text{-}16}$	−	1.7	−	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Intercarrier mode (FM mode; standard B/G)	notes 3, 4 and 5					
Reference amplifier						
Picture carrier amplitude (peak-to-peak value)		$V_{8\text{-}9(p\text{-}p)}$	–	270	–	mV
Operating resistance		$R_{8\text{-}9}$	–	4	–	kΩ
DC potential		$V_{8\text{-}9}$	–	3.9	–	V
Intercarrier mixer and output stage						
Output signal (RMS value) at 5.5 MHz		$V_{12(rms)}$	70	100	–	mV
at 5.74 MHz		$V_{12(rms)}$	32	45	–	mV
Intercarrier bandwidth at −1 dB		B_{12}	–	8	–	MHz
at −3 dB		B_{12}	–	9	–	MHz
Residual video AM on intercarrier signal	note 6		–	3	10	%
Output resistance		R_{12}	–	30	–	Ω
DC potential		V_{12}	–	1,8	–	V
Allowable AC output current (peak value)	note 7	$\pm I_{12(peak)}$	–	–	0.7	mA
Allowable DC output current		$-I_{12}$	–	–	2	mA
AF signal performance	note 8					
Black picture		(S + W)/W	60/58	68/64	–	dB
2T/20T pulses with white bars		(S + W)/W	57/55	60/58	–	dB
6 kHz sinewave (black-to-white modulation)		(S + W)/W	53/51	57/55	–	dB
250 kHz square wave (black-to-white modulation)		(S + W)/W	50/44	56/50	–	dB
AM mode (standard L)	notes 4 and 9					
S/N weighted in accordance with CCIR 468-2						
AF output signal (RMS value)		$V_{6(rms)}$	440	550	660	mV
AF bandwidth	−3 dB; note 12	B_{AF}	0.02	–	120	kHz
Total harmonic distortion		THD	–	1	3	%

parameter	conditions	symbol	min.	typ.	max.	unit
Signal-to-weighted-noise	note 10	(S + W)/W	50	56	–	dB
DC potential		V_6	–	1.8	–	V
Output resistance		R_6	–	200	–	Ω
Allowable AC output current (peak value)	note 7	$\pm I_{6(peak)}$	–	–	0.3	mA
Allowable DC output current		$-I_6$	–	–	1	mA
Standard switch	note 4					
Peak signal AGC (FM mode)	V_{P1}	V_7	1.8	–	V_{P1}	V
or switch open-circuit	V_{P2}	V_7	1.8	–	5.5	V
Mean signal AGC (AM mode)		V_7	–	–	0.8	V
Switch current						
at 0 V		$-I_7$	–	–	200	μA
at V_{P1}		I_7	–	–	10	μA
at V_{P2} (via a 2.2 kΩ series resistor)		I_7	–	–	2.5	mA
Ripple rejection						
Voltage ripple < 200 mV (peak-to-peak value) at 70 Hz						
AM/AF signal						
αRR = voltage ripple on Vp/voltage ripple on output signal		αRR	30	40	–	dB
FM phase noise						
Δf_{rms} intercarrier signal		$\Delta f_{(rms)}$	–	10	20	Hz

Notes to the characteristics

1. Start of gain control (LOW IF input signal) at –3 dB intercarrier signal reduction at pin 12, AGC mode set to FM or –3 dB AF signal reduction at pin 6, AGC mode set to AM.
2. End of gain control (HIGH IF input signal) at + 1 dB intercarrier signal expansion at pin 12, AGC mode set to FM or + 1 dB AF signal expansion at pin 6, AGC mode set to AM.
3. Picture carrier (38.9 MHz) to sound carriers (33.4 MHz/33.158 MHz) ratio: 13/20 dB.
   IF input signal (picture carrier at sync pulse); $V_{1\text{-}16}$ = 10 mV (RMS value), Transmitter mode: DSB.
   Reference for the (S + W)/W ratio (0 dB) corresponds to the sound modulation where f = 1 kHz and frequency deviation Δf = ± 50 kHz.
   With reduced frequency deviation Δf = ± 30 kHz and the (S + W)/W figures will decrease by 4.5 dB.
4. If the device is used only for the B/G standard (no AM), the capacitor at pin 5 can be omitted (pin 5 has to be disconnected). In this instance the AGC will always operate as a peak-signal AGC and is independent of the voltage at pin 7.

Notes to the characteristics (continued)

The AM mode can also be used for the B/G standard, consequently standard switching is not required. However, the intercarrier level depends on the video modulation and the AF performance may decrease.
When the IC is operated from a 12 V power supply pin 7 can be connected to a 12 V logic level via a 2.2 kΩ series resistor.

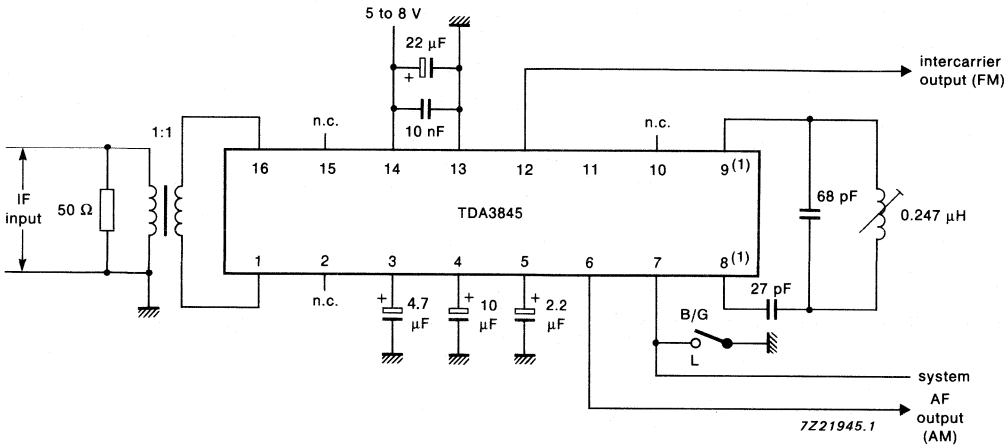
5. LC reference circuit for the picture carrier (pins 8 and 9); 68 pF//0.247 μH; in series with 27 pF: Q-loaded = 40 (Qo = 90); tuned to 38.9 MHz yields quadrature demodulation for the picture carrier which gives optimal video suppression at the intercarrier output (e.g. black-to-white jump of the video modulation).
The series capacitor provides a notch at the sound carrier frequency in order to produce more attenuation for the sound carrier in the PC reference channel. The ratio of parallel to series capacitance depends on the ratio of picture to sound carrier frequency which has to be adapted to other TV transmission standards, if required, in accordance with the formula:

$$C_S = C_P(F_{PC}/F_{SC})^2 - C_P$$

where:
C_S = series capacitor
C_P = parallel capacitor
F_{PC} = picture carrier frequency
F_{SC} = sound carrier frequency

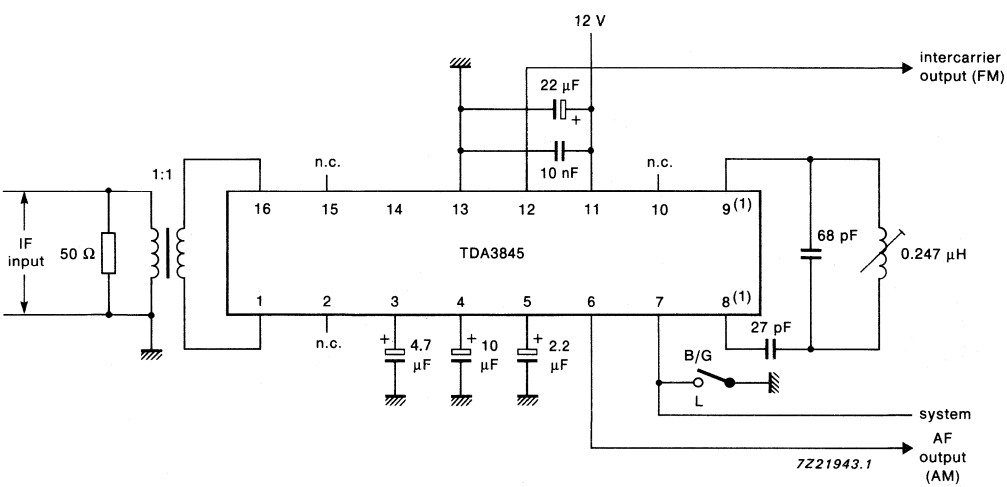
The result is an improved 'intercarrier buzz' in the stereo system B/G, particularly with 250 kHz video modulation (up to 10 dB improvement in sound channel 2), or to suppress 350 kHz video modulated beat in the digitally modulated NICAM subcarrier.
In order to optimize the AF signal performance, fine tuning to the optimal S/W at the sound channel 2 may be achieved by a 250 kHz video modulated squarewave.

6. Residual video AM is defined as:
   m = (A-B)/A
   A = intercarrier level at sync pulse
   B = intercarrier level at 100% white video modulation
7. If higher AC output current is required an external resistor must be connected between the output pin and ground in order to increase the bias current of the emitter follower. The allowable maximum DC output current must not be exceeded.
8. For all S/N measurements the used vision IF modulator must conform to the following:
   Incidental phase modulation for black-to-white jump should be less than 0.5 degrees.
   Intercarrier performance, measured with the television demodulator AMF2 (intercarrier mode weighted S/N ratio) better than 60 dB for 6 kHz sinewave black-to-white video modulation.
   Weighted S/N ratio of the demodulated intercarrier signals in accordance with CCIR 468-2, measured with deemphasis of 50 μs.
   The indicated (S + W)/W ratio X/Y concerns the sound channels 1 and 2 that means demodulated intercarrier signals of 5.5 and 5.74 MHz respectively.
9. Sound carrier frequency = 32.4 MHz modulated with f = 1 kHz and a modulation depth of 80%. IF input signal (sound carrier) $V_{1\text{-}16}$ = 10 mV (RMS value).
10. The capacitor at pin 4 can be omitted, however, the (S + W)/W figure for the AM sound (standard L) will be up to 8 dB worse in the IF voltage range 1 mV to 100 mV.
11. When the supply at V_{P2} = 12 V the performance will be comparable with the performance when V_{P1} = 5 to 8 V.
    The power supply pin that is not in use should be disconnected.
12. The maximum value is given as minimum 120 kHz and typical 700 kHz.



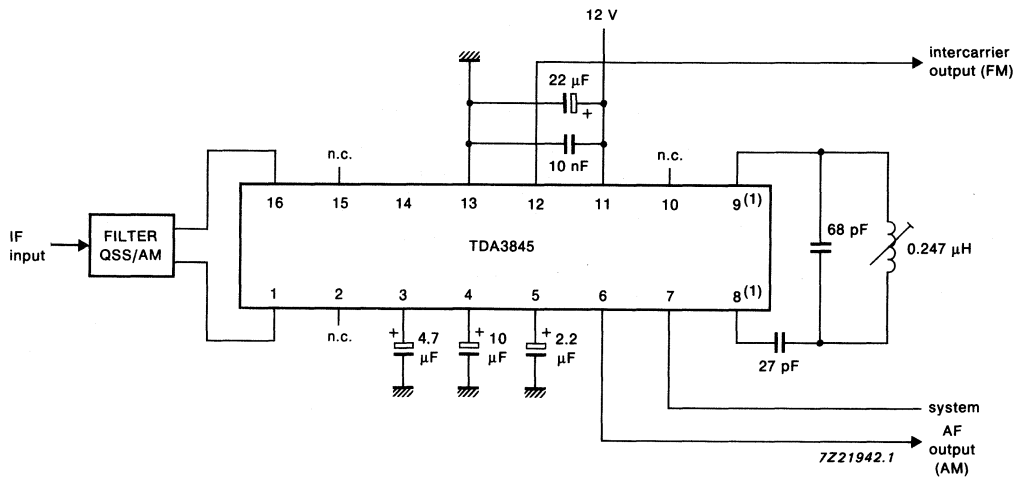
(1) See note 5 to the characteristics.

Fig.2 Test circuit for the + 5 V supply.



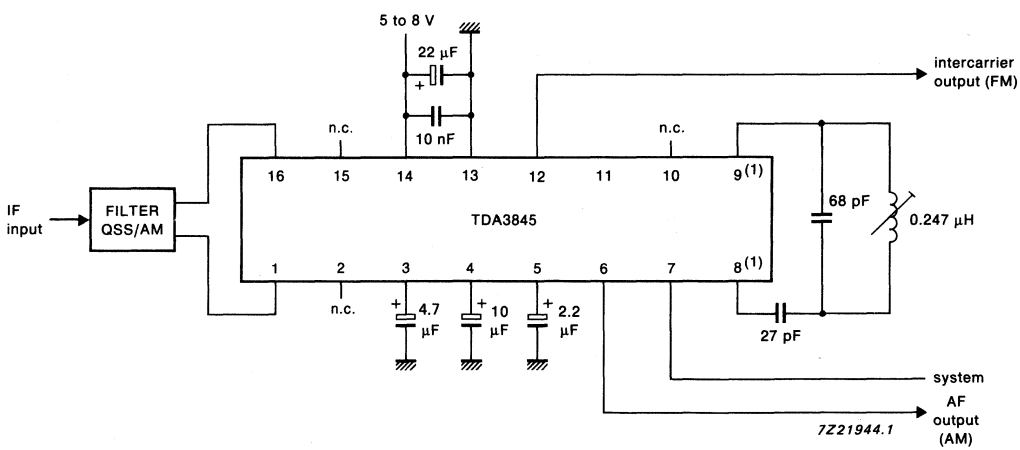
(1) See note 5 to the characteristics.

Fig.3 Test circuit for the + 12 V supply.



(1) See note 5 to the characteristics.

Fig.4 Application diagram for the + 12 V supply.



(1) See note 5 to the characteristics.

Fig.5 Application diagram for the + 5 V supply.

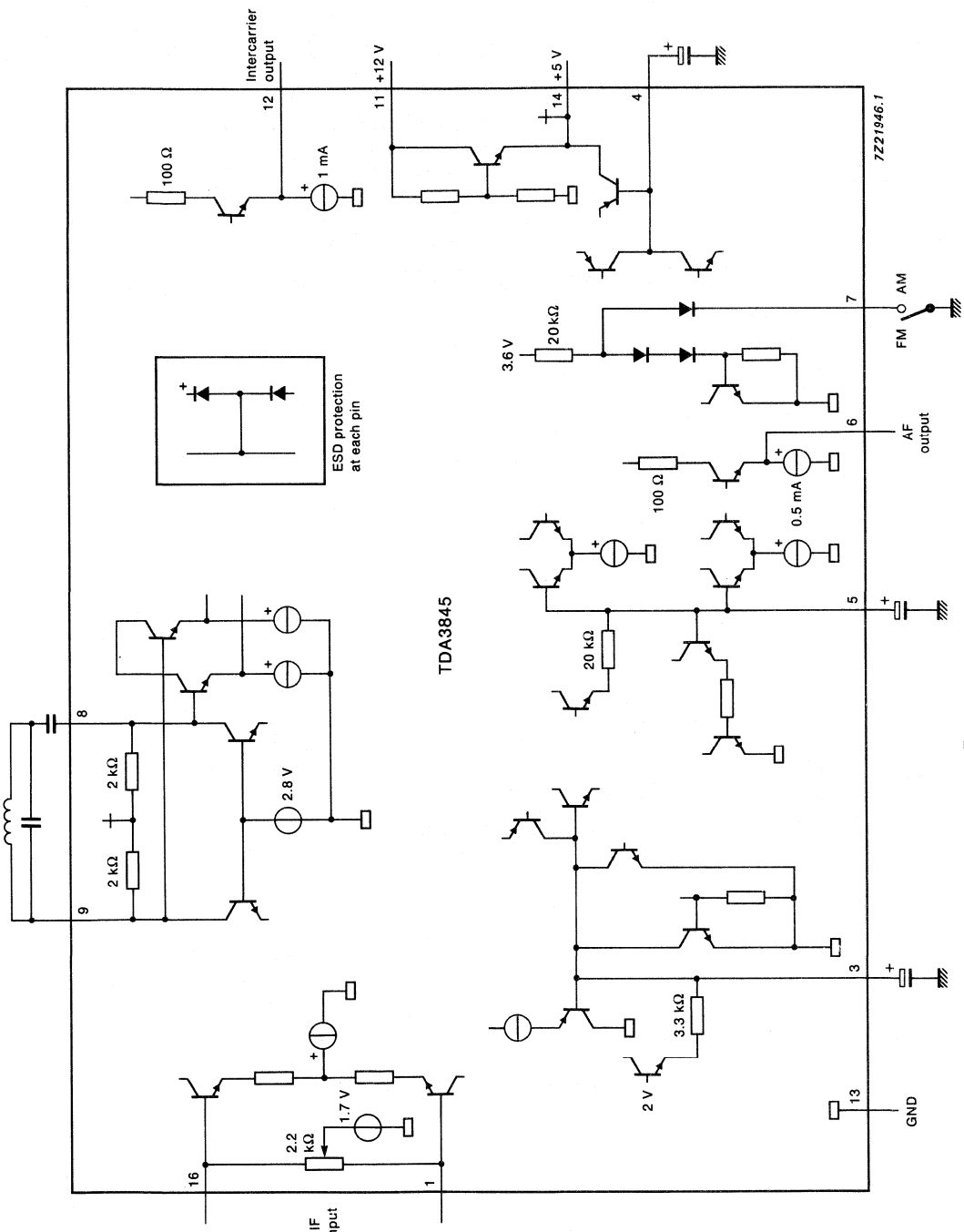
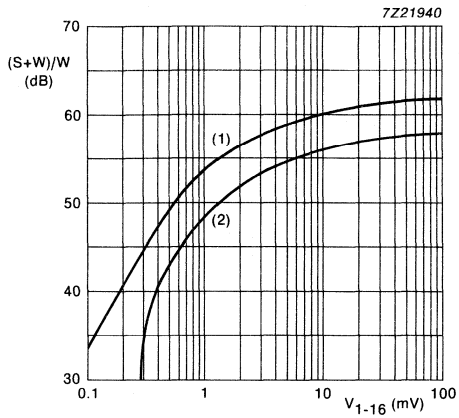


Fig.6 Pin related elements.



Picture modulation; 6 kHz sinewave.
Intercarrier signal; sound channel 1 = 5.5 MHz
sound channel 2 = 5.74 MHz.

Fig.7 Response curve of the signal-to-weighted-noise ratio of the demodulated intercarrier signal.

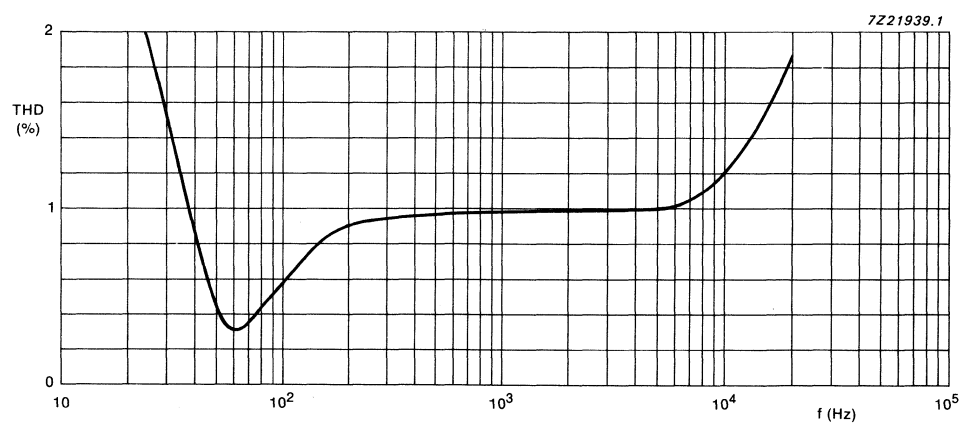


Fig.8 Response curve for the total harmonic distortion of the AM signal.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1992

TDA3853T

TV IF amplifier and demodulator with TV-identification

FEATURES

- Suitable for standards B/G (I, M, N, DK), see Table 1
- Gain controlled 3-stage IF amplifier with typically 80 MHz bandwidth
- High performance synchronous demodulator for negative and positive video modulation; passive regeneration of the reference signal
- Peak-sync-related AGC
- AGC output voltage take over point adjustable
- High sensitive TV identification based on vertical pulse duty cycle recognition; IDENT output
- Video off switch
- Sound trap buffer amplifier
- Tracking generator (AFT output) with Q-demodulator and internal 90 degree phase shifter for tracking the reference circuit
- Low supply voltage 5 V, low power consumption

GENERAL DESCRIPTION

Monolithic integrated circuit for vision IF signal processing in TV and VTR sets.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	4.75	5	6	V
I_P	supply current	-	46	-	mA
V_i	vision IF input signal sensitivity (RMS value, pins 1-20) maximum vision IF input signal (RMS value, pins 1-20)	- 100	70 -	100 -	µV mV
G_v	IF gain control range	63	66	-	dB
$V_{o\ CVBS}$	buffered CVBS output signal on pin 12 (peak-to-peak value)	1.7	2	2.3	V
B	–3 dB video bandwidth (pin 12)	-	14	-	MHz
S/N	signal-to-noise ratio for video	55	60	-	dB
$\alpha_{1.1}$ $\alpha_{3.3}$	intermodulation attenuation at yellow	53 60	56 -	- -	dB dB
α_{spur}	suppression of spurious harmonics of video signal	22	26	-	dB
T_{amb}	operating ambient temperature	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3853T	20	mini-pack	plastic	SOT163A

TV IF amplifier and demodulator with TV-identification

TDA3853T

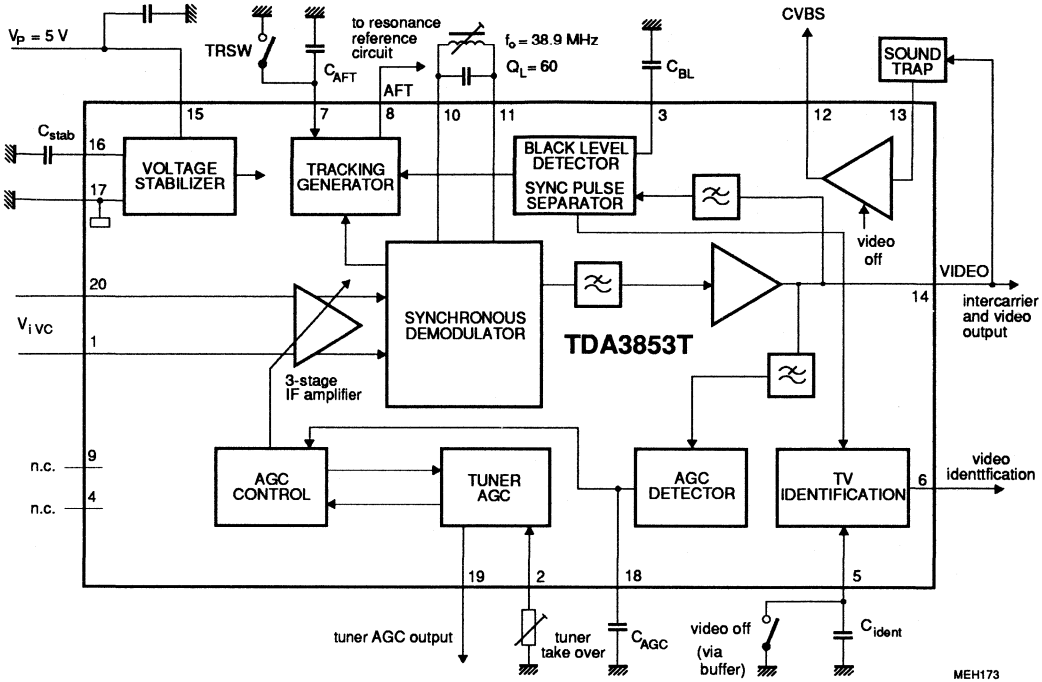


Fig.1 Block diagram.

TV IF amplifier and demodulator with TV-identification

TDA3853T

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\,a}$	1	balanced vision IF input a
TOP	2	tuner AGC take over adjustment point (TOP)
C_{BL}	3	capacitor for black level
n.c.	4	not connected
VIDOFF	5	video off input, identification capacitor
IDENT	6	TV identification output
TRSW	7	set input for tracking switch, tracking hold capacitor
AFT	8	automatic frequency tracking output
n.c.	9	not connected
RES1	10	resonance reference circuit for vision carrier
RES2	11	resonance reference circuit for vision carrier
CVBS	12	CVBS output (positive)
TRAP	13	video buffer amplifier input from sound trap
VIDEO	14	video and sound intercarrier output
V_P	15	+5 V supply voltage
C_{stab}	16	decoupling capacitor for voltage stabilizer
GND	17	ground (0 V)
C_{AGC}	18	capacitor for AGC
AGC	19	AGC output to tuner
$V_{i\,b}$	20	balanced vision IF input b

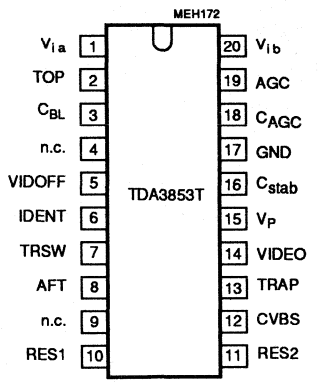


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3853T is a TV IF amplifier/ demodulator for negative modulation.

The IF input signal is amplified, gain-controlled and demodulated (Fig.1).

Vision IF amplifier and demodulator

The vision IF amplifier consists of three AC-coupled differential amplifiers. Gain control is achieved by current divider stages. Emitter feedback resistors in the differential amplifiers are optimized with respect to noise and signal capability.

Synchronous demodulator

The demodulator has a reference amplifier consisting of a differential amplifier with resistive load to provide passive vision carrier regeneration. This allows capacitive coupling of the resonance circuit to obtain a notch filter characteristic and tracking of the resonance circuit.
A cascaded limiter amplifier follows the reference amplifier to eliminate amplitude modulation. The limited IF reference signal is fed to the demodulator. The unlimited IF signal is fed via a phase correction network to the demodulator. The video amplifier is an operational amplifier with a wide bandwidth and internal feedback . The video and sound intercarrier signal is output on pin 14.

Video buffer amplifier

This operational amplifier has a wide bandwidth with internal feedback and frequency compensation. Gain and input impedance are adapted to operate with a ceramic sound trap. The switching functions are described in Table 1.

AGC detector and IF gain control

The video signal is fed through low-pass filters to attenuate the sound carriers and then is fed to the AGC detector.

Peak-sync AGC detection.
A special network provides current pulses to fast charge the AGC capacitor on pin 18 (gain reduction). This achieves a minimum of video distortion.
The AGC control converts the AGC capacitor voltage to three separate voltages to control the IF stages.

Sync pulse separator

The sync pulse separator separates the composite sync signal to gate the AFT. The vertical sync is used for identification. The input is band-limited to obtain a higher ident sensitivity.

Table 1 Switching functions of TDA3853T.

	VIDOFF pin 5	TRSW pin 7	video signal	IDENT pin 6
pin setting	L 2.2 µF	L* L*	video OFF video ON	0.5 mA sink H or 0.5 mA sink

* capacitor on pin 7 means tracking active; LOW means tracking inactive

Tuner AGC

The tuner AGC output current is fed to the open-collector output on pin 19. The take-over point is adjusted externally at pin 2 to adapt the tuner and SAW filter to an optimum IF input level. The IF gain variation over the full tuner gain range (slip) is minimized to ensure a constant tuner output signal.

Identification

An analog integrating network followed by a window comparator identifies the video signal by detection of the duty cycle of the vertical sync pulses. The pulses charge the identification capacitor on pin 5.

Tracking generator (AFT)

A limited 90 degree phase-shifted vision carrier signal is fed to the AFT quadrature demodulator, internal RC networks provide active phase shifting. The linear IF signal is applied to the other AFT quadrature demodulator input. The AFT output signal is applied to a gating stage. Gating with the composite sync pulses activates the AFT demodulator. Therefore the AFT output is free from video modulation. The AFT capacitor (pin 7) is charged by the gated AFT current. The capacitor voltage is converted to an DC output current on pin 9 (open-collector sink/source currents).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	0	6.0	V
I_P	supply current on pin 15	-	55	mA
V_n	voltage on pins 6, 8 and 12	–0.3	V_P	V
$V_{5,7}$	voltage on pins 5 and 7	–0.3	5.5	V
V_{13}	voltage on pin 13	–0.3	5.0	V
V_{14}	voltage on pin 14	–0.3	4.2	V
V_{19}	voltage on pin 19	–0.3	13.2	V
$I_{2,16}$	current on pins 2 and 16	-	–200	μA
$I_{5,6}$	current on pins 5 and 6	-	–60	μA
I_7	current on pin 7	-	–100	μA
I_8	current on pin 8	-	–50	μA
I_{12}	current on pin 12	-	–10	mA
I_{14}	current on pin 14	-	–3	mA
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling* for all pins**	-	±300	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

** Pins 1, 10, 11 and 20 have special protection, the other pins have standard protection by diodes to V_P and GND (this excludes pins 15 (V_P) and 19 (tuner AGC output) which have standard protection to GND only).

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C, f_{VC} = 38.9 MHz; V_{IIF} = 10 mV rms; DSB video modulation; sync level for B/G.
Measurements taken in Fig.3 without notch components and video signal according to Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)		4.75	5	6	V
I_P	supply current		-	46	55	mA
Standard set inputs (Table 1)						
V_{IL}	input voltage LOW, pins 5 and 7		0	-	0.8	V
Vision IF input (pins 1-20)						
V_i	input signal sensivity (RMS value)	–1 dB video	-	70	100	μV
	maximum input signal (RMS value)	+1 dB video; note 1	100	-	-	mV
G_v	IF gain control range	Fig.6	63	66	-	dB
B	IF bandwidth	–3 dB	-	80	-	MHz
R_i	input resistance		-	2	-	kΩ
C_i	input capacitance		-	1.5	-	pF
V_I	DC voltage on pins 1 and 20		-	2.50	-	V
Synchronous demodulator (pins 10 and 11)						
$V_{o\ ref}$	picture carrier amplitude, pins 10-11 (peak-to-peak value)		-	1.6	-	V
R_{10-11}	integrated operating resistance		-	12	-	kΩ
$R_{L\ 10-11}$	load resistance		tbn	-	-	kΩ
Q_L	load Q-factor of resonance circuit; note 2	no notch components	55	60	-	
$V_{10,\ 11}$	DC voltage		-	2.8	-	V
Composite video output (pin 14)						
V_o	output signal (peak-to-peak value)		0.9	1.0	1.1	V
V_{14}	sync level		-	1.5	-	V
	ultra-white level		-	2.63	-	V
	upper video clipping level		-	4.3	-	V
	lower video clipping level		-	0.3	-	V
R_{14}	output resistance		-	-	10	Ω
I_{14}	output current	DC and AC	-	-	±1	mA
B	–1 dB video bandwidth	C_{14} < 20 pF	tbn	10	-	MHz
	–3 dB video bandwidth	C_{14} < 20 pF	tbn	14	-	MHz
RR	ripple rejection on pin 14	f_{ripple} = 70 Hz; note 3	tbn	30	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS buffer amplifier (pins 12 and 13)						
R_{13}	input resistance		-	3.3	-	kΩ
C_{13}	input capacitance		-	2	-	pF
$V_{o\ CVBS}$	typical CVBS output signal on pin 14 (peak-to-peak value)	note 4	-	2	-	V
	CVBS output level	upper video clipping	-	4.25	-	V
		lower video clipping	-	0.3	-	V
		sync level	-	1.35	-	V
I_{12}	output current	DC and AC	-	-	±1	mA
R_{12}	output resistance		-	-	10	Ω
G_v	voltage gain	note 4	6.5	7	7.5	dB
B	–3 dB video bandwidth	C_{14} < 20 pF	tbn	14	-	MHz
RR	ripple rejection on pin 12	f_{ripple} = 70 Hz; note 3	tbn	35	-	dB
Measurements from IF input to CVBS output (pin 12)						
$V_{o\ CVBS}$	typical CVBS output signal on pin 12 (peak-to-peak value)	Fig.10	1.7	2	2.3	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	-	-	0.5	dB
		30 dB gain control	-	0.1	-	dB
ΔG	differential gain	10 to 90% modulation	-	2	5	%
Δφ	differential phase	10 to 90% modulation	-	2	5	°
$tilt_H$	horizontal tilt		-	0.7	1.5	%
B	–2 dB video bandwidth	C_L < 20 pF	tbn	12	-	MHz
S/N	signal-to-noise ratio	note 5; Fig.5	-	58	-	dB
$\alpha_{1.1}$	intermodulation at "blue", note 6	f = 1.1 MHz; Fig.8	56	58	-	dB
	intermodulation at "yellow"	f = 1.1 MHz	53	56	-	dB
$\alpha_{3.3}$	intermodulation at "blue"	f = 3.3 MHz	62	-	-	dB
	intermodulation at "yellow"	f = 3.3 MHz	60	-	-	dB
α_{1H}	residual vision carrier (RMS value)	fundamental wave	-	1	10	mV
α_{2H}		second harmonic	-	1	10	mV
α_{spur}	suppression of spurious video signal harmonics	transformer; Fig.4	22	26	-	dB
RR	ripple rejection on pin 12	f_{ripple} = 70 Hz; note 3	tbn	30	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC detector (pin 18)						
t_{resp}	response to an increasing amplitude step of 50 dB in input signal		-	1	10	ms
	response to a decreasing amplitude step of 50 dB in input signal		-	150	300	ms
V_{18}	gain control voltage on capacitor	full gain range	1.5	-	4	V
I_{18}	peak charging current (peak value)		-	–2	-	mA
	charging current		-	–0.5	-	mA
	discharging current		-	11	-	μA
Tuner AGC (pin 19)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1-20	-	-	1	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1-20	50	-	-	mV
ΔG_{IF}	IF gain variation	maximum ΔI_{AGC} = 1 mA	-	3	6	dB
V_{19}	permitted output voltage	from external	-	-	13.2	V
	saturation voltage	I_{19} = 1 mA	-	0.2	0.5	V
ΔV_{19}	variation of take over point by temperature	ΔT = 60 °C	-	2	3	dB
I_{19}	sink current	no tuner gain reduction; Fig.7	-	0	0.1	μA
		maximum tuner gain reduction	1.5	1.8	2.0	mA
RR	ripple rejection on pin 19	f_{ripple} = 70 Hz; note 3	tbn	20	-	dB
TV identification and black level detector (pins 5, 6 and 3)						
V_i	IF input signal on pins 1-20 (RMS value)	TV identified	-	50	-	μV
C/N	carrier-to-noise ratio at IF input	TV identified; note 7	-	10	-	dB
V_{14}	minimum sync amplitude in relation to typical sync	identification on	-	30	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_6	output voltage for TV identified		4.5	4.95	V_P	V
	output voltage for TV not identified	I_7 = 500 µA	-	0.1	0.4	V
I_6	output current (sink)	no ident	-	500	-	µA
	allowed leakage current (source)	ident	-	-	−1	µA
V_5	voltage for "identification on"	2.2 µF capacitor on pin 5	-	2.6	-	V
I_{leak}	permitted leakage current (capacitor pin 5)		-	-	3	µA
$t_{p\,V}$	vertical pulse duty cycle for TV identified	$t_{sync}/t_{vertical}$	4	8	25	10^{-3}
Tracking generator, AFT (pins 7 and 8)		note 8				
V_8	maximum output voltage	note 9; Fig.9	4.3	-	4.7	V
	minimum output voltage		0.3	-	0.7	V
	permitted output voltage		-	-	V_P	V
I_8	sink output current		160	180	220	µA
	source output current		−160	−180	−220	µA
	offset output current		-	-	±20	µA
S	control steepness	$\Delta I_9/\Delta f$; note 9	-	2	-	µA/kHz
$\Delta\varphi$	phase offset spread for 38.9 MHz	note 10	-	-	±4	°
V_7	input voltage for TRSW	tracking off; Table 1	0	-	0.8	V
	(independent of other mode switches)	tracking on	open-circuit			V

Notes to the characteristics

1. Video signal is still gain controlled with 2 V (p-p) on output ; but intermodulation figures are lowered.
2. AFT characteristic depends on Q-factor.
3. Ripple rejection for f = 50 to 100 Hz.
4. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p). When no sound trap is applied, a 330 Ω resistor must be connected from output to input (from pin 14 to pin 13).
5. S/N is the ratio of the black-to-white amplitude (pin 12) and the RMS value of noise (black, pin 12). B = 5 MHz weighted in accordance with CCIR-567 at a source impedance of 50 Ω.

6. $\alpha_{1.1}$ = 20 log (V_o at 4.4 MHz / V_o at 1.1 MHz) + 3.6 dB; $\alpha_{1.1}$ value at 1.1 MHz related to black/white signal.
   $\alpha_{3.3}$ = 20 log (V_o at 4.4 MHz / V_o at 3.3 MHz); $\alpha_{3.3}$ value at 3.3 MHz related to colour carrier.
7. The carrier-to-noise ratio at IF input for "TV identified" is defined as the ratio of carrier (top sync, RMS value) and noise (RMS value). Conditions: 5 MHz bandwidth; V_{iIF} = 10 mV RMS (top sync) and a video signal of 2T + 20T + white bar.
8. A current source output is provided to match the AFT output signal to the different tuning systems. The internal 90 degrees phase shifter is matched for f_o = 38.9 MHz.
9. The AFT characteristic depends on Q_L of the resonance circuit (Q_L = 60, without notch components).
10. ±4 º corresponds to ±23 kHz for Q_L as in Fig.1 (refer to note 9).

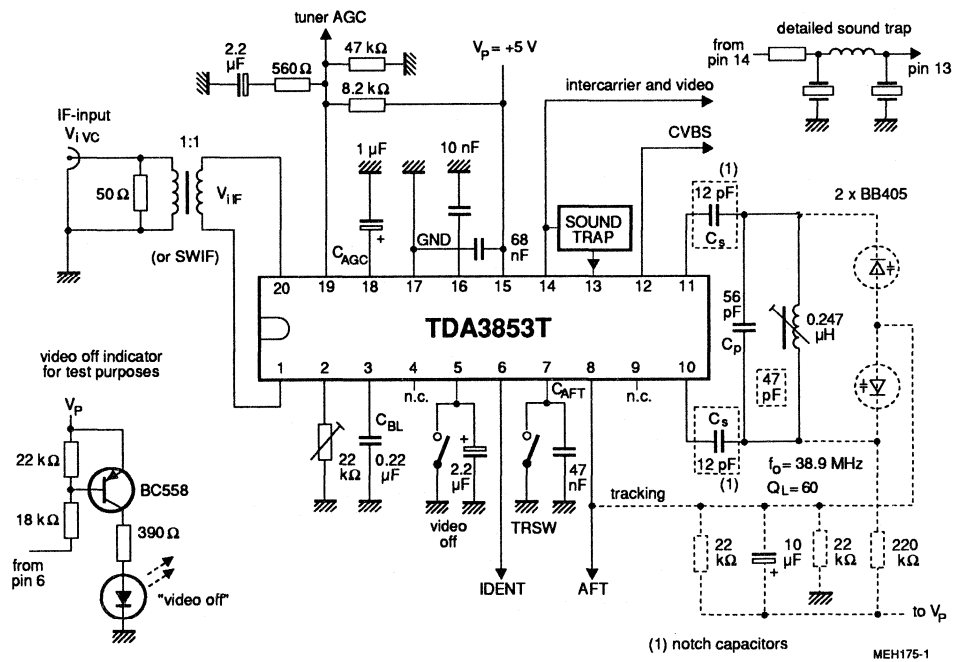


Fig.3 Test and application circuit. Test circuit without notch capacitors and with sound trap replaced by a 330 Ω resistor. Dashed components for tracking application only; application circuit with SWIF.

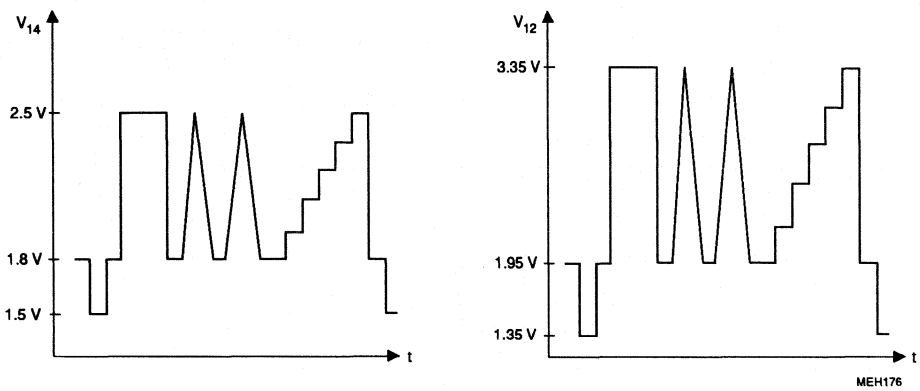


Fig.4 Video test signals.

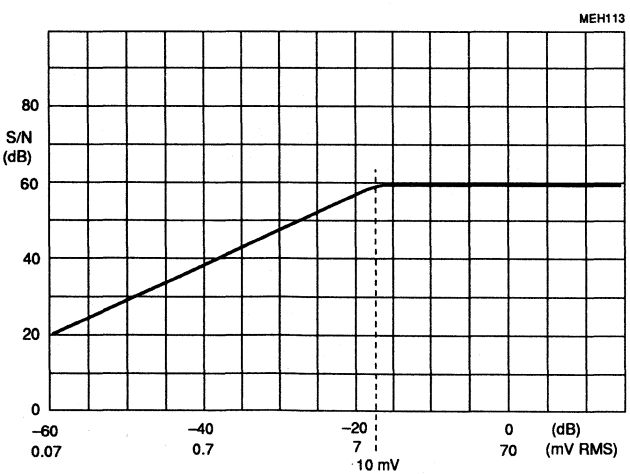


Fig.5 Signal-to-noise ratio (typical) as a function of IF input signal.

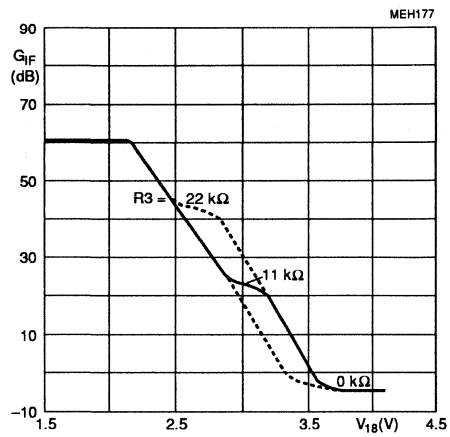


Fig.6 IF gain as a function of adjustment at pin 2.

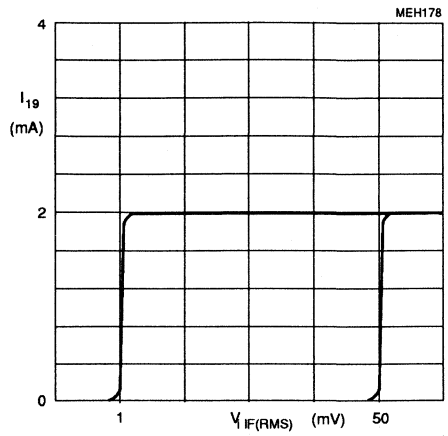
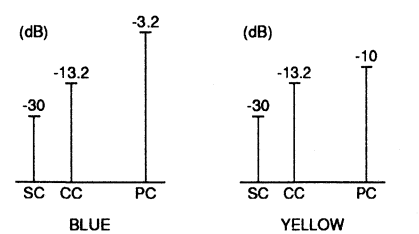


Fig.7 Tuner AGC characteristic.



SC = sound carrier level
CC = chrominance carrier level
PC = picture carrier level
} with respect to TOP sync level.

Sound trap attenuation: 17 dB.

MEH114

Fig.8 Input conditions for intermodulation measurements.

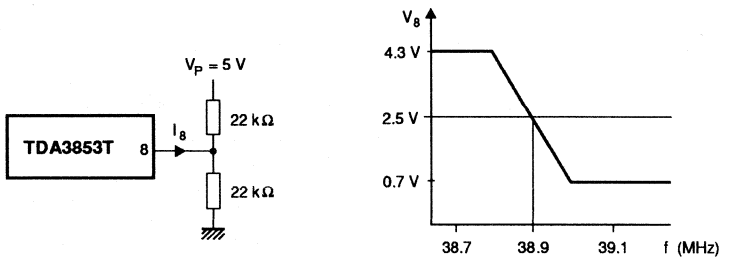


Fig.9 AFT characteristic.

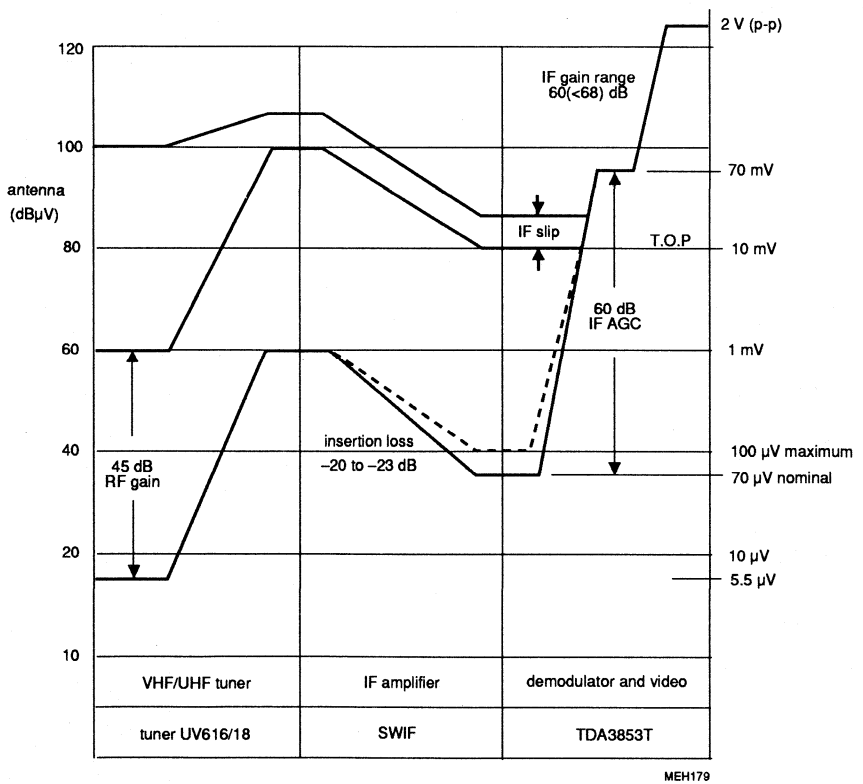


Fig.10 Front end level diagram.

TV IF amplifier and demodulator with TV-identification

TDA3853T

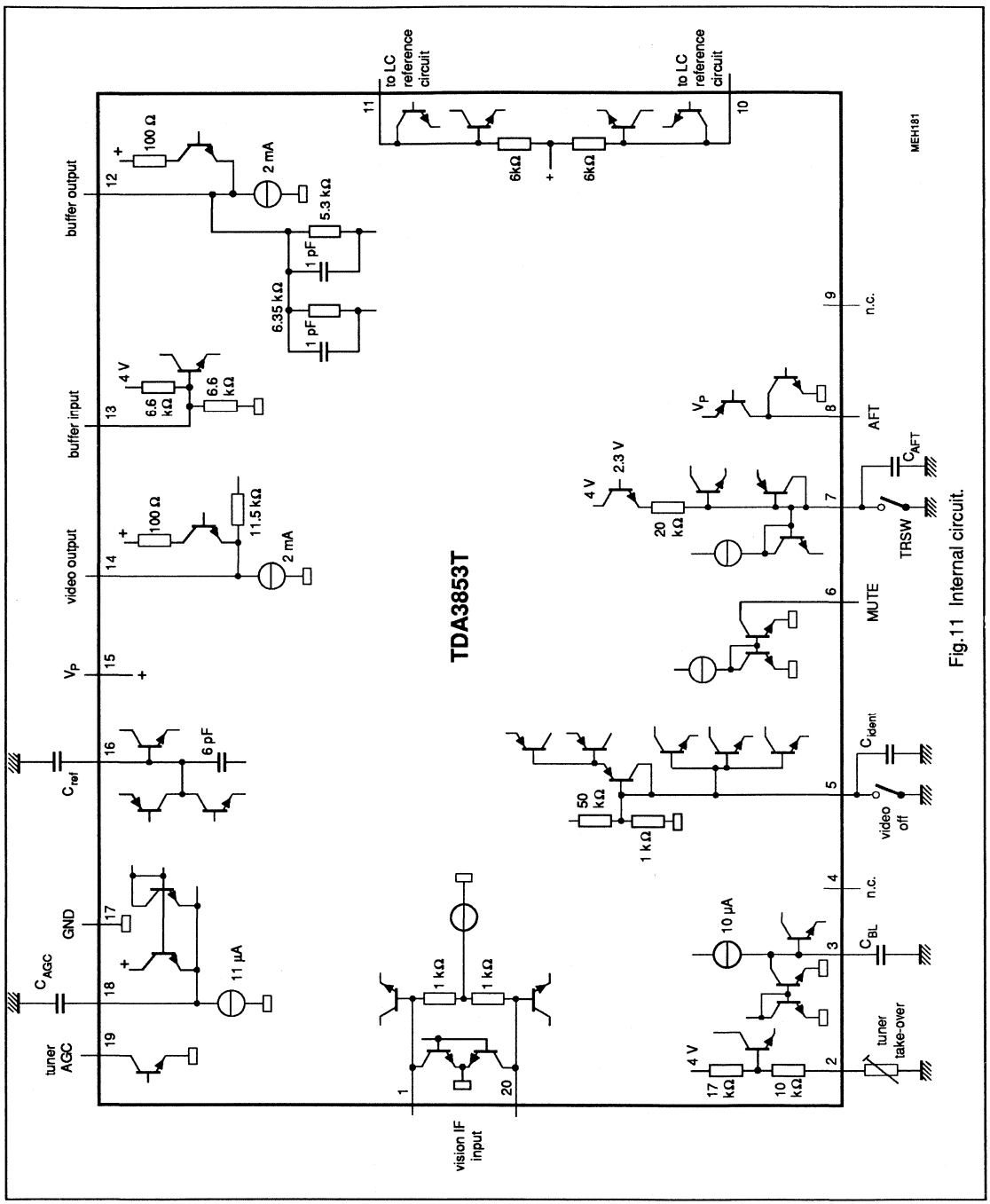


Fig.11 Internal circuit.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA3856

Quasi-split sound processor for all standards

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- Automatic muting of the AF2 signal (at B/G) by the input level
- AM signal processing for L standard and switching over the audio signal
- Stereo-matrix correction
- Layout-compatible with TDA3858 (32 pins) and TDA3857 (20 pins)

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM or AM sound.

Gain controlled wideband IF amplifier, input select switch.

AGC generation due to peak sync for FM or mean signal level for AM.

Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 21)	4.5	5	8.8	V
I_P	supply current	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
$V_{o\ (rms)}$	audio output signal for FM (B/G)	-	1	-	V
$V_{o\ (rms)}$	audio output signal for AM (L)	-	0.6	-	V
THD	total harmonic distortion				
	for FM	-	0.5	-	%
	for AM	-	1	-	%
S/N (W)	weighted signal-to-noise ratio				
	for FM	-	68	-	dB
	for AM	-	56	-	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3856	24	shrink DIL	plastic	SOT234

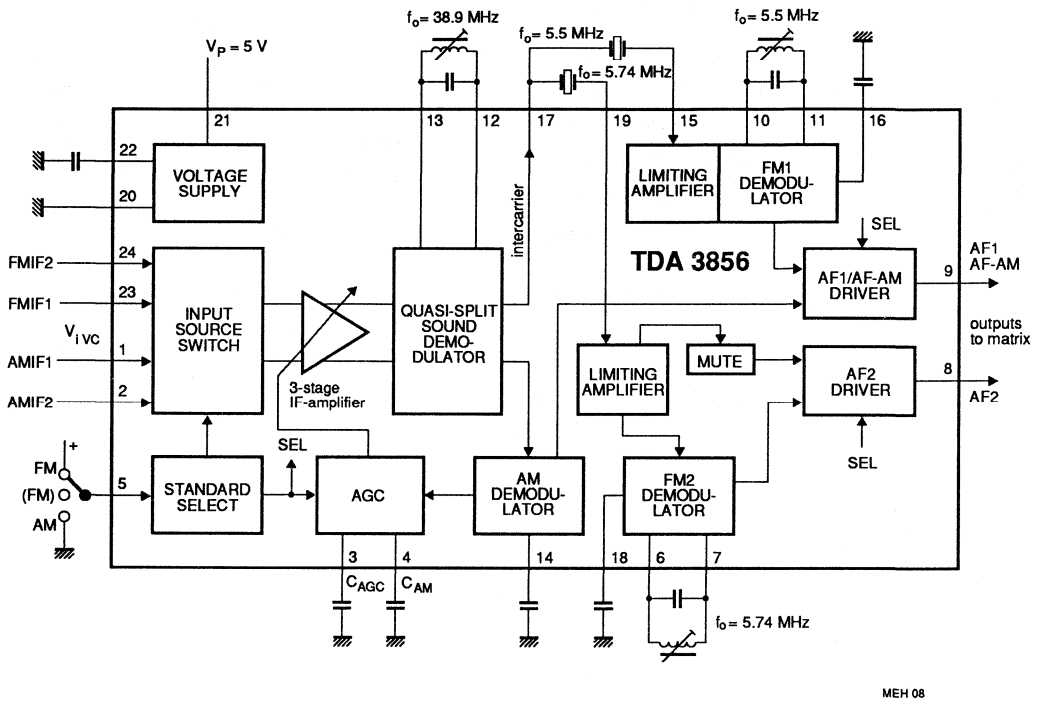


Fig.1 Block diagram (B/G and L).

Quasi-split sound processor for all standards

TDA3856

PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard
C_{AGC}	3	charge capacitor for AGC (FM and AM)
C_{AM}	4	charge capacitor for AM AGC
MODE	5	3-state input for standard select
FM2R1	6	reference circuit for FM2 (5.74 MHz)
FM2R2	7	reference circuit for FM2 (5,74 MHz)
AF2	8	AF2 output (AF out of 5.74 MHz)
AF1	9	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	10	reference circuit for FM1 (5.5 MHz)
FM1R2	11	reference circuit for FM1 (5.5 MHz)
VC-R1	12	reference circuit for the vision carrier (38.9 MHz)
VC-R2	13	reference circuit for the vision carrier (38.9 MHz)
C_{AFAM}	14	DC-decoupling capacitor for AM demodulator (AF-AM)
FM1I	15	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	16	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	17	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	18	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	19	intercarrier input for FM2 (5.74 MHz)
GND	20	ground (0 V)
V_P	21	+5 ... +8 V supply voltage (pin 28 not connected)
C_{ref}	22	charge capacitor for reference voltage
FMIF1	23	IF difference input 1 for B/G standard (38.9 MHz)
FMIF2	24	IF difference input 2 for B/G standard (38.9 MHz)

PIN CONFIGURATION

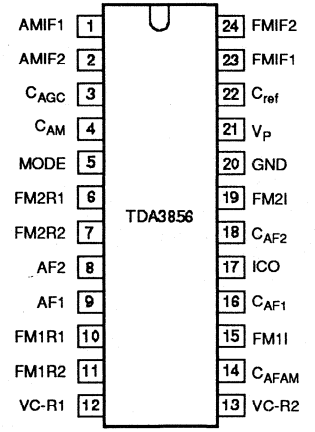


Fig.2 Pin configuration.

Quasi-split sound processor for all standards

TDA3856

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is for all standards. Dependent on the voltage on pin 5 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode):
Pins 23 and 24 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 19 , AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected).

The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.

With 1 mV on pin 19, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 23 and 24 generate noise on pin 19, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise on pin 19 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

L standard (AM mode):
Pins 1 and 2 are active, AGC detector uses mean signal level. The audio signal from the AM demodulator is output on AF1, with AF2 output muted.

The series capacitor C_S in 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to the formula

$$C_S = C_P (f_{VC}/f_{SC})^2 - C_P.$$

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier.
The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.

Measurements at the demodulators:
For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV-demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_{mod} = 1$ kHz; with a deviation of ±30 kHz the S/N ratio is deteriorated by 4.5 dB.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltages (pin 21)	-	8.8	V
V_I	voltage (pins 1, 2, 5, 8, 9, 15, 17, 19, 23 and 24)	0	V_P	V
P_{tot}	total power dissipation	0	650	mW
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling*			
	all pins except 1, 2, 23 and 24	±500	-	V
	pins 1, 2, 23 and 24	+400	-	V
	pins 1, 2, 23 and 24	–500	-	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz. Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 21)		4.5	5	8.8	V
I_P	supply current (pin 21)		48	60	72	mA
IF source control (pin 5)						
V_5	input voltage in order to obtain standards					
	B/G (FM) with automatic muting	pin 5 connected	2.8	-	V_P	V
		pin 5 open-circuit	-	2.8	-	V
	B/G (FM) without muting	pin 5 connected or alternative measure: 22 kΩ to GND	1.3	-	2.3	V
	L (AM sound)	pin 5 connected	0	-	0.8	V
I_5	input current	$V_5 = V_{P1}$	-	-	100	µA
		V_5 = 0	-	-	–300	µA

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF input not activated (pins 1-2 or 23-24)						
R_I	input resistance		-	-	100	Ω
V_I	DC input voltage (pins 1, 2 or 23, 24)	internally set LOW	-	-	0.1	V
$\alpha_{12\text{-}13}$	crosstalk attenuation of IF input switch	note 1	50	56	-	dB
IF amplifier (pins 1-2 or 23-24)						
R_I	input resistance		-	2.2	-	kΩ
C_I	input capacitance		-	2.5	-	pF
V_I	DC potential, voltage (pins 1, 2, 23, 24)		-	1.75	-	V
$V_{i\ IF\ (rms)}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity B/G standard (RMS value, pins 23-24)	–3 dB intercarrier signal reduction at pin 17	-	70	100	μV
	input signal sensivity L standard (RMS value, pins 1-2)	–3 dB intercarrier signal reduction at pin 9	-	70	100	μV
ΔG_v	IF gain control range		60	63	-	dB
B	IF bandwidth	–3 dB	50	70	-	MHz
V_3	voltage range for gain control (pin 3)		1.7	-	2.6	V
Resonance amplifier (pins 12-13)						
$V_{o\ (p\text{-}p)}$	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
$R_{12\text{-}13}$	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 5	-	0.247	-	μH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{12,\ 13}$	DC voltage (pins 12 and 13)		-	V_P–1	-	V
Intercarrier mixer output (pin 17)						
$V_{o\ (rms)}$	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{17}	residual video AM on intercarrier	note 2	-	3	10	%
$V_{VC\ (rms)}$	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{17}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 17)		-	-	±0.7	mA
I_{17}	allowable DC output current		-	-	–2	mA
V_{17}	DC voltage		-	1.75	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiting amplifiers (pins 15 and 19)						
$V_{i\ (rms)}$	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	µV
	maximum input signal (RMS value)		200	-	-	mV
$R_{15, 19}$	input resistance		-	560	-	Ω
$V_{15, 19}$	DC voltage		-	0	-	V
$V_{i\ (rms)}$	level detector threshold for no muting (RMS value, pin 19)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) at pins 15 and 19 without ceramic filters, R_S = 50 Ω. De-emphasis 50 µs and $V_5 = V_P$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 6-7 and 10-11.						
$V_{IC\ (rms)}$	intercarrier signals (RMS values, pins 6-7 and 10-11)		-	100	-	mV
V	DC voltage (pins 6, 7, 10, and 11)		-	1.8	-	V
$V_{o\ (rms)}$	AF output signals (RMS values, pins 8 and 9)		0.84	0.95	1.07	V
ΔV_o	difference of AF signals between channels (pins 8 and 9)		-	-	1	dB
$R_{8, 9}$	output resistance		-	100	-	Ω
$V_{8, 9}$	DC voltage		-	2.1	-	V
$I_{8, 9\ (M)}$	allowed AC current of emitter output (peak value)	note 3	-	-	±1.5	mA
$I_{8, 9}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
$V_{o\ (rms)}$	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 9-8)		60	70	-	dB
$V_{16, 18}$	DC voltage (pins 16 and 18)		-	1.7	-	V

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM mode, input signal at pins 1-2		SC = 32.4 MHz; f_{mod} = 1 kHz, m = 0.8; $V_{i\ AM\ (rms)}$ = 10 mV				
$V_{o\ (rms)}$	AF output signal at pin 9 (RMS value)		530	600	675	mV
R_9	output resistance (pin 9)		-	100	-	Ω
$I_{o\ (M)}$	maximum AC output current (peak value)	note 3	-	-	±1.5	mA
I_9	maximum DC output current		-	-	–2	mA
V_9	DC voltage		-	2.1	-	V
THD	total harmonic distortion	Fig.4	-	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	50	56	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
V_{14}	DC voltage (pin 14)		-	2	-	V
Audio frequency performance for FM operation in B/G standard ($V_5 = V_P$), unless otherwise specified.						
V_o	signals attenuation of AF source selector					
	AF2 at pin 8	$V_5 = V_P$	70	-	-	dB
	for not required signal AF1 at pin 9	5.5 MHz at pin 15; V_5 = 0; V_i = 10 mV	70	-	-	dB
	or not required signal AF1 at pin 9	signal for L standard $V_5 = V_P$	70	-	-	dB
$dV_{8,9}$	DC level deviation (pins 8 and 9)	when switching to FM or AM sound or Mute	-	5	25	mV
AF outputs (pins 8 and 9)						
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3 de-emphasis 50 μs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R=70 Hz $V_{R\ (p-p)}$ = 200 mV	30	40	-	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at $R_{12\text{-}13}$ = 470 Ω (instead of LC circuit); input signal $V_{i\ (rms)}$ = 20 mV (pins 23-24). AGC voltage V_3 set to a value to achive $V_{o\ (rms)}$ = 20 mV (pins 12-13). After switching (V_5 = 0 V) measure attenuation. IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100% picture modulation.)
3. For larger current: R_L > 2.2 kΩ (pin 8 or 9 to GND) in order to increase the bias current of the output emitter follower.

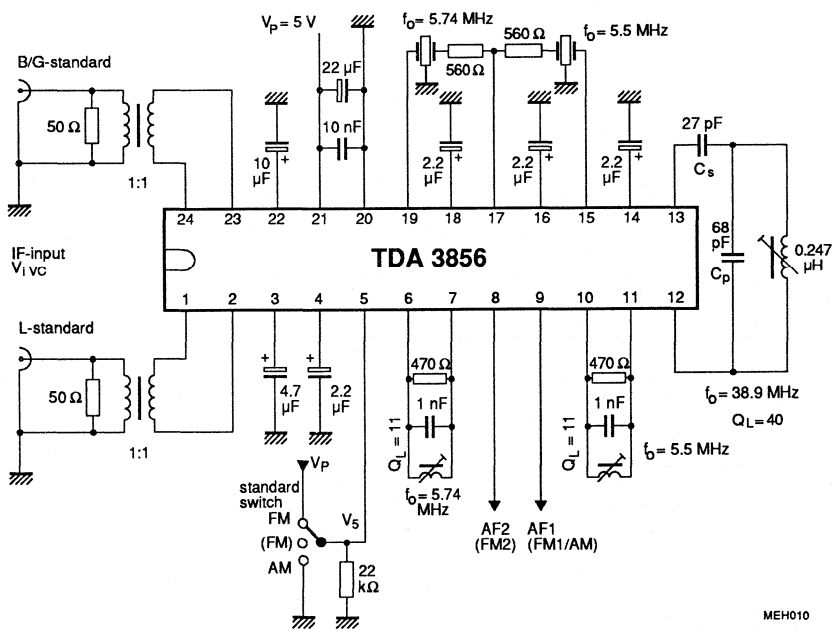


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used).

CHARACTERISTICS (continued)

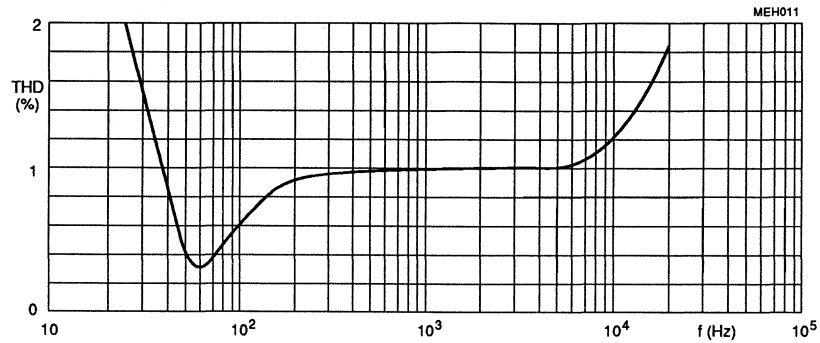
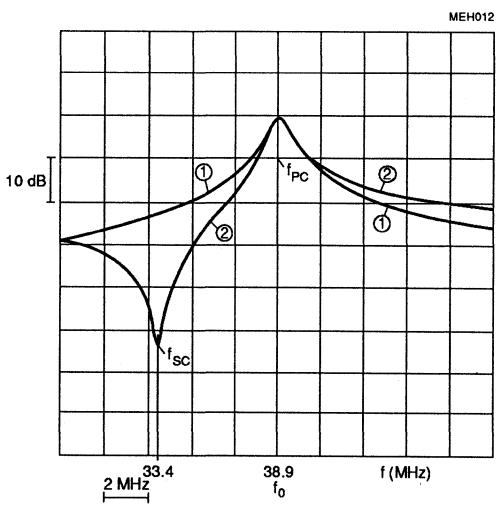


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard ($V_5 = 0$).



(1) simple resonant circuit
(2) resonant circuit with C_P = 68 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION

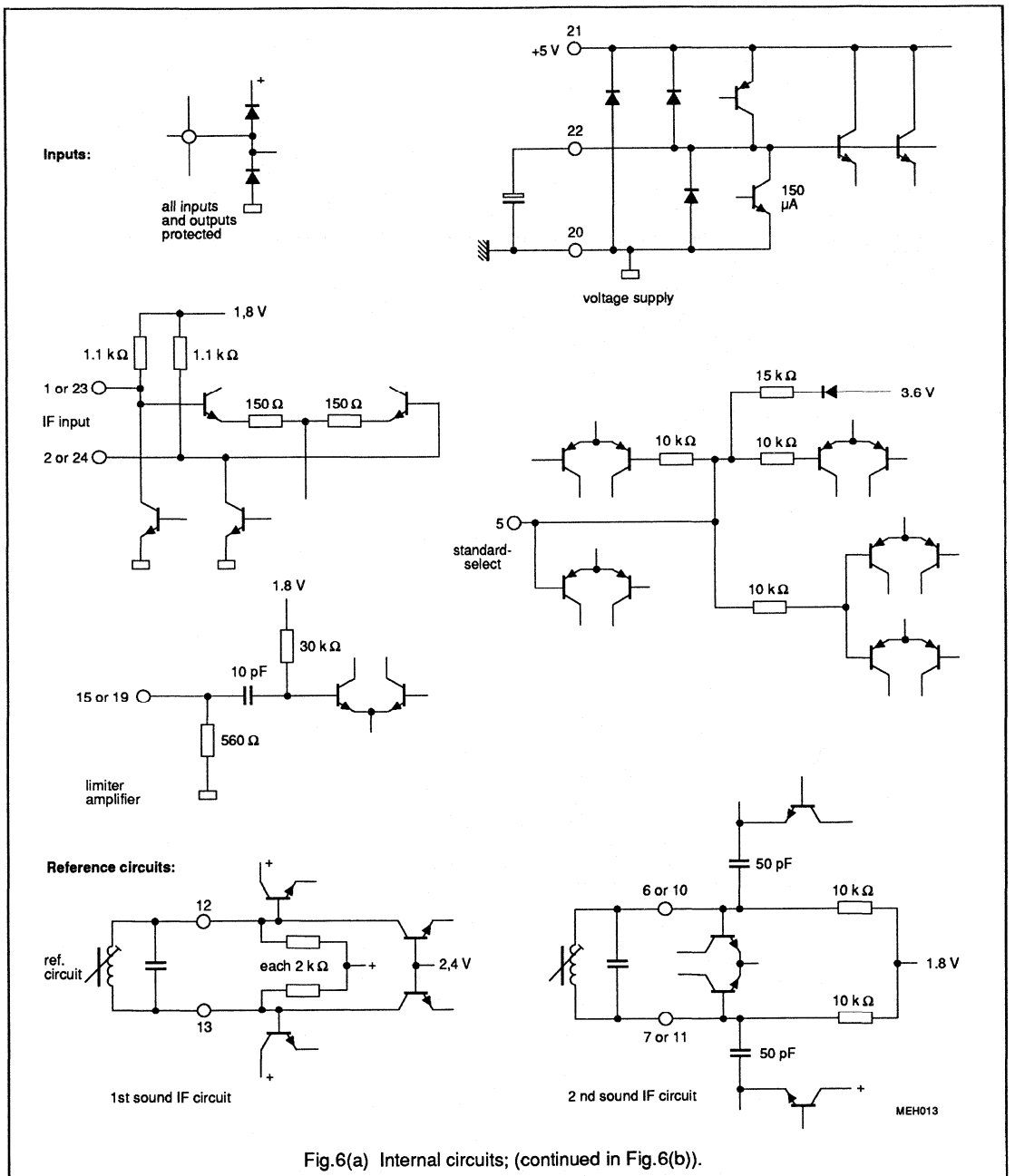


Fig.6(a) Internal circuits; (continued in Fig.6(b)).

APPLICATION INFORMATION (continued)

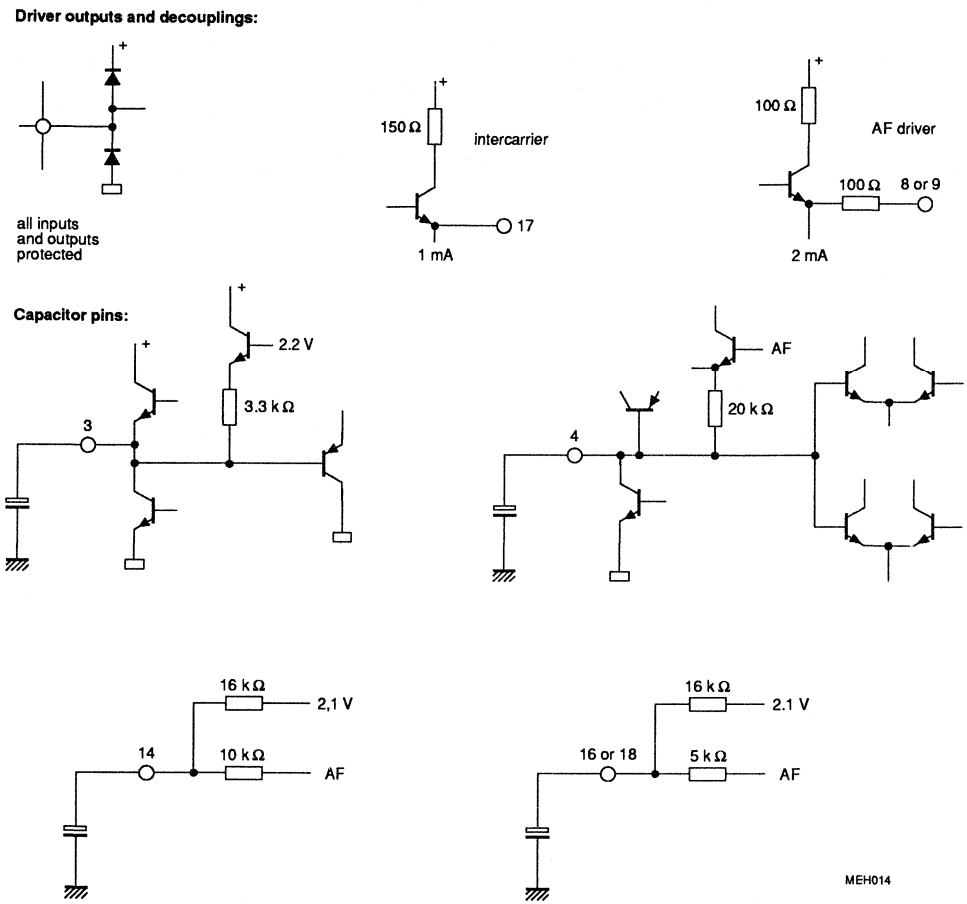


Fig.6(b) Internal circuits; (continued from Fig.6(a)).

Philips Semiconductors

Data sheet	
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TDA3857

Quasi-split sound processor with two FM demodulators

FEATURES

- Quasi-split sound processor for all FM standards e. g. B/G
- Reducing of spurious video signals by tracking function and AFC for the vision carrier reference circuit; (indispensable for NICAM)
- Automatic muting of the AF2 signal (at B/G) by the input level
- Layout-compatible with TDA3856 (24 pins) and TDA3858 (32 pins)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 19)	4.5	5	8.8	V
I_P	supply current	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
$V_{o\ AF}$	audio output signal (RMS value)	-	1	-	V
THD	total harmonic distortion	-	0.5	-	%
S/N(W)	weighted signal-to-noise ratio	-	68	-	dB

GENERAL DESCRIPTION

Symmetrical IF inputs.

Gain controlled wideband IF amplifier.

AGC generation due to peak sync Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3857	20	DIL	plastic	SOT146

Quasi-split sound processor with two FM demodulators

TDA3857

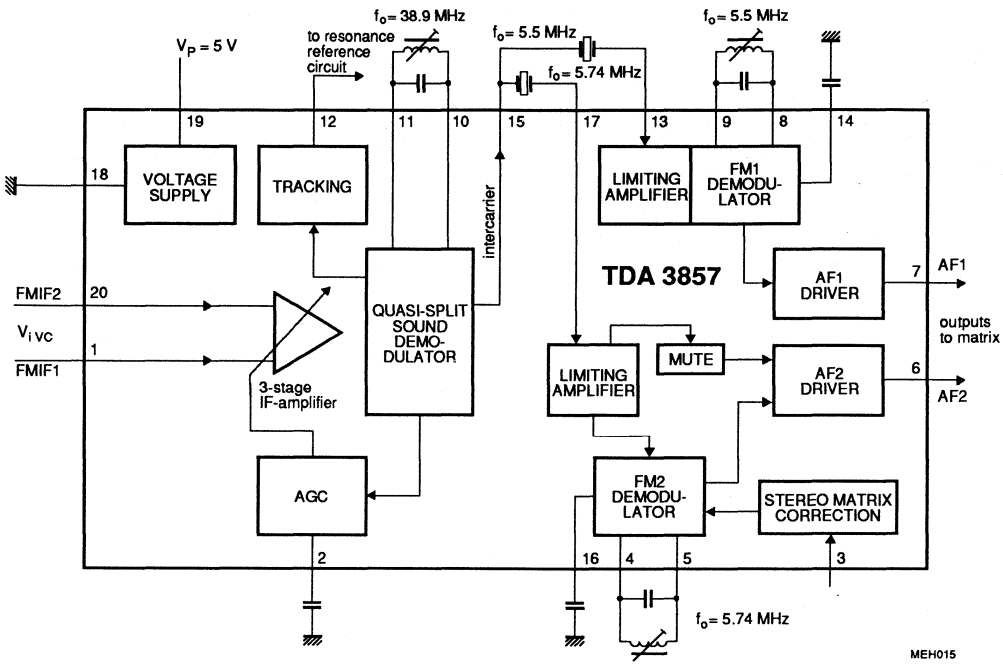


Fig.1 Block diagram (standard B/G).

Quasi-split sound processor with two FM demodulators

TDA3857

PINNING

SYMBOL	PIN	DESCRIPTION
FMIF1	1	IF difference input 1 for B/G standard (38.9 MHz)
C_{AGC}	2	charge capacitor for AM AGC
MATR	3	input for stereo matrix correction
FM2R1	4	reference circuit for FM2 (5.74 MHz)
FM2R2	5	reference circuit for FM2 (5,74 MHz)
AF2	6	AF2 output (AF out of 5.74 MHz)
AF1	7	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	8	reference circuit for FM1 (5.5 MHz)
FM1R2	9	reference circuit for FM1 (5.5 MHz)
VC-R1	10	reference circuit for the vision carrier (38.9 MHz)
VC-R2	11	reference circuit for the vision carrier (38.9 MHz)
TRACK	12	DC output level for tracking
FM1I	13	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	14	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	15	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	16	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	17	intercarrier input for FM2 (5.74 MHz)
GND	18	ground (0 V)
V_P	19	+5 ... +8 V supply voltage (pin 28 not connected)
FMIF2	20	IF difference input 2 for B/G standard (38.9 MHz)

PIN CONFIGURATION

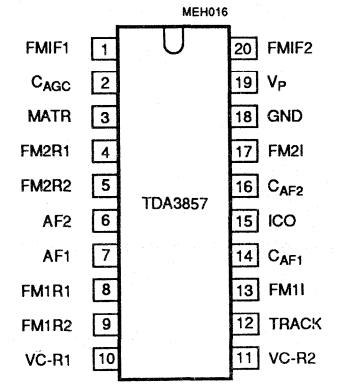


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is suitable for all FM standards (e. g. B/G).

B/G standard:
AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 17 , AF2 output is muted. The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.
With 1 mV on pin 17, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 1 and 20 generate noise on pin 17, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise on pin 17 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

The series capacitor C_s in the 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to

$$C_S = C_P (f_{VC} / f_{SC})^2 - C_P.$$

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier. The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.
Measurements at the demodulators: For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_m = 1$ kHz; with a deviation of ±30 kHz the S/N ratio is deteriorated by 4.5 dB.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltages (pin 19)	-	8.8	V
V_I	voltage (pins 1, 6, 7, 13, 15, 17 and 20)	0	V_P	V
P_{tot}	total power dissipation	0	635	mW
T_{stg}	storage temperature range	−25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling*			
	all pins except 1 and 20	±500	-	V
	pins 1 and 20	+400	-	V
	pins 1 and 20	−500	-	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz.
Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 19)		4.5	5	8.8	V
I_P	supply current (pin 19)		48	60	72	mA
IF amplifier (pins 1 and 20)						
R_I	input resistance		-	2.2	-	kΩ
C_I	input capacitance		-	2.5	-	pF
V_I	DC input voltage		-	1.75	-	V
$V_{i\ IF\ (rms)}$	max input signal (RMS value, pins 1-20)	V_o = +1 dB	70	100	-	mV
	input signal sensivity (RMS value)	−3 dB intercarrier signal reduction at pin 15	-	70	100	μV
ΔG_V	IF gain control range		60	63	-	dB
V_2	voltage range for gain control (pin 2)		1.7	-	2.6	V
B	IF bandwith	−3 dB	50	70	-	MHz

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resonance amplifier (pins 10-11)						
$V_{o\ (p\text{-}p)}$	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
R	operating resistance		-	4	-	kΩ
L	inductance	Fig. 3 and 4	-	0.247	-	μH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonance circuit	Q_o = 90	-	40	-	
$V_{10,\ 11}$	DC voltage (pins 10 and 11)		-	V_P–1	-	V
Intercarrier mixer output (pin 15)						
$V_{o\ (rms)}$	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{15}	residual video AM on intercarrier	note 1	-	3	10	%
$V_{VC\ (rms)}$	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{15}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 15)		-	-	±0.7	mA
I_{15}	allowable DC output current		-	-	–2	mA
V_{15}	DC voltage		-	1.75	-	V
Limiting amplifiers (pins 13 and 17)						
$V_{i\ (rms)}$	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	μV
	maximum input signal (RMS value)		200	-	-	mV
$R_{13,\ 17}$	input resistance		-	560	-	Ω
$V_{13,\ 17}$	DC voltage		-	0	-	V
$V_{i\ (rms)}$	level detector threshold for no muting (RMS value, pin 17)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM1 and FM2 demodulators Measurements with FM-IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) at pins 13 and 17 without ceramic filters, $R_S = 50\ \Omega$. De-emphasis 50 µs. Q_L-factor = 11 for resonant circuits at pins 4-5 and 8-9.						
$V_{IC\ (rms)}$	intercarrier signals (RMS values, pins 4-5 and 8-9)		-	100	-	mV
V	DC voltage (pins 4, 5, 8, and 9)		-	1.8	-	V
$V_{o\ (rms)}$	AF output signals (RMS values, pins 6 and 7)		0.84	0.95	1.07	V
ΔV_o	difference of AF signals between channels (pins 6 and 7)	note 2	-	-	1	dB
$R_{6,7}$	output resistance		-	100	-	Ω
$V_{6,7}$	DC voltage		-	2.1	-	V
$I_{6,7(M)}$	allowed AC current of emitter output (peak value)	note 3	-	-	±1.5	mA
$I_{6,7}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
$V_{o\ (rms)}$	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 6-7)		60	70	-	dB
V_3	adjusting voltage for AF2 signal (pin 3)	note 4	0	-	5	V
ΔG_{AF2}	minimum gain range due to V_3		–1.5	-	1.0	dB
	typical gain range due to V_3		–2.5	-	1.5	dB
$V_{14,16}$	DC voltage (pins 14 and 16)		-	1.7	-	V
Tracking automatic frequency control (AFC) of the vision carrier reference circuit.						
$V_{o\ 12}$	tracking output voltage range (pin 12)	note 5	V_P–3.3	-	V_P–1	V
F_{TR}	tracking reducing factor for					
	black picture		-	9	-	
	white test picture		-	4	-	
	50 % grey picture		-	6	-	
S	AFC steepness (open loop) for					
	black picture		-	–8	-	mV/kHz
	white test picture		-	–3	-	mV/kHz
	50 % grey picture		-	–5.5	-	mV/kHz

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio frequency performance for FM operation in B/G standard, unless otherwise specified.						
V_o	signals attenuation of AF source selector	AF2 at pin 6	70	-	-	dB
$dV_{6,7}$	DC level deviation (pins 6 and 7)	when switching to FM or AM sound or Mute	-	5	25	mV
AF outputs (pins 6 and 7)						
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3 de-emphasis 50 µs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R=70 Hz $V_{R\ (p-p)}$ = 200 mV	30	40	-	dB

Notes to the characteristics

1. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100 % picture modulation.)
2. AF signal can be adjusted by V_3
3. For larger current: R_L > 2.2 kΩ (pin 6 or 7 to GND) in order to increase the bias current of the output emitter follower.
4. If not used, pin 3 should not be connected.
5. Automatic frequency control (AFC) of the vision carrier reference circuit (pins 10 and 11) for reducing spurious video signals in the stereo/dual sound modes. The factor of reducing F_{TR} at a deviation Δf_{VC} specifies the ratio of spurious signals with/without tracking function.

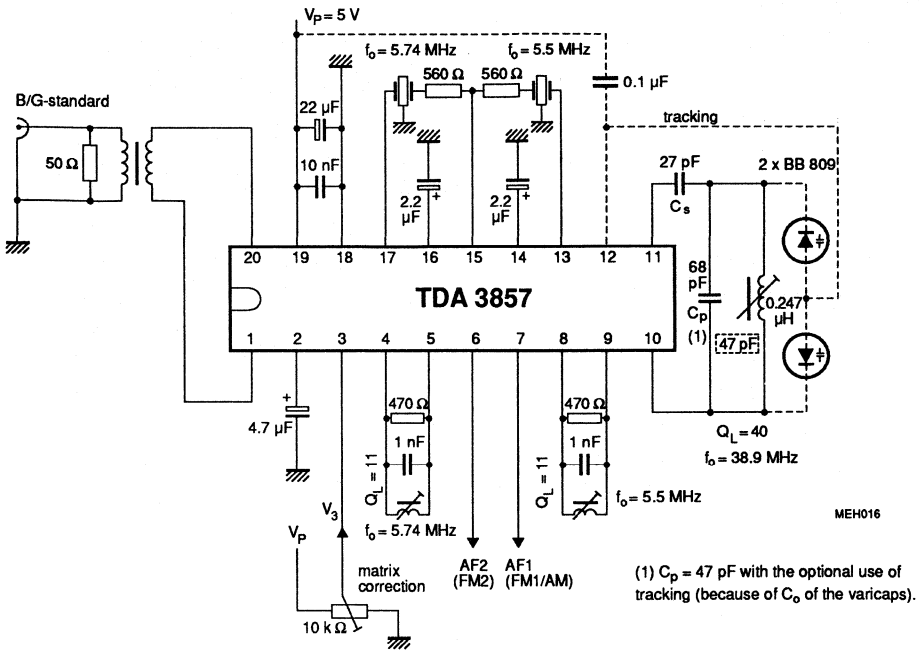
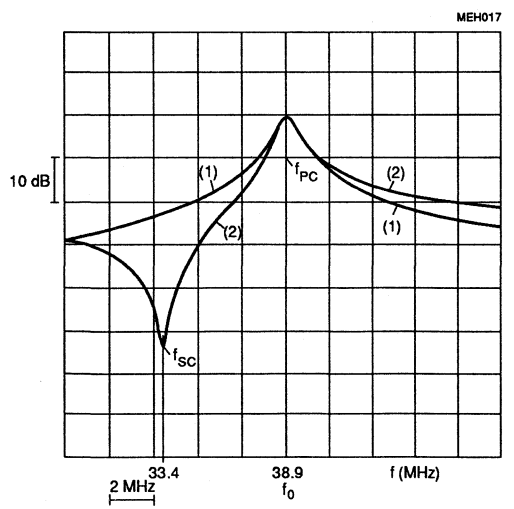


Fig.3 Test and application circuit for standard B/G (for application SAW-filter must be used).



(1) simple resonant circuit
(2) resonant circuit with C_P = 68 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.4 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION

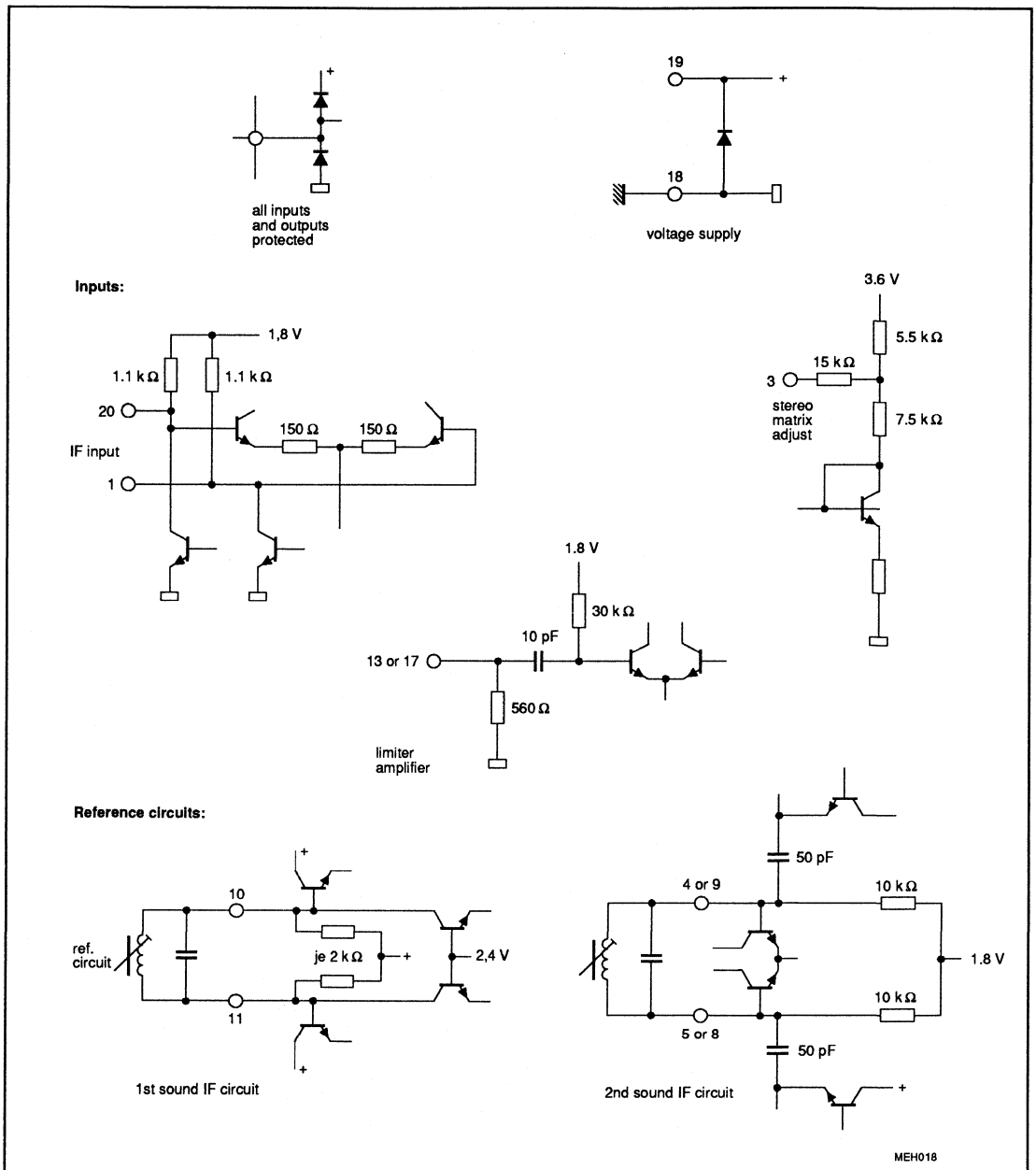


Fig.5(a) Internal circuits; (continued in Fig.5(b)).

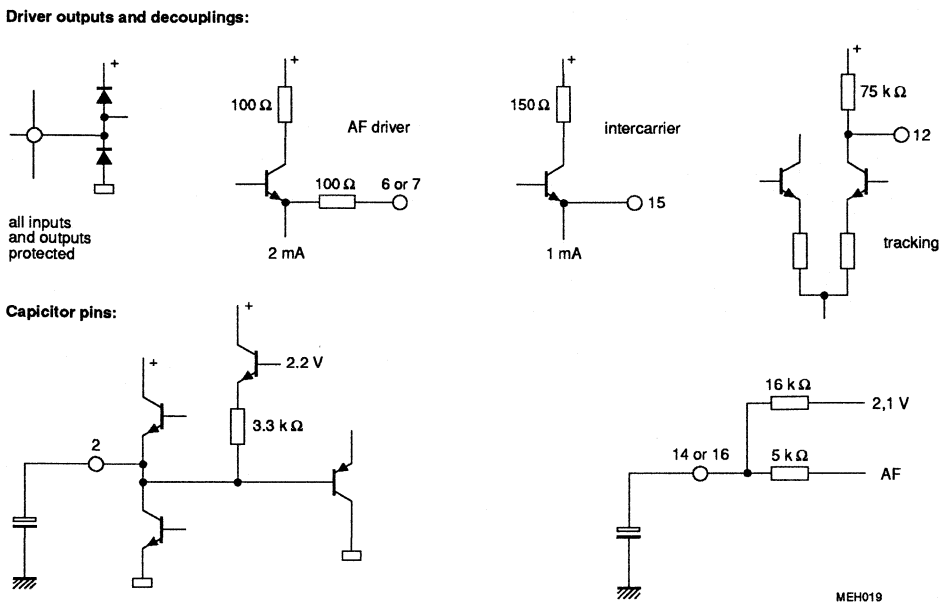


Fig.5(b) Internal circuits; (continued from Fig.5(a)).

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA3858

Quasi-split sound processor for all standards

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- Reducing of spurious video signals by tracking function and AFC for the vision carrier reference circuit; (indispensable for NICAM)
- Automatic muting of the AF2 signal (at B/G) by the input level
- AM signal processing for L standard and switching over the audio signal
- Stereo-matrix correction
- Layout-compatible with TDA3856 (24 pins) and TDA3857 (20 pins)

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM or AM sound.

Gain controlled wideband IF amplifier, input select switch.

AGC generation due to peak sync for FM or mean signal level for AM.

Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (pin 27)	4.5	5	8.8	V
V_{P2}	alternative supply voltage (pin 28)	10.8	12	13.2	V
Data at V_{P1} = 5 V					
I_P	supply current (pin 27)	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
$V_{o\ (rms)}$	audio output signal for FM (B/G)	-	1	-	V
$V_{o\ (rms)}$	audio output signal for AM (L)	-	0.6	-	V
THD	total harmonic distortion				
	for FM	-	0.5	-	%
	for AM	-	1	-	%
S/N (W)	weighted signal-to-noise ratio				
	for FM	-	68	-	dB
	for AM	-	56	-	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3858	32	shrink DIL	plastic	SOT232

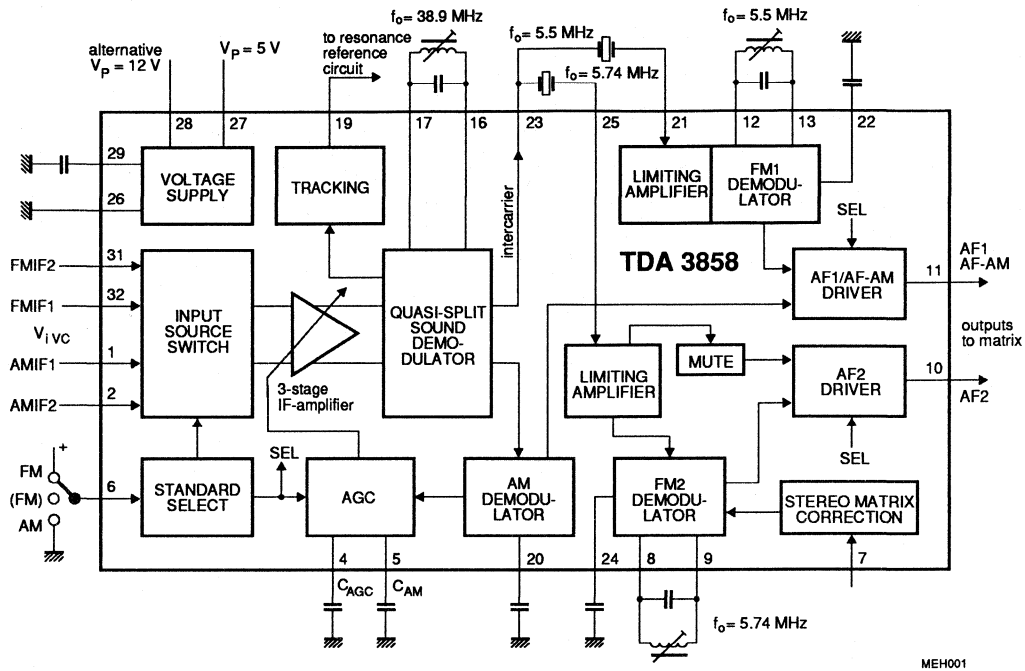


Fig.1 Block diagram (B/G and L standards).

Quasi-split sound processor for all standards

TDA3858

PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard
n.c.	3	not connected
C_{AGC}	4	charge capacitor for AGC (FM and AM)
C_{AM}	5	charge capacitor for AM AGC
MODE	6	3-state input for standard select
MATR	7	input for stereo matrix correction
FM2R1	8	reference circuit for FM2 (5.74 MHz)
FM2R2	9	reference circuit for FM2 (5,74 MHz)
AF2	10	AF2 output (AF out of 5.74 MHz)
AF1	11	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	12	reference circuit for FM1 (5.5 MHz)
FM1R2	13	reference circuit for FM1 (5.5 MHz)
n.c.	14	not connected
n.c.	15	not connected
VC-R1	16	reference circuit for the vision carrier (38.9 MHz)
VC-R2	17	reference circuit for the vision carrier (38.9 MHz)
n.c.	18	not connected
TRACK	19	DC output level for tracking
C_{AFAM}	20	DC-decoupling capacitor for AM demodulator (AF AM)
FM1I	21	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	22	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	23	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	24	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	25	intercarrier input for FM2 (5.74 MHz)
GND	26	ground (0 V)
V_{P1}	27	+5 to +8 V supply voltage (pin 28 not connected)
V_{P2}	28	+12 V supply voltage (pin 27 not connected)
C_{ref}	29	charge capacitor for reference voltage
n.c.	30	not connected
FMIF1	31	IF difference input 1 (B/G standard, 38.9 MHz)
FMIF2	32	IF difference input 2 (B/G standard, 38.9 MHz)

PIN CONFIGURATION

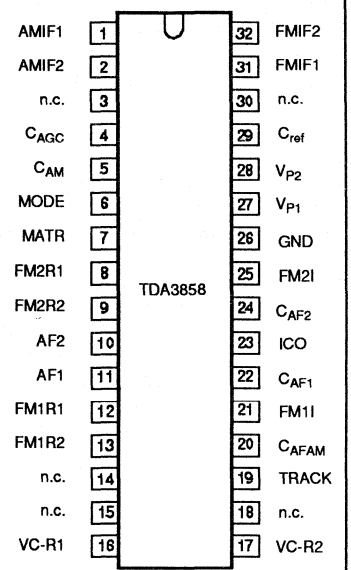


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is for all standards. Dependent on the voltage on pin 6 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode):
Pins 31 and 32 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 25 , AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected). The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.
With 1 mV on pin 25, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals on pins 31 and 32 generate noise on pin 25, which is present in the intercarrier signal and passes through the 5,74 MHz filter. Noise on pin 25 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

L standard (AM mode):
Pins 1 and 2 are active, AGC detector uses mean signal level.The audio signal from the AM demodulator is output on AF1, with AF2 output muted.

The series capacitor C_s in 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to
$C_S = C_P (f_{VC} / f_{SC})^2 - C_P$.

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier. The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.
Measurements at the demodulators:
For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV-demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_m = 1$ kHz; with a deviation of ±30 kHz the S/N ratio is deteriorated by 4.5 dB.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltages (pin 27)	-	8.8	V
V_{P2}	supply voltages (pin 28)	-	13.2	V
V_I	voltage (pins 1, 2, 6, 10, 11, 21, 23, 25, 31 and 32)	0	V_P	V
$V_{I)}$	voltage at 12 V supply (pin 6)	0	5.5	V
P_{tot}	total power dissipation	0	950	mW
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling*			
	all pins except 1, 2, 31 and 32	±500	-	V
	pins 1, 2, 31 and 32	+400	-	V
	pins 1, 2, 31 and 32	–500	-	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_{P1} = 5 V (pin 27) and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz.
Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage.range (pin 27)	pin 28 not connected	4.5	5	8.8	V
V_{P2}	supply voltage.range (pin 28)	pin 27 not connected	10.8	12	13.2	V
I_{P1}	supply current (pin 27)	V_{P1} = 5 V	48	60	72	mA
IF input not activated (pins 1-2 or 31-32)						
R_I	input resistance		-	-	100	Ω
V_I	DC input voltage (pins 1-2 or 31-32)	LOW internal set	-	-	0.1	V
$\alpha_{16\text{-}17}$	crosstalk attenuation of IF input switch	note 1	50	56	-	dB

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF source control (pin 6)						
V_6	input voltage in order to obtain standards					
	B/G (FM) with automatic muting	pin 6 connected	2.8	-	V_{P1}	V
		pin 6 open-circuit	-	2.8	-	V
	B/G (FM) without muting	pin 6 connected	1.3	-	2.3	V
		or alternative measure: 22 kΩ to GND				
	L (AM sound)	pin 6 connected	0	-	0.8	V
I_6	input current	$V_6 = V_{P1}$	-	-	100	µA
		$V_6 = 0$	-	-	–300	µA
$V_{6\ (12\ V)}$	maximum input voltage (pin 6)	supply at pin 28	-	-	5.5	V
IF amplifier (pins 31-32 or 1-2)						
R_I	input resistance		-	2.2	-	kΩ
C_I	input capacitance		-	2.5	-	pF
V_I	DC potential, voltage (pins 1, 2, 31, 32)		-	1.75	-	V
$V_{i\ IF\ (rms)}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity B/G standard (RMS value, pins 31-32)	–3 dB intercarrier signal reduction at pin 23	-	70	100	µV
	input signal sensivity L standard (RMS value, pins 1-2)	–3 dB intercarrier signal reduction at pin 11	-	70	100	µV
ΔG_v	IF gain control range		60	63	-	dB
B	IF bandwidth	–3 dB	50	70	-	MHz
V_4	voltage range for gain control (pin 4)		1.7	-	2.6	V
Resonance amplifier (pins 16-17)						
$V_{o\ (p\text{-}p)}$	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
$R_{16\text{-}17}$	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 5	-	0.247	-	µH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{16,\ 17}$	DC voltage (pins 16 and 17)		-	V_P–1	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Intercarrier mixer output (pin 23)						
$V_{o\ (rms)}$	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{23}	residual video AM on intercarrier	note 2	-	3	10	%
$V_{VC\ (rms)}$	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{23}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 23)		-	-	±0.7	mA
I_{23}	allowable DC output current		-	-	–2	mA
V_{23}	DC voltage		-	1.75	-	V
Limiting amplifiers (pins 21 and 25)						
$V_{i\ (rms)}$	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	μV
	maximum input signal (RMS value)		200	-	-	mV
$R_{21,\ 25}$	input resistance		-	560	-	Ω
$V_{21,\ 25}$	DC voltage		-	0	-	V
$V_{i\ (rms)}$	level detector threshold for no muting (RMS value, pin 25)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB
Tracking automatic frequency control (AFC) of the vision carrier reference circuit.						
V_o	tracking output voltage range (pin 19)	note 3	V_{P1}–3.3	-	V_{P1}–1	V
F_{TR}	tracking reducing factor for					
	black picture		-	9	-	
	white test picture		-	4	-	
	50 % grey picture		-	6	-	
S	AFC steepness (open loop) for					
	black picture		-	–8	-	mV/kHz
	white test picture		-	–3	-	mV/kHz
	50 % grey picture		-	–5.5	-	mV/kHz

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) at pins 21 and 25 without ceramic filters, $R_S = 50\ \Omega$. De-emphasis 50 μs and $V_6 = V_{P1}$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 8-9 and 12-13.						
$V_{IC\ (rms)}$	intercarrier signals (RMS values, pins 8-9 and 12-13)		-	100	-	mV
V	DC voltage (pins 8, 9, 12, and 13)		-	1.8	-	V
$V_{o\ (rms)}$	AF output signals (RMS values, pins 10 and 11)		0.84	0.95	1.07	V
ΔV_o	difference of AF signals between channels (pins 10 and 11)	note 4	-	-	1	dB
$R_{10, 11}$	output resistance		-	100	-	Ω
$V_{10, 11}$	DC voltage		-	2.1	-	V
$I_{10, 11(M)}$	allowed AC current of emitter output (peak value)	note 5	-	-	±1.5	mA
$I_{10, 11}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
$V_{o\ (rms)}$	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 10-11)		60	70	-	dB
V_7	adjusting voltage for AF2 signal (pin 7)	note 6	0	-	5	V
ΔG_{AF2}	minimum gain range due to V_7		–1.5	-	1.0	dB
ΔG_{AF2}	typical gain range due to V_7		–2.5	-	1.5	dB
$V_{22, 24}$	DC voltage (pins 22 and 24)		-	1.7	-	V
AM mode, input signal at pins 1-2		SC = 32.4 MHz; f_{mod} = 1 kHz, m = 0.8; $V_{i\ AM\ (rms)}$ = 10 mV				
$V_{o\ (rms)}$	AF output signal at pin 11 (RMS value)		530	600	675	mV
R_{11}	output resistance (pin 11)		-	100	-	Ω
$I_{o\ (M)}$	maximum AC output current (peak value)	note 5	-	-	±1.5	mA
I_{11}	maximum DC output current		-	-	–2	mA
V_{11}	DC voltage		-	2.1	-	V
THD	total harmonic distortion	Fig.4	-	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	50	56	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
V_{20}	DC voltage (pin 20)		-	2	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio frequency performance for FM operation in B/G standard ($V_6 = V_P$), unless otherwise specified.						
V_o	signals attenuation of AF source selector					
	AF2 at pin 10	$V_6 = V_P$	70	-	-	dB
	for not required signal AF1 at pin 11	5.5 MHz at pin 21; $V_6 = 0$; $V_i = 10$ mV	70	-	-	dB
	or not required signal AF1 at pin 11	signal for L standard $V_6 = V_P$	70	-	-	dB
$dV_{10, 11}$	DC level deviation (pins 10 and 11)	when switching to FM or AM sound or Mute	-	5	25	mV
AF outputs (pins 10 and 11)						
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3 de-emphasis 50 µs				
	black picture	$f_i = 5.5$ MHz	59	63	-	dB
	2T/20T pulses with white bar	$f_i = 5.5$ MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	$f_i = 5.5$ MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	$f_i = 5.5$ MHz	50	56	-	dB
	black picture	$f_i = 5.742$ MHz	57	61	-	dB
	2T/20T pulses with white bar	$f_i = 5.742$ MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	$f_i = 5.742$ MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	$f_i = 5.742$ MHz	50	56	-	dB
RR	ripple rejection	all standards: f_R=70 Hz $V_{R\ (p-p)} = 200$ mV	30	40	-	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at $R_{16-17} = 470\ \Omega$ (instead of LC circuit); input signal $V_{i\ (rms)} = 20$ mV (pins 31-32). AGC voltage V_4 set to a value to achive $V_{o\ (rms)} = 20$ mV (pins 16-17). After switching ($V_6 = 0$ V) measure attenuation. IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100 % picture modulation.)
3. Automatic frequency control (AFC) of the vision carrier reference circuit (pins 16 and 17) for reducing spurious video signals in the stereo/dual sound modes. The factor of reducing F_{TR} at a deviation Δf_{VC} specifies the ratio of spurious signals with/without tracking function.
4. AF signal can be adjusted by V_7
5. For larger current: $R_L > 2.2$ kΩ (pin 10 or 11 to GND) in order to increase the bias current of the output emitter follower.
6. If not used, pin 7 should not be connected.

CHARACTERISTICS (continued)

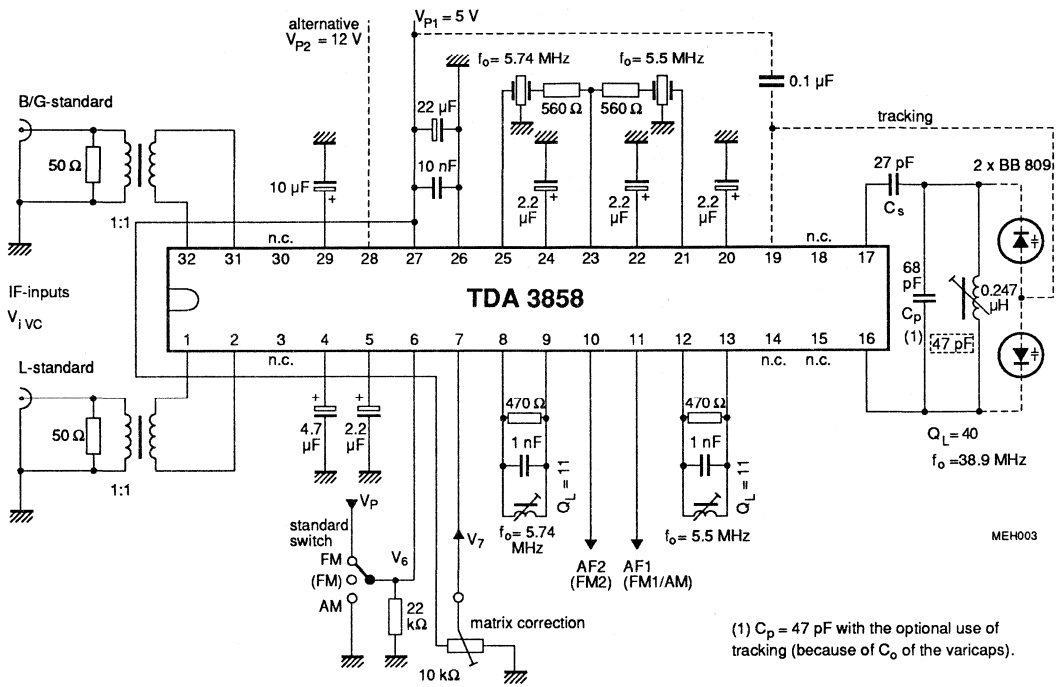


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used). For 12 V supply at pin 28, the capacitors shown at pin 27 must be connected to pin 28.

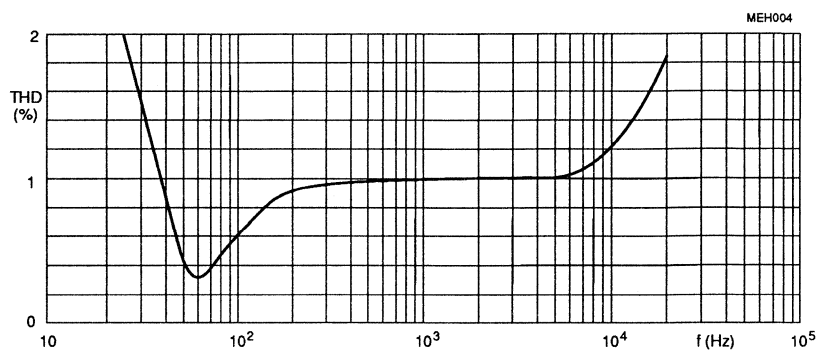
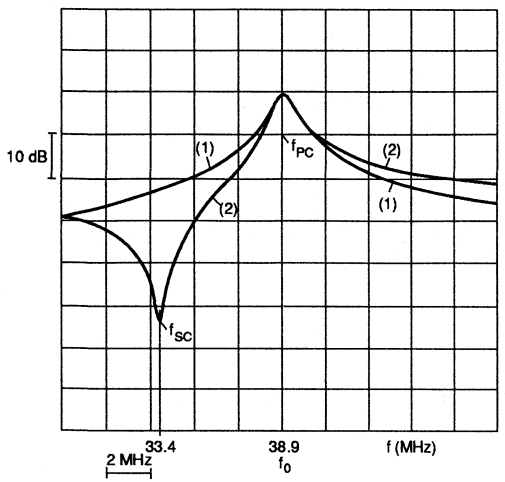


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard (V_6 = 0).

APPLICATION INFORMATION



(1) simple resonant circuit
(2) resonant circuit with C_P = 68 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION (continued)

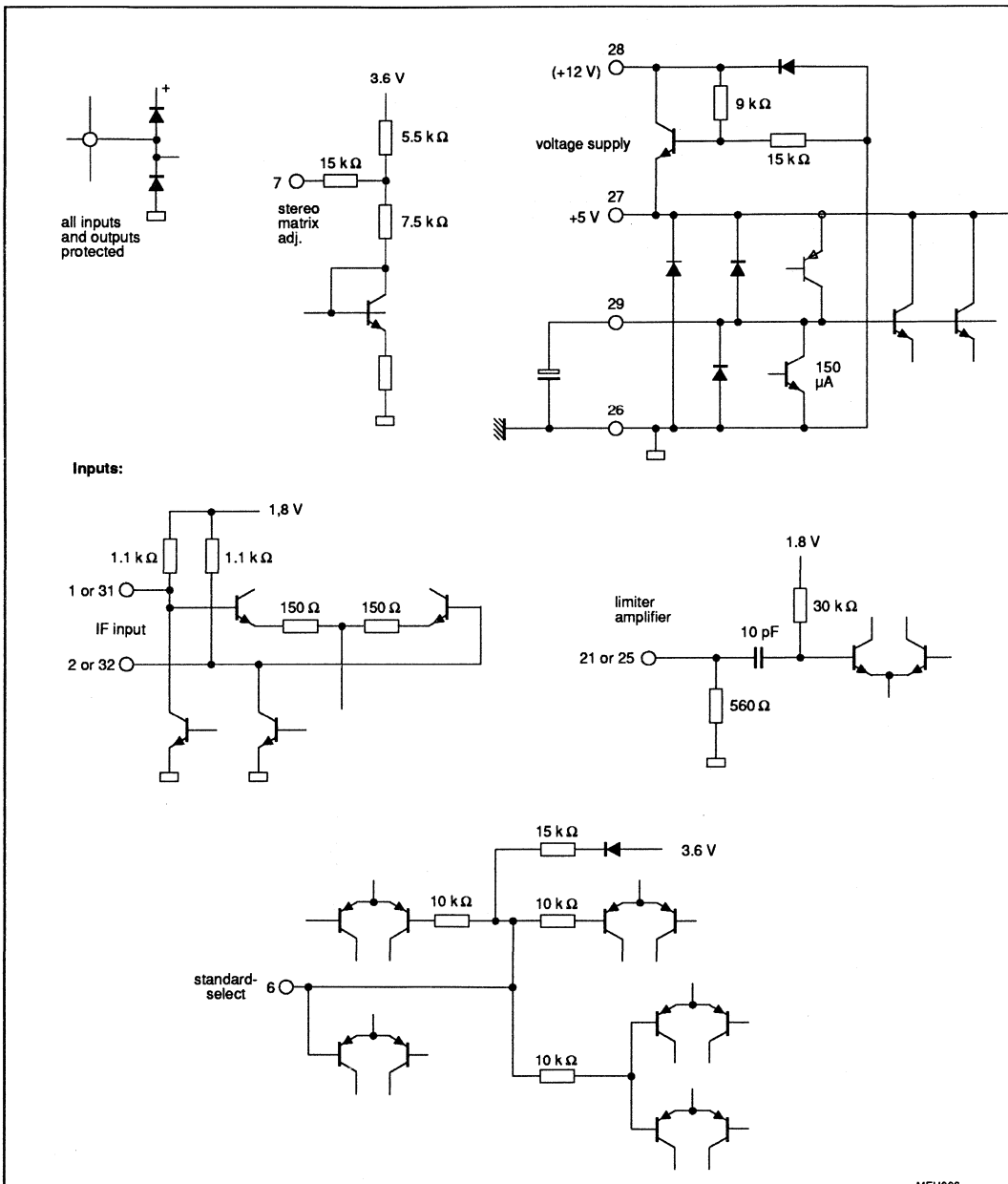


Fig.6(a) Internal circuits; (continued in Fig.6(b)).

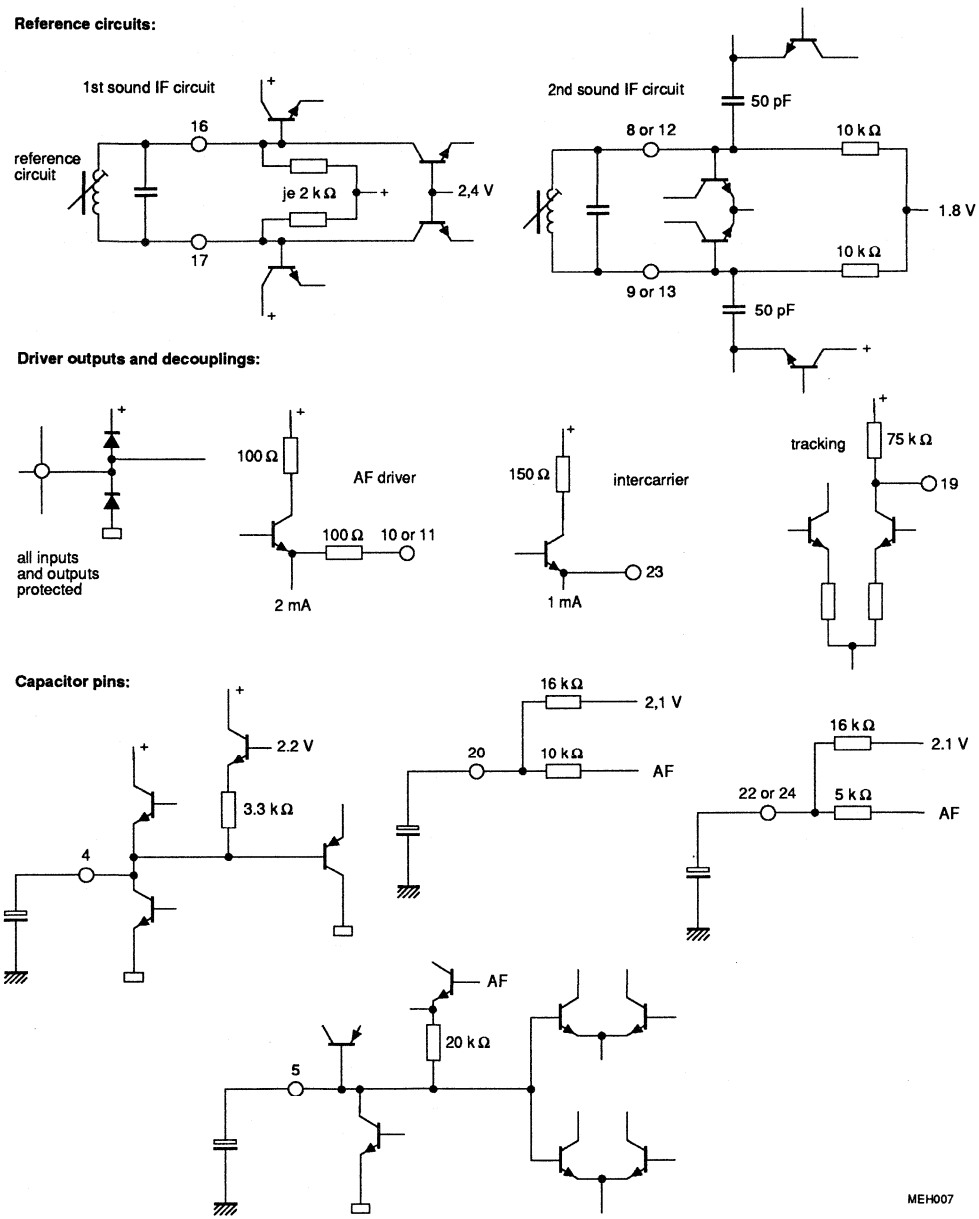


Fig.6(b) Internal circuits; (continued from Fig.6(a)).

Data sheet	
status	Preliminary specification
date of issue	January 1992

TDA3866
Quasi-split sound processor for all standards

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- AF2 signal automatically muted (at B/G) by the input signal level
- AM signal processing for L standard and switching over the audio signal
- Stereo-matrix correction
- Layout-compatible with TDA3858 (32 pins) and TDA3857 (20 pins)
- AM output level typically 500 mV at m = 0.54 (+2.5 dB in comparison to TDA 3856)

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM or AM sound.

Gain controlled wideband IF amplifier, input select switch.

AGC generation due to peak sync for FM or mean signal level for AM.

Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 21)	4.5	5	8.8	V
I_P	supply current	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
V_o	audio output signal for FM standard B/G (RMS value)	-	1	-	V
	audio output signal for AM standard L (RMS value)	-	0.5	-	V
THD	total harmonic distortion				
	for FM	-	0.5	-	%
	for AM	-	1	-	%
S/N (W)	weighted signal-to-noise ratio				
	for FM	-	68	-	dB
	for AM	-	56	-	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3866	24	shrink DIL	plastic	SOT234

Quasi-split sound processor for all standards

TDA3866

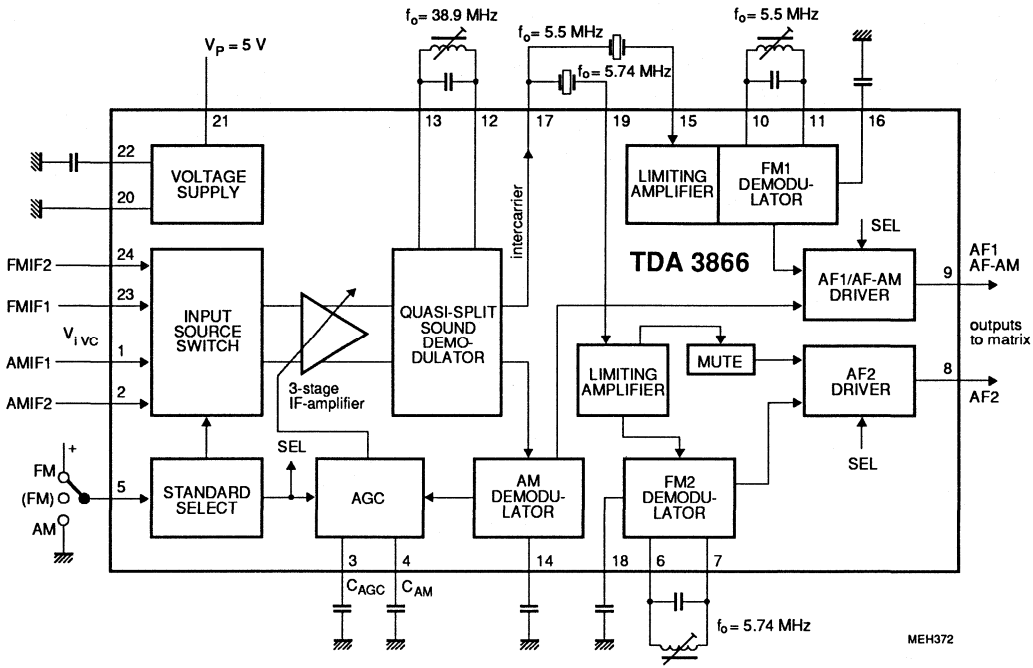


Fig.1 Block diagram (B/G and L).

Quasi-split sound processor for all standards

TDA3866

PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard
C_{AGC}	3	charge capacitor for AGC (FM and AM)
C_{AM}	4	charge capacitor for AM AGC
MODE	5	3-state input for standard select
FM2R1	6	reference circuit for FM2 (5.74 MHz)
FM2R2	7	reference circuit for FM2 (5,74 MHz)
AF2	8	AF2 output (AF out of 5.74 MHz)
AF1	9	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	10	reference circuit for FM1 (5.5 MHz)
FM1R2	11	reference circuit for FM1 (5.5 MHz)
VC-R1	12	reference circuit for the vision carrier (38.9 MHz)
VC-R2	13	reference circuit for the vision carrier (38.9 MHz)
C_{AFAM}	14	DC-decoupling capacitor for AM demodulator (AF-AM)
FM1I	15	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	16	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	17	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	18	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	19	intercarrier input for FM2 (5.74 MHz)
GND	20	ground (0 V)
V_P	21	+5 ... +8 V supply voltage
C_{ref}	22	charge capacitor for reference voltage
FMIF1	23	IF difference input 1 for B/G standard (38.9 MHz)
FMIF2	24	IF difference input 2 for B/G standard (38.9 MHz)

PIN CONFIGURATION

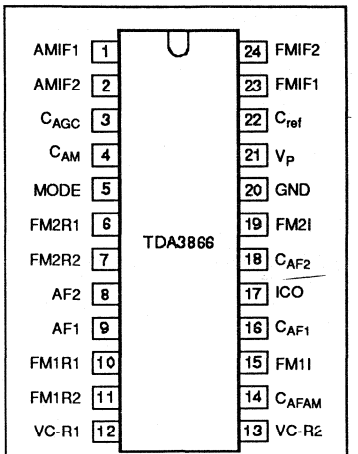


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is for all standards. Dependent on the voltage on pin 5 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode):
Pins 23 and 24 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 19 , AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected).

The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.

With 1 mV on pin 19, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 23 and 24 generate noise on pin 19, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise on pin 19 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

The series capacitor C_S in 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to the formula

$$C_S = C_P (f_{VC}/f_{SC})^2 - C_P.$$

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier.
The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.

Measurements at the demodulators:
For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV-demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_{mod} = 1$ kHz; with a deviation of ± 27 kHz the S/N ratio is deteriorated by 5.3 dB.

L standard (AM mode):
Pins 1 and 2 are active, AGC detector uses mean signal level. The audio signal from the AM demodulator is output on AF1, with AF2 output muted.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltages (pin 21)	-	8.8	V
V_n	input and output voltage (pins 1, 2, 5, 8, 9, 15, 17, 19, 23 and 24)	0	V_P	V
P_{tot}	total power dissipation	0	635	mW
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* all pins except 1, 2, 23 and 24	±500	-	V
	pins 1, 2, 23 and 24	+400	-	V
	pins 1, 2, 23 and 24	–500	-	V

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz. Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = 50 kHz unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 21)		4.5	5	8.8	V
I_P	supply current (pin 21)		48	60	72	mA
IF source control (pin 5)						
V_5	input voltage in order to obtain standards					
	B/G (FM) with automatic muting	pin 5 connected	2.8	-	V_P	V
		pin 5 open-circuit	-	2.8	-	V
	B/G (FM) without muting	pin 5 connected	1.3	-	2.3	V
		22 kΩ to GND (alternative measure)	-	1.8	-	V
	L (AM sound)	pin 5 connected	0	-	0.8	V
I_5	input current	$V_5 = V_P$	-	-	100	μA
		V_5 = 0	-	-	–300	μA

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF input not activated (pins 1-2 or 23-24)						
R_I	input resistance		-	-	100	Ω
V_{DC}	DC input voltage (pins 1, 2, 23 and 24)	internally set LOW	-	-	0.1	V
$\alpha_{1,2\text{-}23,24}$	crosstalk attenuation of IF input switch	note 1	50	56	-	dB
IF amplifier (pins 1-2 or 23-24)						
R_I	input resistance		1.75	2.2	2.65	kΩ
C_I	input capacitance		1.0	1.5	2.2	pF
V_I	DC potential, voltage (pins 1, 2, 23, 24)		-	1.75	-	V
$V_{i\ IF}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity B/G standard (RMS value, pins 23-24)	–3 dB intercarrier signal reduction on pin 17	-	70	100	μV
	input signal sensivity L standard (RMS value, pins 1-2)	–3 dB intercarrier signal reduction on pin 9	-	70	100	μV
ΔG_v	IF gain control range		60	63	-	dB
B	IF bandwidth	–3 dB	50	70	-	MHz
V_3	voltage range for gain control (pin 3)	$G_{min} - G_{max}$	1.7	-	2.6	V
Resonance amplifier (pins 12-13)						
V_o	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
$R_{12\text{-}13}$	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 5	-	0.247	-	μH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{12,\ 13}$	DC voltage (pins 12 and 13)		-	V_P–1	-	V
Intercarrier mixer output (pin 17)						
V_o	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{17}	residual video AM on intercarrier	note 2	-	3	10	%
V_{VC}	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{17}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 17)		-	-	±0.7	mA
I_{17}	allowable DC output current		-	-	–2	mA
V_{17}	DC voltage		-	1.75	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiting amplifiers (pins 15 and 19)						
V_i	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	μV
	maximum input signal (RMS value)		200	-	-	mV
$R_{15, 19}$	input resistance		-	560	-	Ω
$V_{15, 19}$	DC voltage		-	0	-	V
V_i	level detector threshold for no muting (RMS value, pin 19)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) at pins 15 and 19 without ceramic filters, R_S = 50 Ω. De-emphasis 50 μs and $V_5 = V_P$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 6-7 and 10-11.						
V_{IC}	intercarrier signals (RMS values, pins 6-7 and 10-11)		-	100	-	mV
V_{DC}	DC voltage (pins 6, 7, 10, and 11)		-	1.8	-	V
V_o	AF output signals (RMS values, pins 8 and 9)		0.75	0.95	1.20	V
ΔV_o	difference of AF signals between channels (pins 8 and 9)		-	-	1	dB
$R_{8, 9}$	output resistance		-	100	-	Ω
$V_{8, 9}$	DC voltage		-	2.1	-	V
$I_{8, 9}$	allowed AC current of emitter output (peak value)	note 3	-	-	±1.5	mA
$I_{8, 9}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
V_o	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 9-8)		60	70	-	dB
$V_{16, 18}$	DC voltage (pins 16 and 18)		-	1.7	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM mode, input signal at pins 1-2		SC = 32.4 MHz; f_{mod} = 1 kHz, m = 0.54; $V_{i\,AM}$ = 10 mV rms				
V_o	AF output signal on pin 9 (RMS value)		400	500	600	mV
R_9	output resistance (pin 9)		-	100	-	Ω
I_o	maximum AC output current (peak value)	note 3	-	-	±1.5	mA
I_9	maximum DC output current		-	-	–2	mA
V_9	DC voltage		-	2.1	-	V
THD	total harmonic distortion	Fig.4	-	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	50	56	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
V_{14}	DC voltage (pin 14)		-	2	-	V
Audio frequency performance for FM operation in B/G standard ($V_5 = V_P$) unless otherwise specified.						
Measurements on AF outputs (pins 8 and 9)						
V_o	signals attenuation of AF signal switches					
	mute: AF2 on pin 8	V_5 = 0	70	-	-	dB
	AM mode: not required signal AF1 on pin 9 (from FM)	5.5 MHz on pin 18; V_5 = 0; V_i = 10 mV	70	-	-	dB
	FM mode: not required signal AF1 on pin 9 (from AM)	signal for L standard (pins 1-2); $V_5 = V_P$	70	-	-	dB
$dV_{8,9}$	DC level deviation (pins 8 and 9)	when switching to FM or AM sound or Mute	-	5	25	mV
S/N(W)	weighted signal-to-noise ratio on output pin 9	CCIR 468-3 de-emphasis 50 µs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	on output pin 8					
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R = 70 Hz V_R = 200 mV (p-p)	30	40	-	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at $R_{12\text{-}13}$ = 470 Ω (instead of LC circuit); input signal $V_{i\ (rms)}$ = 20 mV (pins 23-24). AGC voltage V_3 set to a value to achive $V_{o\ (rms)}$ = 20 mV (pins 12-13). After switching (V_5 = 0 V) measure attenuation. IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100% picture modulation.)
3. For larger current: R_L > 2.2 kΩ (pin 8 or 9 to GND) in order to increase the bias current of the output emitter follower.

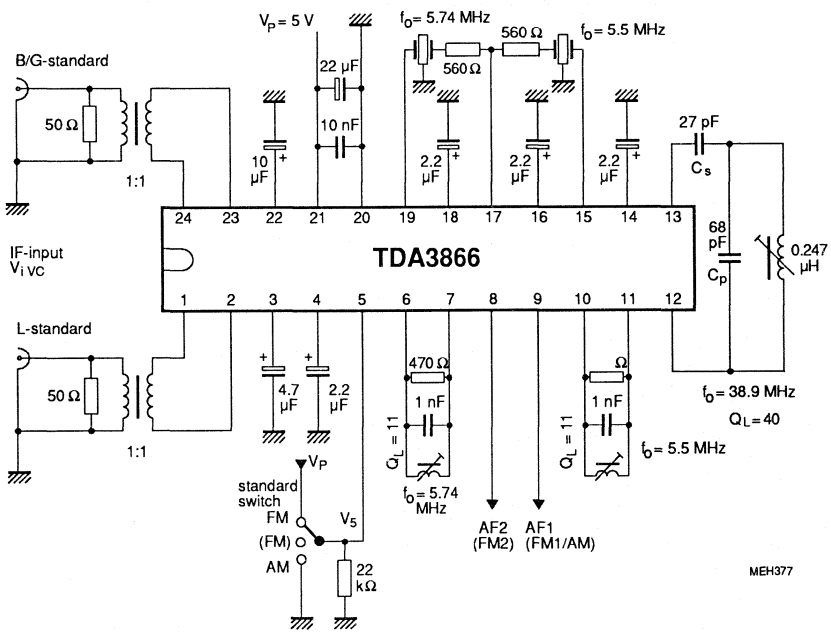


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used).

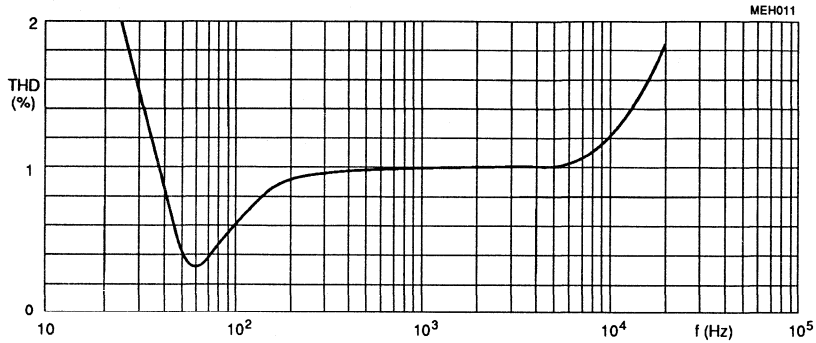
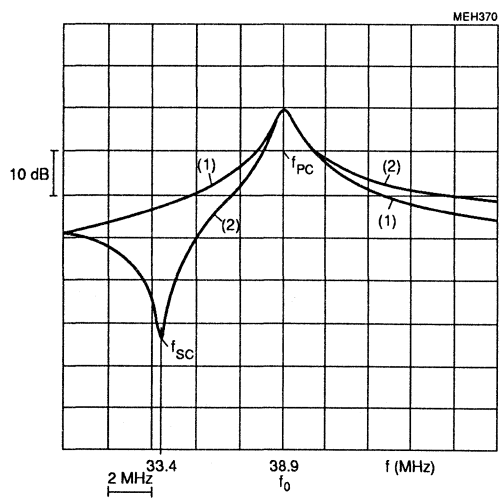


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard ($V_5 = 0$).



(1) simple resonace circuit (without C_S)
(2) resonance circuit with C_S = 27 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

APPLICATION INFORMATION

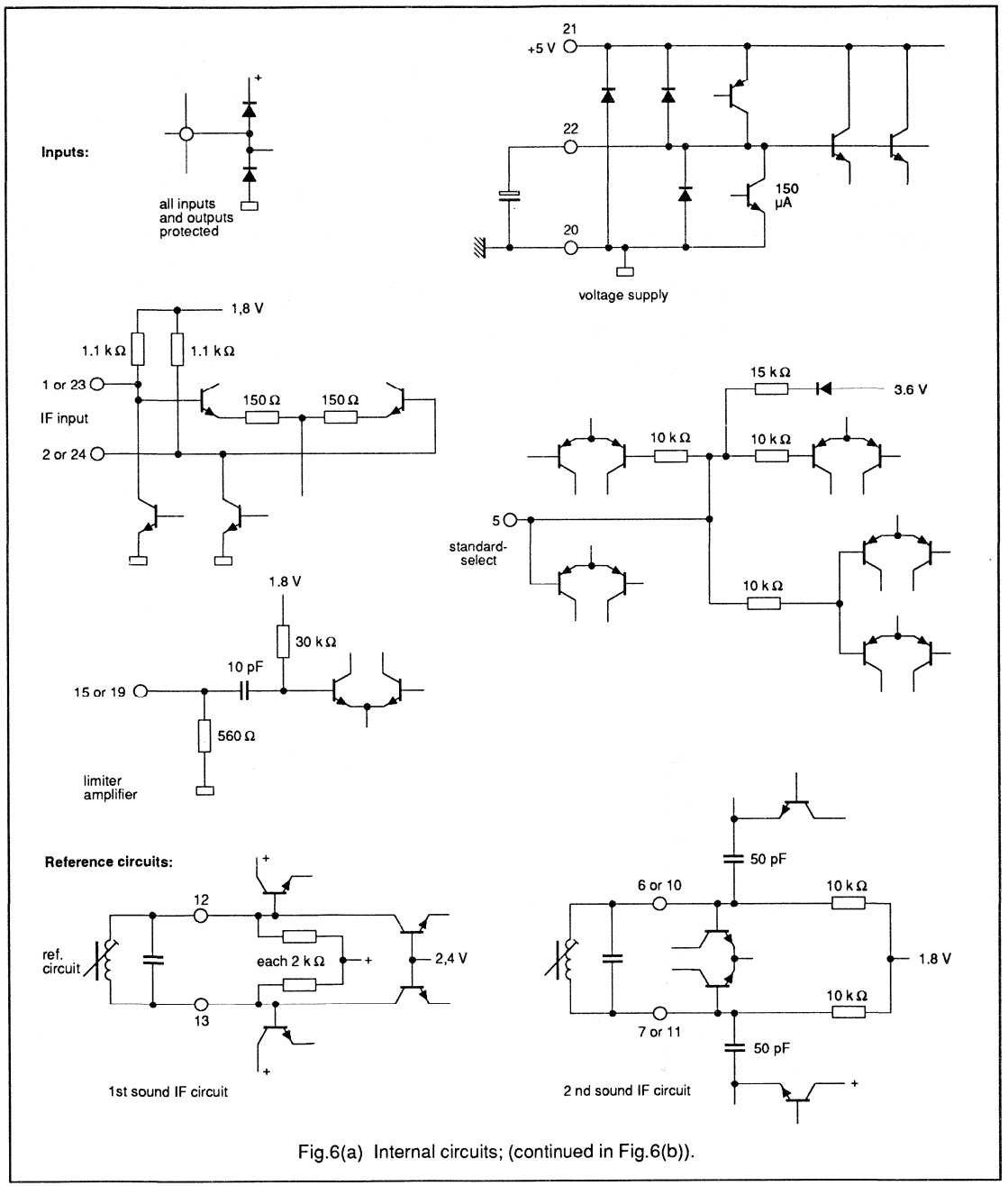


Fig.6(a) Internal circuits; (continued in Fig.6(b)).

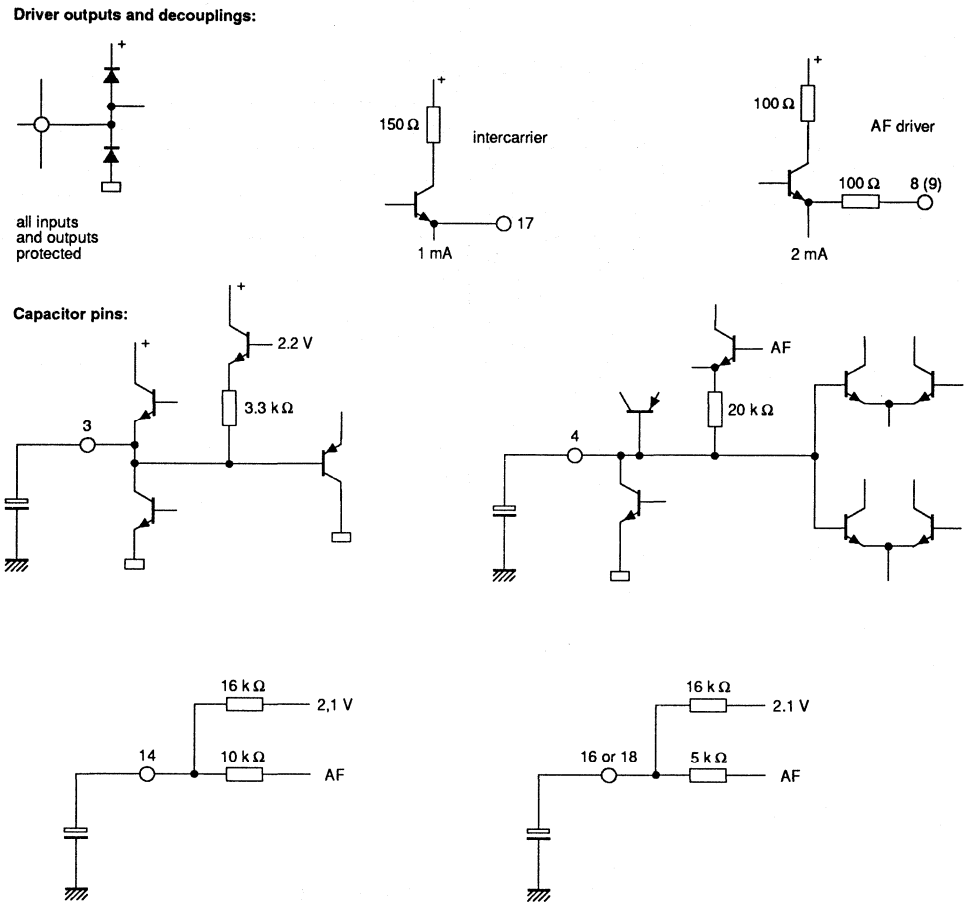


Fig.6(b) Internal circuits; (continued from Fig.6(a)).

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1992

TDA3867T

Quasi-split sound processor with two FM demodulators

FEATURES

- Quasi-split sound processor for all FM standards e. g. B/G
- Reduction of spurious video signals by tracking function and AFC for the vision carrier reference circuit; (indispensable for NICAM)
- AF2 signal automatically muted (at B/G) by the input signal level

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 24)	4.5	5	8.8	V
I_P	supply current (pin 24)	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
V_o	audio output signal (RMS value)	-	1	-	V
THD	total harmonic distortion	-	0.5	-	%
S/N (W)	weighted signal-to-noise ratio for FM	-	68	-	dB
	for FM with 6 kHz sinus vision modulation	-	56	-	dB

GENERAL DESCRIPTION

Symmetrical IF input and gain controlled wideband IF amplifier.

AGC generation due to peak sync Reference amplifier for the regeneration of the vision carrier.

Optimized limiting amplifier for AM suppression in the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3867T	28	mini-pack	plastic	SOT136A

Quasi-split sound processor with two FM demodulators

TDA3867T

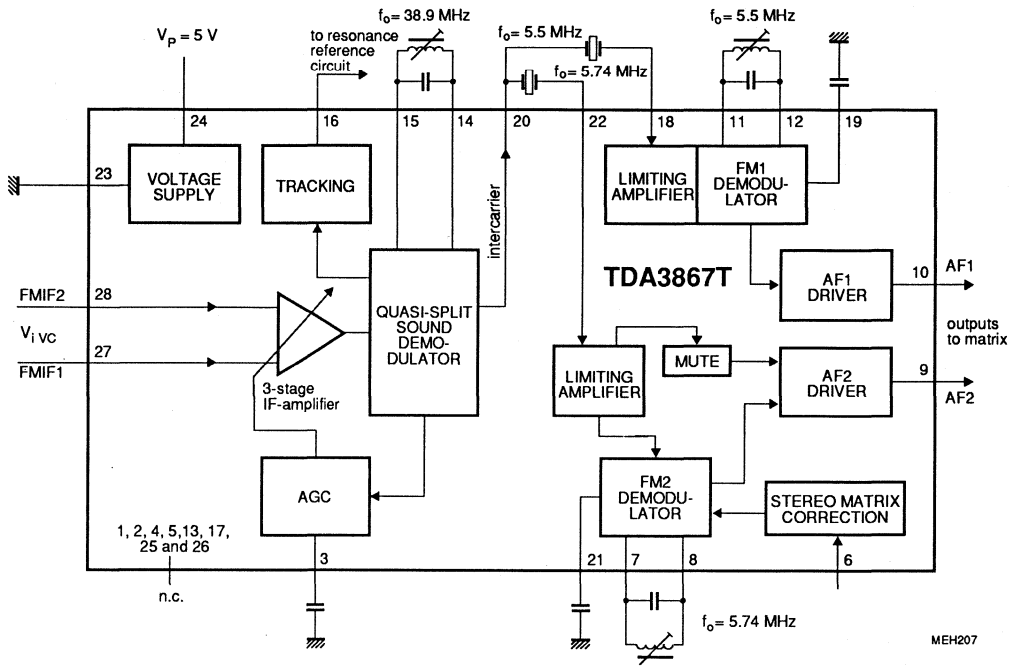


Fig.1 Block diagram.

Quasi-split sound processor with two FM demodulators

TDA3867T

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
C_{AGC}	3	charge capacitor for AGC
n.c.	4	not connected
n.c.	5	not connected
MATR	6	input for stereo matrix correction
FM2R1	7	reference circuit for FM2 (5.74 MHz)
FM2R2	8	reference circuit for FM2 (5,74 MHz)
AF2	9	AF2 output (AF out of 5.74 MHz)
AF1	10	AF1 output (AF out of 5.5 MHz)
FM1R1	11	reference circuit for FM1 (5.5 MHz)
FM1R2	12	reference circuit for FM1 (5.5 MHz)
n.c.	13	not connected
VC-R1	14	reference circuit for the vision carrier (38.9 MHz)
VC-R2	15	reference circuit for the vision carrier (38.9 MHz)
TRACK	16	DC output level for tracking
n.c.	17	not connected
FM1i	18	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	19	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	20	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	21	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	22	intercarrier input for FM2 (5.74 MHz)
GND	23	ground (0 V)
V_P	24	+5 to +8 V supply voltage
n.c.	25	not connected
n.c.	26	not connected
FMIF1	27	IF difference input 1 (B/G standard, 38.9 MHz)
FMIF2	28	IF difference input 2 (B/G standard, 38.9 MHz)

PIN CONFIGURATION

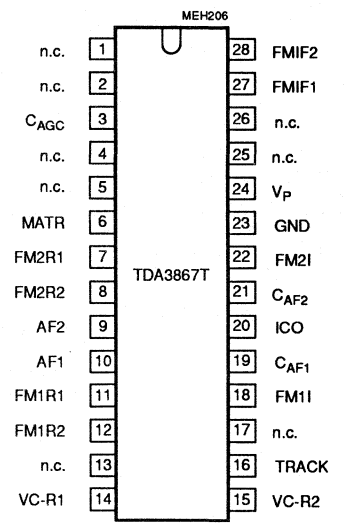


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is suitable for all FM standards (e. g. B/G).
The AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 22 , AF2 output is muted. The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.
With 1 mV on pin 22, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals at pins 27 and 28 generate noise on pin 22, which is present in the intercarrier signal and passes through the 5.74 MHz filter. Noise on pin 22 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

The series capacitor C_S in the 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to

$$C_S = C_P (f_{VC} / f_{SC})^2 - C_P.$$

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier. The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.
Measurements at the demodulators: For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_m = 1$ kHz; with a deviation of ± 27 kHz the S/N ratio is deteriorated by 5.3 dB.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltages (pin 24)	-	8.8	V
V_n	input and output voltage (pins 9, 10, 18, 20, 22, 27 and 28)	0	V_P	V
P_{tot}	total power dissipation	0	635	mW
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* all pins except 27 and 28	±500	-	V
	pins 27 and 28	+400 –500	- -	V V

CHARACTERISTICS

V_{P1} = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz.
Vision carrier (VC) modulated with different video signals , modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = ±50 kHz unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 24)		4.5	5	8.8	V
I_P	supply current (pin 24)	V_P = 5 V	48	60	72	mA
IF amplifier (pins 27-28)						
R_I	input resistance		1.75	2.2	2.65	kΩ
C_I	input capacitance		1.0	1.5	2.2	pF
V_I	DC potential, voltage (pins 27 and 28)		-	1.75	-	V
$V_{i\ IF}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity (RMS value)	–3 dB intercarrier signal reduction on pin 20	-	70	100	μV
ΔG_v	IF gain control range		60	63	-	dB
B	IF bandwidth	–3 dB	50	70	-	MHz
V_3	voltage range for gain control (pin 3)	$G_{min} - G_{max}$	1.7	-	2.6	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resonance amplifier (pins 14-15)						
V_o	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
R_{14-15}	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 4	-	0.247	-	µH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{14, 15}$	DC voltage (pins 14 and 15)		-	V_P–1	-	V
Intercarrier mixer output (pin 20)						
V_o	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{20}	residual video AM on intercarrier	note 1	-	3	10	%
V_{VC}	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{20}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 20)		-	-	±0.7	mA
I_{20}	allowable DC output current		-	-	–2	mA
V_{20}	DC voltage		-	1.75	-	V
Limiting amplifiers (pins 18 and 22)						
V_i	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	µV
	maximum input signal (RMS value)		200	-	-	mV
$R_{18, 22}$	input resistance		-	560	-	Ω
$V_{18, 22}$	DC voltage		-	0	-	V
V_i	level detector threshold for no muting (RMS value, pin 22)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tracking automatic frequency control (AFC) of the vision carrier reference circuit.						
V_o	tracking output voltage range (pin 16)	note 5	V_{P1}–3.3	-	V_{P1}–1	V
F_{TR}	tracking reducing factor for					
	black picture		-	9	-	
	white test picture		-	4	-	
	50 % grey picture		-	6	-	
S	AFC steepness (open loop) for					
	black picture		-	–8	-	mV/kHz
	white test picture		-	–3	-	mV/kHz
	50 % grey picture		-	–5.5	-	mV/kHz
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm 50$ kHz) on pins 18 and 22 without ceramic filters, $R_S = 50\ \Omega$. De-emphasis of 50 µs and $V_5 = V_P$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 7-8 and 11-12.						
V_{IC}	intercarrier signals (RMS values, pins 7-8 and 11-12)		-	100	-	mV
V_{DC}	DC voltage (pins 7, 8,11 and 12)		-	1.8	-	V
V_o	AF output signals (RMS values, pins 9 and 10)		0.75	0.95	1.20	V
ΔV_o	difference of AF signals between channels (pins 9 and 10)	pin 6 open-circuit; note 2	-	-	1	dB
$R_{9, 10}$	output resistance		-	100	-	Ω
$V_{9, 10}$	DC voltage		-	2.1	-	V
$I_{9, 10}$	allowed AC current of emitter output (peak value)	note 3	-	-	±1.5	mA
	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
V_o	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 9-10)		60	70	-	dB
V_6	adjusting voltage for AF2 signal (pin 6)	note 4	0	-	5	V
ΔG_{AF2}	minimum gain range due to V_6	due to V_6	–1.5	-	1.0	dB
	typical gain range	due to V_6	–2.5	-	1.5	dB
$V_{19, 21}$	DC voltage (pins 19 and 21)		-	1.7	-	V

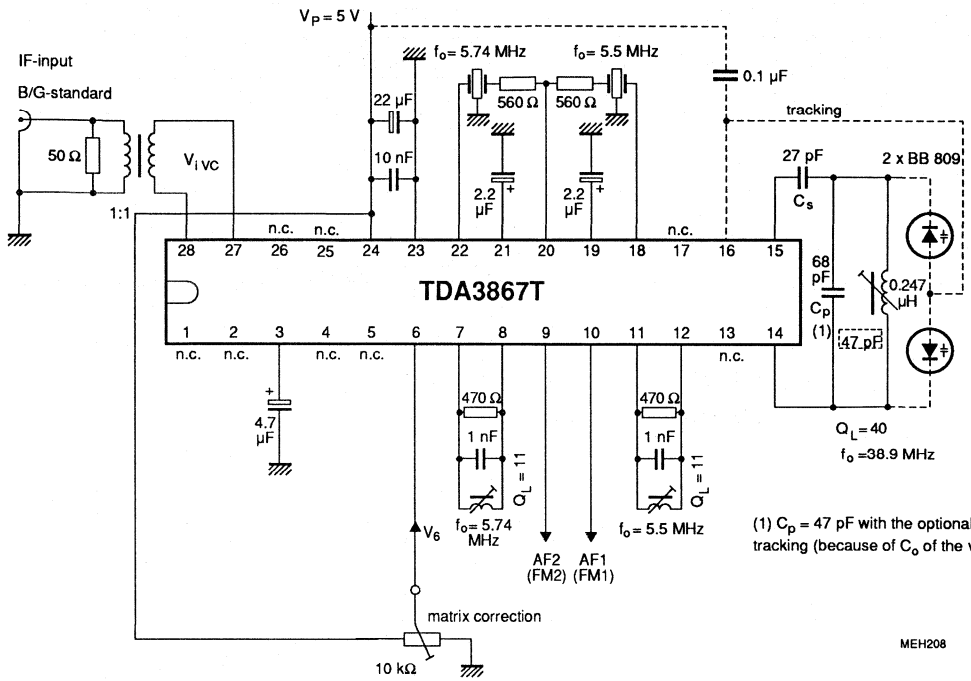
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio frequency performance in B/G standard unless otherwise specified.						
Measurements on AF outputs (pins 9 and 10)						
V_o	AF signal attenuation	V_i = 400 µV;				
	mute: AF2 on pin 9	5.74 MHz on pin 22	70	-	-	dB
dV_9	DC level deviation	after mute switching	-	5	25	mV
S/N(W)	weighted signal-to-noise ratio on output pin 10	CCIR 468-3 de-emphasis 50 µs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	on output pin 9					
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R = 70 Hz V_R = 200 mV (p-p)	30	40	-	dB

Notes to the characteristics

1. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100 % picture modulation.)
2. AF2 signal can be adjusted by V_6
3. For larger current: R_L > 2.2 kΩ (pin 9 or 10 to GND) in order to increase the bias current of the output emitter follower.
4. If not used, pin 6 should not be connected.
5. Automatic frequency control (AFC) of the vision carrier reference circuit (pins 14 and 15) for reducing spurious video signals in the stereo/dual sound modes. The factor of reducing F_{TR} at a deviation Δf_{VC} specifies the ratio of spurious signals with/without tracking function.

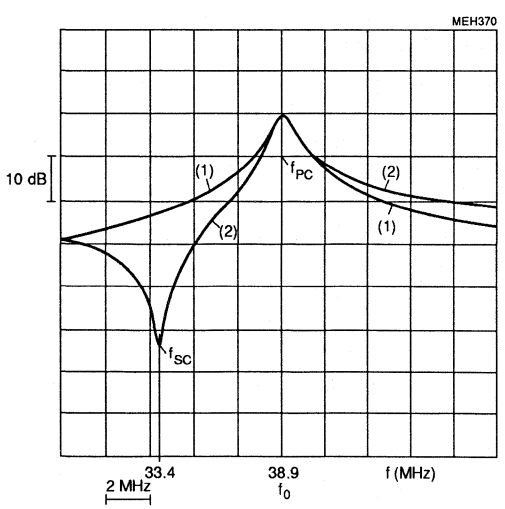
Quasi-split sound processor with two FM demodulators

TDA3867T



(1) C_p = 47 pF with the optional use of tracking (because of C_o of the varicaps).

Fig.3 Test and application circuit (for application SAW-filters must be used).



(1) simple resonance circuit (without C_S)
(2) resonance circuit with C_S = 27 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.4 Frequency response of the 38.9 MHz reference circuit.

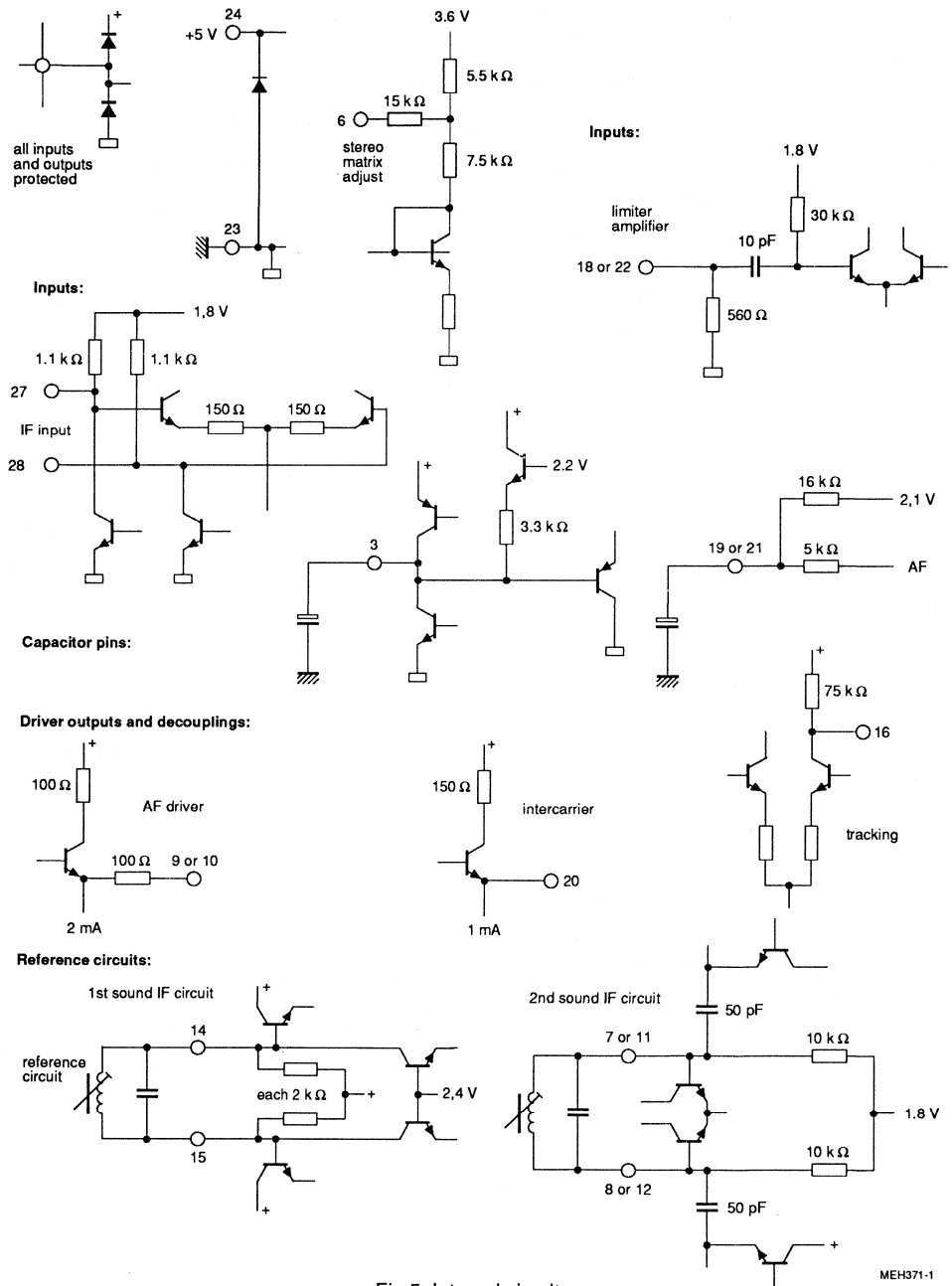


Fig.5 Internal circuits.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	January 1992

TDA3868T

Quasi-split sound processor for all standards

FEATURES

- Quasi-split sound processor for all standards e. g. B/G (FM sound) and L (AM sound)
- Reduction of spurious video signals by tracking function and AFC for the vision carrier reference circuit; (indispensable for NICAM)
- AF2 signal automatically muted (at B/G) by input signal level
- AM signal processing for L standard and audio switching over
- Stereo-matrix correction
- AM output level typically 500 mV at m = 0.54 (+2.5 dB in comparison to TDA3858)

GENERAL DESCRIPTION

Separate symmetrical IF inputs for FM and AM sound.

Gain controlled wideband IF amplifier and input select switch.

AGC generation due to peak-sync for FM or mean signal level for AM.

Reference amplifier to regenerate the vision carrier.

Limiting amplifier optimized for AM suppression of the regenerated vision carrier signal and 90° phase shifter.

Intercarrier mixer for FM sound, output with low-pass filter.

Separate signal processing for 5.5 and 5.74 MHz intercarriers.

Wide supply voltage range, only 300 mW power dissipation at 5 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 24)	4.5	5	8.8	V
Data at V_P = 5 V					
I_P	supply current (pin 24)	-	60	72	mA
$V_{i\ IF}$	IF input sensitivity (–3 dB)	-	70	100	μV
V_o	audio output signal for FM standard B/G (RMS value)	-	1	-	V
	audio output signal for AM standard L (RMS value)	-	0.5	-	V
THD	total harmonic distortion for FM	-	0.5	-	%
	for AM	-	1	-	%
S/N (W)	weighted signal-to-noise ratio for FM	-	68	-	dB
	for FM with 6 kHz sinus vision modulation	-	56	-	dB
	for AM	-	56	-	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3868T	28	mini-pack	plastic	SOT136A

Quasi-split sound processor for all standards

TDA3868T

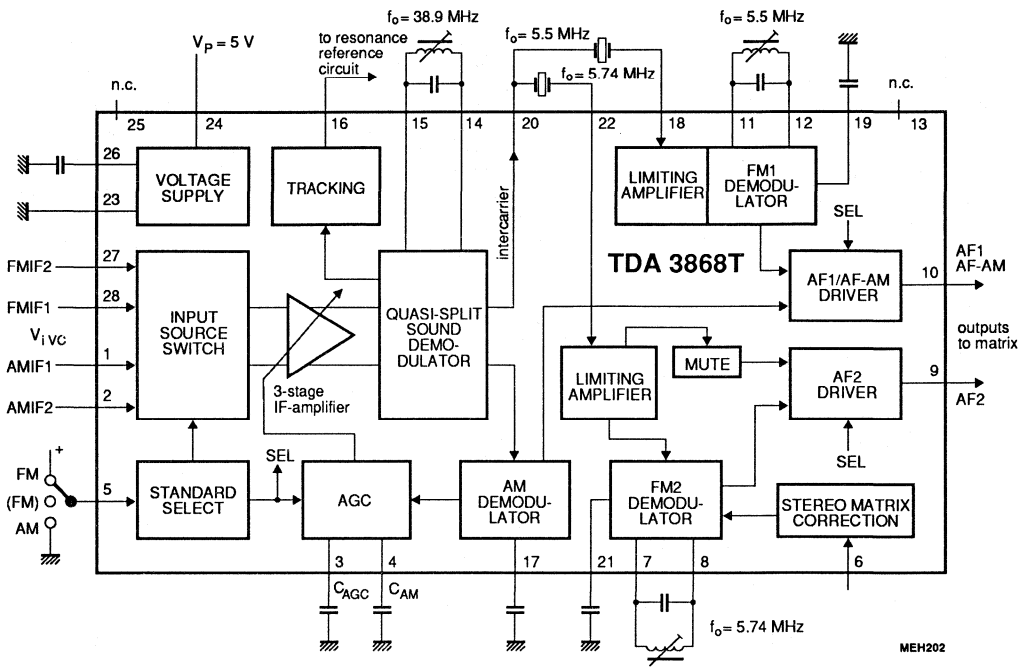


Fig.1 Block diagram (B/G and L standards).

Quasi-split sound processor for all standards

TDA3868T

PINNING

SYMBOL	PIN	DESCRIPTION
AMIF1	1	AM IF difference input 1 for L standard (32.4 MHz)
AMIF2	2	AM IF difference input 2 for L standard (32.4 MHz)
C_{AGC}	3	charge capacitor for AGC (FM and AM)
C_{AM}	4	charge capacitor for AM AGC
MODE	5	3-state input for standard select
MATR	6	input for stereo matrix correction
FM2R1	7	reference circuit for FM2 (5.74 MHz)
FM2R2	8	reference circuit for FM2 (5,74 MHz)
AF2	9	AF2 output (AF out of 5.74 MHz)
AF1	10	AF1 output (AF out of 5.5 MHz or AM)
FM1R1	11	reference circuit for FM1 (5.5 MHz)
FM1R2	12	reference circuit for FM1 (5.5 MHz)
n.c.	13	not connected
VC-R1	14	reference circuit for the vision carrier (38.9 MHz)
VC-R2	15	reference circuit for the vision carrier (38.9 MHz)
TRACK	16	DC output level for tracking
C_{AFAM}	17	DC-decoupling capacitor for AM demodulator (AF AM)
FM1I	18	intercarrier input for FM1 (5.5 MHz)
C_{AF1}	19	DC-decoupling capacitor for FM1 demodulator (AF1)
ICO	20	intercarrier output signal (5.5/5.74 MHz)
C_{AF2}	21	DC-decoupling capacitor for FM2 demodulator (AF2)
FM2I	22	intercarrier input for FM2 (5.74 MHz)
GND	23	ground (0 V)
V_P	24	+5 to +8 V supply voltage
n.c.	25	not connected
C_{ref}	26	charge capacitor for reference voltage
FMIF1	27	IF difference input 1 (B/G standard, 38.9 MHz)
FMIF2	28	IF difference input 2 (B/G standard, 38.9 MHz)

PIN CONFIGURATION

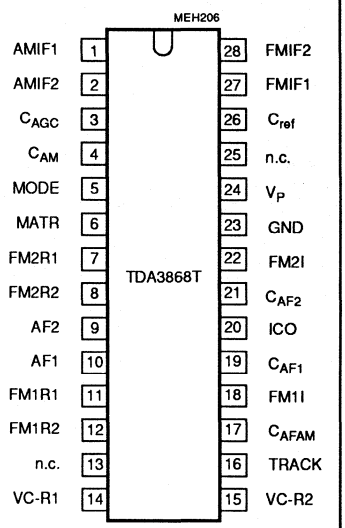


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The quasi-split sound processor is for all standards. Dependent on the voltage on pin 5 either FM mode (B/G) or AM mode (L) is selected.

B/G standard (FM mode):
Pins 27 and 28 are active, AGC detector uses peak sync level. Sound carrier SC1 (5.5 MHz) provides AF1, sound carrier SC2 (5.74 MHz) provides AF2. With no sound carrier SC2 on pin 22 , AF2 output is muted (in mid-position of the standard select switch FM mode without muting of AF2 is selected). The mute circuit prevents false signal recognition in the stereo decoder at high IF signal levels when no second sound carrier exists (mono) and an AF signal is present in the identification signal frequency range.
With 1 mV on pin 22, under measurement conditions, AF2 is switched on (see limiting amplifier). Weak input signals on pins 27 and 28 generate noise on pin 22, which is present in the intercarrier signal and passes through the 5,74 MHz filter. Noise on pin 22 inhibits muting. No misinterpretation due to white noise occurs in the stereo decoder; when non-correlated noise masks the identification signal frequencies, which may be present in sustained tone signals. The stereo decoder remains switched to mono.

The series capacitor C_s in 38.9 MHz resonant circuit provides a notch at the sound carrier frequency in order to provide more attenuation for the sound carrier in the vision carrier reference channel. The ratio of parallel/series capacitor depends on the ratio of VC/SC frequency and has to be adapted to other TV transmission standards if necessary, according to
$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$.

The result is an improved "intercarrier buzz" (up to 10 dB improvement in sound channel 2 with 250 kHz video modulation for B/G stereo) or suppression of 350 kHz video modulated beat frequency in the digitally-modulated NICAM subcarrier. The picture carrier for quadrature demodulation in the intercarrier mixer is not exactly 90 degrees due to the shift variation in the integrated phase shift network. The tuning of the LC reference circuit to provide optimal video suppression at the intercarrier output is not the same as that to provide optimal intercarrier buzz suppression. In order to optimize the AF signal performance, a fine tuning for the optimal S/N at the sound channel 2 (from 5.74 MHz) may be performed with a 250 kHz square wave video modulation.
Measurements at the demodulators:
For all signal-to-noise measurements the generator must meet the following specifications; phase modulation errors < 0.5 degree for B/W-jumps intercarrier signal-to-noise ratio as measured with "TV-demodulator AMF2" (weighted S/N) must be > 60 dB at 6 kHz sine wave modulation of the B/W-signal. Signal-to-noise ratios are measured with $\Delta f = \pm 50$ kHz deviation and $f_m = 1$ kHz; with a deviation of ±27 kHz the S/N ratio is deteriorated by 5.3 dB.

L standard (AM mode):
Pins 1 and 2 are active, AGC detector uses mean signal level.The audio signal from the AM demodulator is output on AF1 with AF2 output muted.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltages (pin 24)	-	8.8	V
V_I	voltage (pins 1, 2, 5, 9, 10, 18, 20, 22, 27 and 28)	0	V_P	V
P_{tot}	total power dissipation	0	635	mW
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* all pins except 1, 2, 27 and 28	±500	-	V
	pins 1, 2, 27 and 28	+400	-	V
	pins 1, 2, 27 and 28	–500	-	V

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C, measurements taken in Fig.3 with f_{VC} = 38.9 MHz, f_{SC1} = 33.4 MHz and f_{SC2} = 33.158 MHz.
Vision carrier (VC) modulated with different video signals, modulation depth 100 % (proportional to 10 % residual carrier).
Vision carrier amplitude (RMS value) $V_{i\ VC}$ = 10 mV; vision to sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB. Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation Δf = ±50 kHz unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 24)		4.5	5	8.8	V
I_P	supply current (pin 24)	V_P = 5 V	48	60	72	mA
IF input not activated (pins 1-2 or 27-28)						
R_I	input resistance		-	-	100	Ω
V_I	DC input voltage (pins 1-2 or 31-32)	LOW internal set	-	-	0.1	V
$\alpha_{1,2\text{-}27.28}$	crosstalk attenuation of IF input switch	note 1	50	56	-	dB

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF source control (pin 5)						
V_5	input voltage in order to obtain standards					
	B/G (FM) with automatic muting	pin 5 connected	2.8	-	V_{P1}	V
		pin 5 open-circuit	-	2.8	-	V
	B/G (FM) without muting	pin 5 connected	1.3	-	2.3	V
		or alternative measure: 22 kΩ to GND				
	L (AM sound)	pin 5 connected	0	-	0.8	V
I_5	input current	$V_5 = V_P$	-	-	100	μA
		$V_5 = 0$	-	-	–300	μA
IF amplifier (pins 27-28 or 1-2)						
R_I	input resistance		2.75	2.2	2.65	kΩ
C_I	input capacitance		1.0	1.5	2.2	pF
V_I	DC potential, voltage (pins 1, 2, 27, 28)		-	1.75	-	V
$V_{i\ IF}$	maximum input signal (RMS value)	V_o = +1 dB	70	100	-	mV
	input signal sensivity B/G standard (RMS value, pins 27-28)	–3 dB intercarrier signal reduction on pin 20	-	70	100	μV
	input signal sensivity L standard (RMS value, pins 1-2)	–3 dB intercarrier signal reduction on pin 10	-	70	100	μV
ΔG_v	IF gain control range		60	63	-	dB
B	IF bandwidth	–3 dB	50	70	-	MHz
V_3	voltage range for gain control (pin 3)	$G_{min} - G_{max}$	1.7	-	2.6	V
Resonance amplifier (pins 14-15)						
V_o	vision carrier amplitude (peak-to-peak value)	f_o = 38.9 MHz	-	270	-	mV
$R_{14\text{-}15}$	operating resistance		-	4	-	kΩ
L	inductance	Fig.3 and 5	-	0.247	-	μH
C	capacitance	C_S = 27 pF	-	68	-	pF
Q_L	Q-factor of resonant circuit	Q_o = 90	-	40	-	
$V_{14,\ 15}$	DC voltage (pins 14 and 15)		-	V_P–1	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Intercarrier mixer output (pin 20)						
V_o	output signal for 5.5 MHz (RMS value)		71	95	125	mV
	output signal for 5.74 MHz (RMS value)		32	43	56	mV
B	IF bandwidth	–1 dB	-	8.5	-	MHz
		–3 dB	-	10	-	MHz
V_{VID}/V_{20}	residual video AM on intercarrier	note 2	-	3	10	%
V_{VC}	residual vision carrier (RMS value)	1st/2nd harmonic; (38.9/77.8 MHz)	-	0.5	1	mV
R_{20}	output resistance (emitter follower)	1 mA emitter current	-	30	-	Ω
I_o	allowable AC output current (pin 20)		-	-	±0.7	mA
I_{20}	allowable DC output current		-	-	–2	mA
V_{20}	DC voltage		-	1.75	-	V
Limiting amplifiers (pins 18 and 22)						
V_i	minimum input signal (RMS value)	–3 dB AF signal	-	300	450	μV
	maximum input signal (RMS value)		200	-	-	mV
$R_{18, 22}$	input resistance		-	560	-	Ω
$V_{18, 22}$	DC voltage		-	0	-	V
V_i	level detector threshold for no muting (RMS value, pin 22)	only 5.74 MHz channel	-	1	-	mV
ΔV_i	hysteresis of level detector		-	5	-	dB
Tracking automatic frequency control (AFC) of the vision carrier reference circuit.						
V_o	tracking output voltage range (pin 16)	note 3	V_{P1}–3.3	-	V_{P1}–1	V
F_{TR}	tracking reducing factor for					
	black picture		-	9	-	
	white test picture		-	4	-	
	50 % grey picture		-	6	-	
S	AFC steepness (open loop) for					
	black picture		-	–8	-	mV/kHz
	white test picture		-	–3	-	mV/kHz
	50 % grey picture		-	–5.5	-	mV/kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM1 and FM2 demodulators Measurements with FM IF input signals of 5.5 MHz and 5.74 MHz with $V_{i\ IF\ (rms)}$ = 10 mV (f_{mod} = 1 kHz, deviation $\Delta f = \pm$ 50 kHz) at pins 18 and 22 without ceramic filters, R_S = 50 Ω. De-emphasis 50 µs and $V_5 = V_P$ (B/G standard). Q_L-factor = 11 for resonant circuits at pins 7-8 and 11-12.						
V_{IC}	intercarrier signals (RMS values, pins 7-8 and 11-12)		-	100	-	mV
V_{DC}	DC voltage (pins 7, 8, 11 and 12)		-	1.8	-	V
V_o	AF output signals (RMS values, pins 9 and 10)		0.75	0.95	1.20	V
ΔV_o	difference of AF signals between channels (pins 9 and 10)	pin 6 open-circuit; note 4	-	-	1	dB
$R_{9, 10}$	output resistance		-	100	-	Ω
$V_{9, 10}$	DC voltage		-	2.1	-	V
$I_{9, 10}$	allowed AC current of emitter output (peak value)	note 5	-	-	±1.5	mA
$I_{9, 10}$	maximum allowed DC output current		-	-	–2	mA
THD	total harmonic distortion		-	0.5	1.0	%
V_o	AF output signal (RMS value)	THD = 1.5 %	1.25	-	-	V
α_{AM}	AM suppression	1 kHz, m = 0.3	48	54	-	dB
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	64	68	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
α_{CR}	crosstalk attenuation (pins 9-10)		60	70	-	dB
V_6	adjusting voltage for AF2 signal (pin 6)	note 6	0	-	5	V
ΔG_{AF2}	minimum gain range	due to V_6	–1.5	-	1.0	dB
	typical gain range	due to V_6	–2.5	-	1.5	dB
$V_{19, 21}$	DC voltage (pins 19 and 21)		-	1.7	-	V
AM mode, input signal at pins 1-2		SC = 32.4 MHz; f_{mod} = 1 kHz, m = 0.54; $V_{i\ AM}$ = 10 mV rms				
V_o	AF output signal on pin 10 (RMS value)		400	500	600	mV
R_{10}	output resistance (pin 10)		-	100	-	Ω
I_o	maximum AC output current (peak value)	note 5	-	-	±1.5	mA
I_{10}	maximum DC output current		-	-	–2	mA
V_{10}	DC voltage		-	2.1	-	V
THD	total harmonic distortion	Fig.4	-	1	2	%
S/N(W)	weighted signal-to-noise ratio	CCIR 468-3	50	56	-	dB
B	AF bandwidth	–3 dB	0.02	-	100	kHz
V_{17}	DC voltage (pin 17)		-	2	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio frequency performance for FM operation in B/G standard ($V_5 = V_P$) unless otherwise specified.						
Measurements on AF outputs (pins 9 and 10)						
V_o	signal attenuation of AF signal switches					
	mute: AF2 on pin 9	V_5 = 0	70	-	-	dB
	AM mode: not required signal AF1 on pin 10 (from FM)	5.5 MHz on pin 18; V_5 = 0; V_i = 10 mV	70	-	-	dB
	FM mode: not required signal AF1 on pin 10 (from AM)	signal for L standard (pins 1-2); $V_5 = V_P$	70	-	-	dB
$dV_{9,10}$	DC level deviation (pins 9 and 10)	when switching to FM or AM sound or Mute	-	5	25	mV
S/N(W)	weighted signal-to-noise ratio on output pin 10	CCIR 468-3 de-emphasis 50 µs				
	black picture	f_i = 5.5 MHz	59	63	-	dB
	2T/20T pulses with white bar	f_i = 5.5 MHz	57	61	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.5 MHz	52	56	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.5 MHz	50	56	-	dB
	on output pin 9					
	black picture	f_i = 5.742 MHz	57	61	-	dB
	2T/20T pulses with white bar	f_i = 5.742 MHz	55	59	-	dB
	6 kHz sine wave, B/W-modulated	f_i = 5.742 MHz	50	54	-	dB
	250 kHz square wave B/W-modulated	f_i = 5.742 MHz	50	56	-	dB
RR	ripple rejection	all standards; f_R = 70 Hz V_R = 200 mV (p-p)	30	40	-	dB

Notes to the characteristics

1. Crosstalk attenuation of IF input switch, measured at $R_{14\text{-}15}$ = 470 Ω (instead of LC circuit); input signal V_i = 20 mV rms (pins 27-28). AGC voltage V_3 set to a value to achive V_o = 20 mV rms (pins 14-15). After switching (V_5 = 0 V) measure attenuation. IF coupling with OFWG3203 and OFWL9350 (Siemens).
2. Spurious intercarrier AM: m = (A–B)/A (wherein A = signal at sync; B = signal with 100 % picture modulation.)
3. Automatic frequency control (AFC) of the vision carrier reference circuit (pins 14 and 15) for reducing spurious video signals in the stereo/dual sound modes. The factor of reducing F_{TR} at a deviation Δf_{VC} specifies the ratio of spurious signals with/without tracking function.
4. AF2 signal can be adjusted by V_6
5. For larger current: R_L > 2.2 kΩ (pin 9 or 10 to GND) in order to increase the bias current of the output emitter follower.
6. If not used, pin 6 should not be connected.

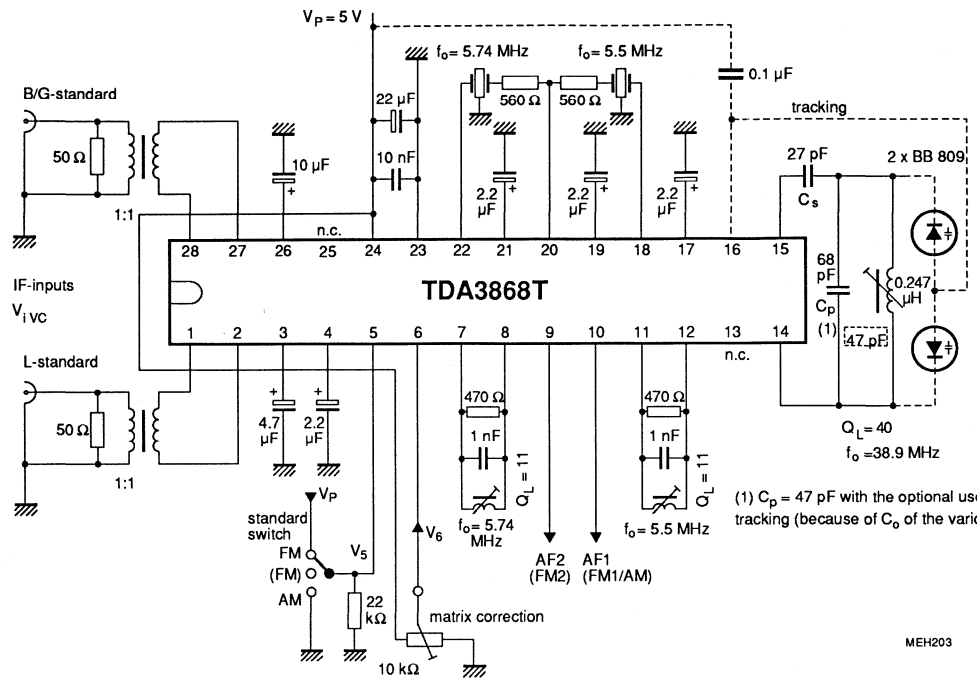


Fig.3 Test and application circuit for standards B/G and L (for application SAW-filters must be used).

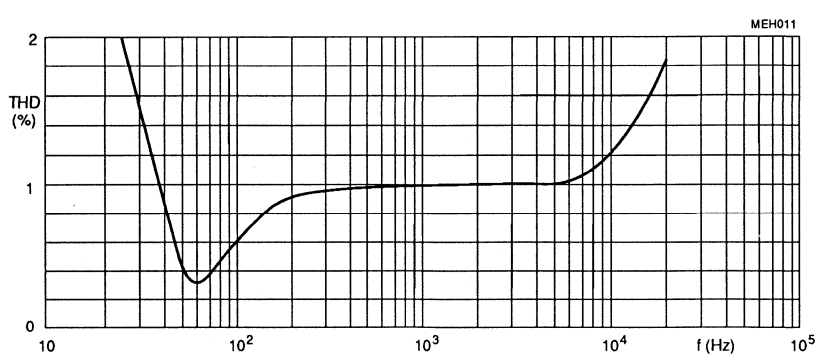
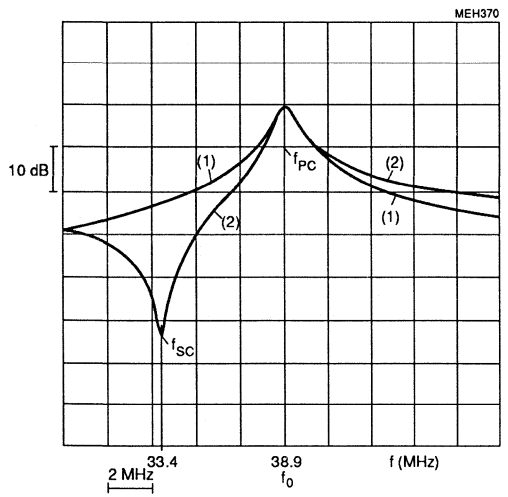


Fig.4 Total harmonic distortion (THD) as a function of audio frequency at AM standard (V_5 = 0).

APPLICATION INFORMATION



(1) simple resonance circuit (without C_S)
(2) resonance circuit with C_S = 27 pF

$C_S = C_P (f_{VC}/f_{SC})^2 - C_P$
C_S = 27 pF (Fig.3)

Fig.5 Frequency response of the 38.9 MHz reference circuit.

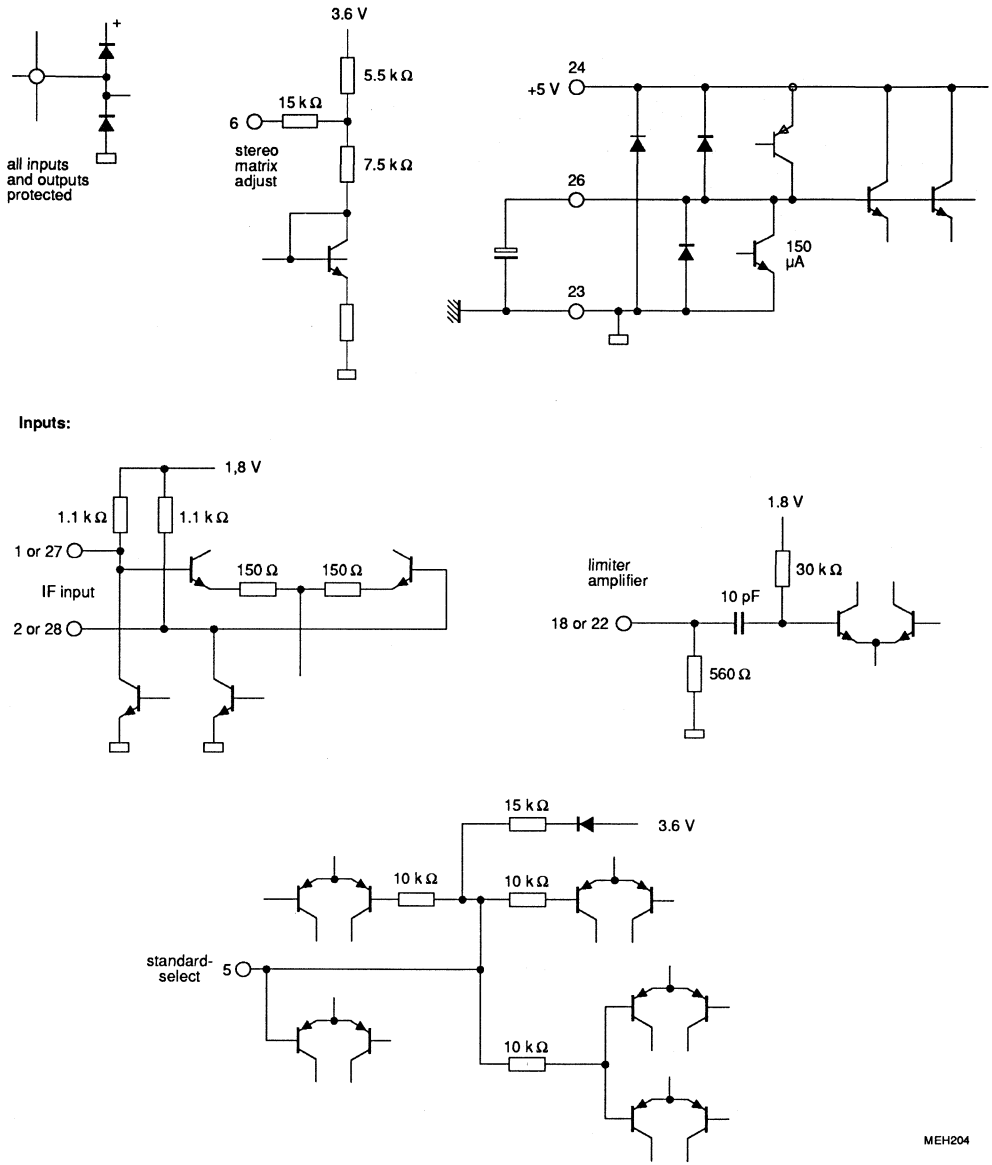


Fig.6(a) Internal circuits; (continued in Fig.6(b)).

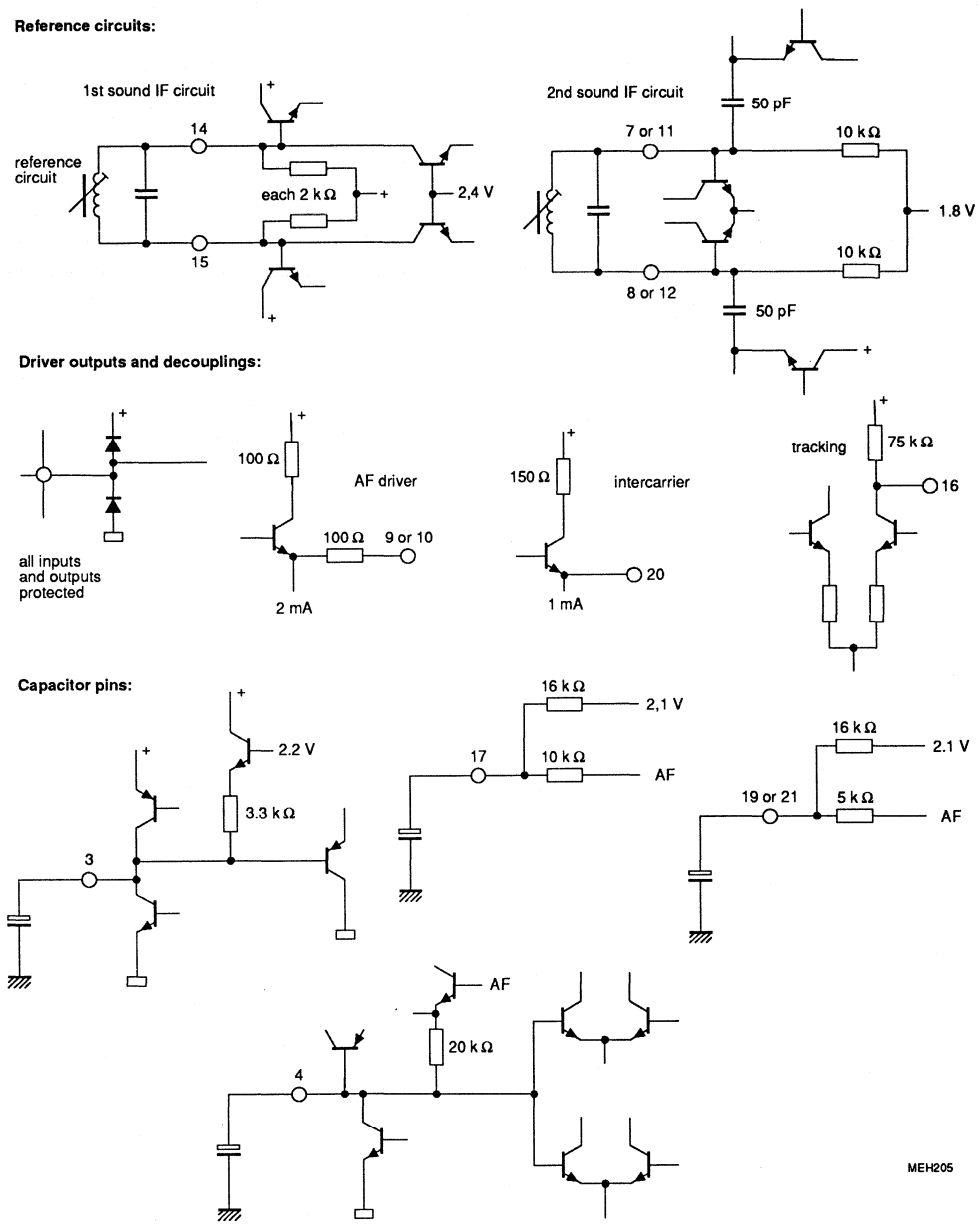


Fig.6(b) Internal circuits; (continued from Fig.6(a)).

VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301 is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame-transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 13		$V_{13\text{-}16}$	4.5	5.0	5.5	V
pin 1		$V_{1\text{-}16}$	11.0	11.25	11.5	V
Supply current	$V_{13\text{-}16}$ = 5 V	I_{13}	–	14	–	mA
Operating current	$V_{1\text{-}16}$ = 11.25 V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+150	°C
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

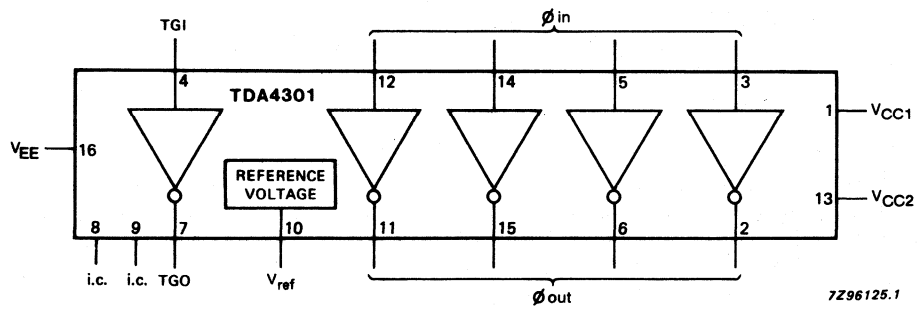


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 13		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 11 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	–20	+70	°C
Storage temperature range		T_{stg}	–25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 10)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 13)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

AC CHARACTERISTICS

$V_{CC1} = V_{1-16} = 11.25$ V; $V_{CC2} = V_{13-16} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 12 and 14)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_{\phi TH}$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 11 and 15)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

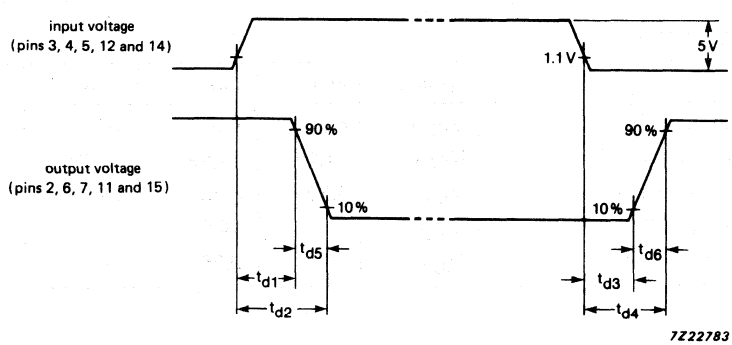


Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load only one switching may be done at a time.

APPLICATION INFORMATION

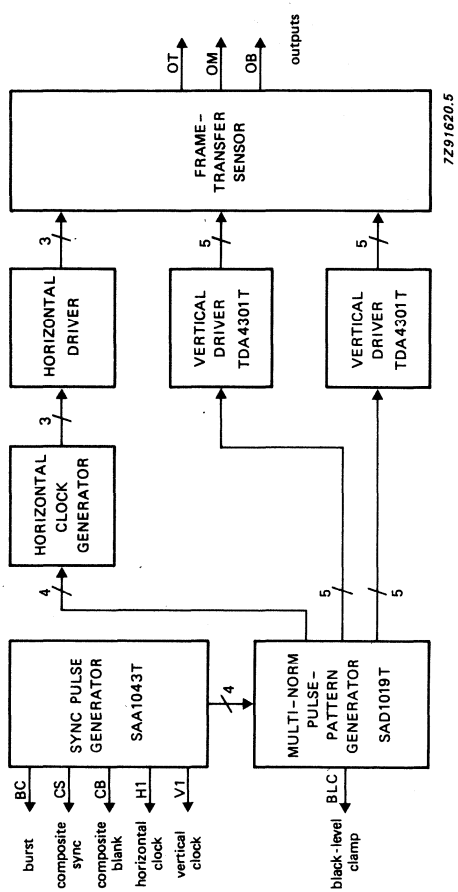


Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301T is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 11		V_{11-14}	4.5	5.0	5.5	V
pin 1		V_{1-14}	11.0	11.25	11.5	V
Supply current	V_{11-14} = 5 V	I_{11}	–	14	–	mA
Operating current	V_{1-14} = 11.25 V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+150	°C
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO14; SOT108A).

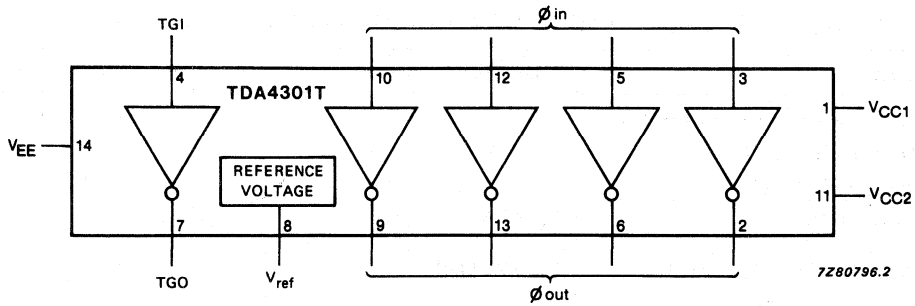


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 11		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 9 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 8)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 11)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

AC CHARACTERISTICS

$V_{CC1} = V_{1-14} = 11.25$ V; $V_{CC2} = V_{11-14} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 10 and 12)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_\phi TH$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 9 and 13)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p-p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

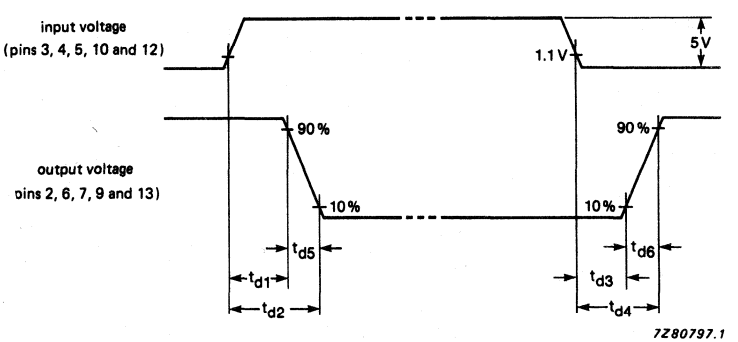


Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load switching only one may be done at a time.

APPLICATION INFORMATION

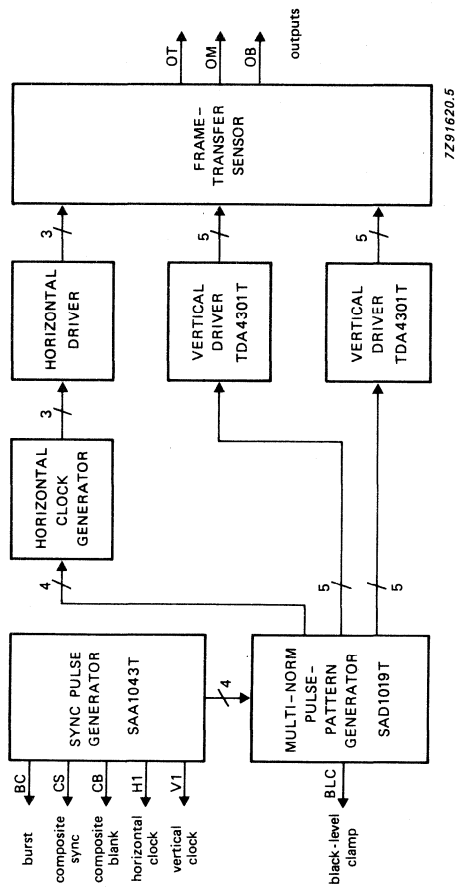


Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

MASTER GAIN

GENERAL DESCRIPTION

The TDA4306 is an integrated circuit which controls the amplification of the four output signals (White, Yellow, Green and Cyan) from the frame transfer sensors (NXA1021 to NXA1041). The matching of the four channels is excellent over the whole control and temperature range. An on-chip white clipping circuit protects the white processor (TDA4303) from output signals that are too large. If white clipping occurs, a pulse is available to kill the colour information. Highlights will always be white, not coloured.

Features

- Four variable gain amplifiers
- White clipping circuit
- Blanking switch
- 2.1 V reference voltage

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 20)	$V_P = V_{20\text{-}10}$	4.75	5.0	5.25	V
Reference voltage (pin 6)	V_{ref}	1.9	2.1	2.3	V
Total power dissipation	P_{tot}	90	140	200	mW
Storage temperature range	T_{stg}	−25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINES

TDA4306 : 20-lead DIL; plastic (SOT146).
TDA4306T: 20-lead mini-pack; plastic (SO20; SOT163A).

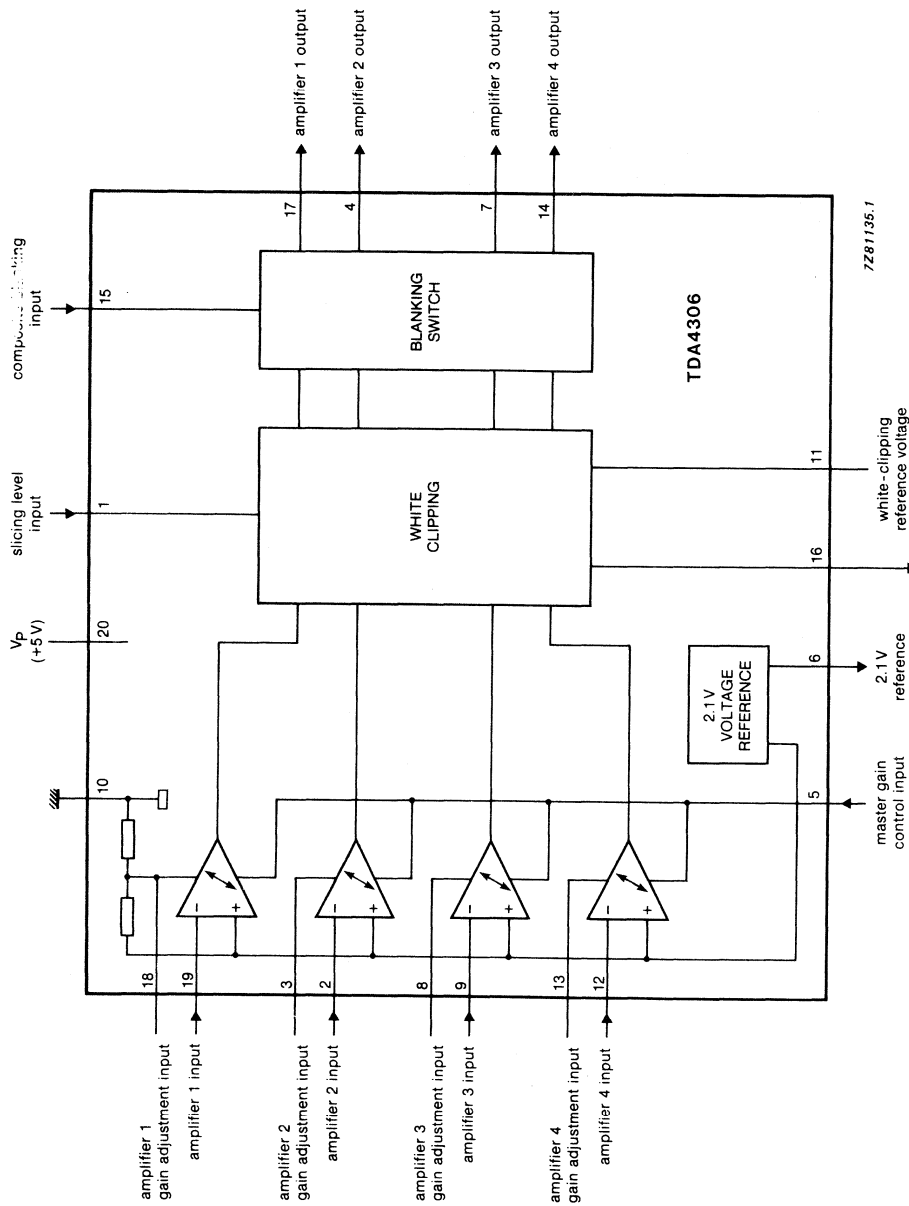


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 20)	V_P	–	12	V
Input voltage (pins 1, 2, 3, 5, 8, 9 12, 13, 15, 18 and 19)	V_I	–	5	V
Output current (pins 17, 4, 7 and 14) $t < 1$ s	I_O	–	100	mA
Total power dissipation				
SO package*	P_{tot}	–	370	mW
DIL package	P_{tot}	–	1000	mW
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−25	+ 150	°C

* Mounted on a printed-circuit board.

CHARACTERISTICS

$V_P = V_{20-10} = 5$ V; $T_{amb} = 25\,^{o}C$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 20)	V_P	4.75	5.0	5.25	V
Reference voltage (pin 6)	V_{ref}	1.9	2.1	2.3	V
Temperature drift of V_{ref}	ΔV_{ref}	–	0.18	–	mV/°C
External load current	$I_{L(ext.)}$	–	–	10	mA
Total power dissipation	P_{tot}	90	140	200	mW
Variable gain amplifiers					
Inputs (pins 2, 9, 12 and 19; note 1)					
Input voltage (peak-to-peak value)					
negative video	$V_{n-10(p-p)}$	–	–	–1100	mV
positive video (gain = 1)	$V_{n-10(p-p)}$	–	–	400	mV
Input bias current at $V_I = 2.6$ V	$I_{n(bias)}$	–	2.2	5	μA
Input resistance	$R_{2, 9, 12, 19}$	–	300	–	kΩ
Outputs (pins 17, 4, 7 and 14)					
DC offset voltage of input to output (output = V_{ref})		–	–	–220	mV
DC offset voltage of input to output (output = V_{ref})		–	–	100	mV
Offset voltage between blanked output and V_{ref}		–	–	2	mV
Drift of blanked output voltages	ΔV_O	10	–	–	μV/°C
Output sink current	I_{OS}	–	–	100	μA
Resistive load of output to ground	R_L	1.5	–	–	kΩ
Output voltage swing at $V_{ref} = 2.1$ V		–	V_{ref}–500 mV	–	
Output voltage swing at $V_{ref} = 2.1$ V		–	V_{ref}+ 1200 mV	–	
Output impedance	$\|Z_O\|$	–	100	–	Ω
Power supply rejection ratio (1 kHz)	RR	–	30	–	dB
Bandwidth	B	6	–	–	MHz

parameter	symbol	min.	typ.	max.	unit
Master gain control input (pin 5)					
Gain control range			see Fig. 2		
Input current at V_{5-10} = 0 V	I_5	–	–	30	μA
Matching of gain (note 2) between the 4 channels ($f_{temp.\ range}$ and as $f_{gain\ range}$ 2 to x 8)		–	–	1	%
Gain stability = $f_{temp.range}$ $-20 < t < 60$ °C		–	3	–	%
Differential gain	dG	–	–	1	%
Differential phase	dϕ	–	–	2	deg.
Gain adjustment inputs (pins 18, 3, 8, 13)					
Input voltage range	V_{adj}	0.9	–	1.9	V
Overall gain (MG = 2)					
at V_{adj} = 0.9 V	G	–	–	2.2	
at V_{adj} = 1.9 V	G	1.5	–	–	
Input current (pins 3, 8 and 13) at V_I = 1,6 V	I_I	–	–	2	μA
Input resistance (pin 18)	R_{18}	–	3.25	–	kΩ
Input voltage (pin 18; open-circuit)	V_I	–	1.2	–	V
White clipping circuit					
Slicing level (pin 1)					
input voltage range	V_{1-10}	0.5	–	1.8	V
input current at V_{1-10} = 1 V	I_1	–	–	2	μA
White clipping reference voltage (pin 11)	V_{11-10}	–	V_{1-10} x 2.5 V	–	V
Output pulse (pin 16) (peak-to-peak value)	$V_{16-10(p-p)}$	3.0	–	–	V
Output voltage (pin 16)					
LOW	V_{OL}	–	–	1	V
HIGH	V_{OH}	4	–	–	V
Output sink current (pin 16)	I_{OS}	–	–	0.1	mA
Delay of a variable gain amplifier input to white clipping output	t_d	–	–	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Blanking switch (pin 15)					
Composite blanking input voltage					
active HIGH	$V_{15\text{-}10}$	2.4	–	V_P	V
active LOW	$V_{15\text{-}10}$	–	–	1.4	V
Input current at $V_{15\text{-}10} = 5$ V	I_{15}	–	–	2	μA
Input capacitance	C_I	–	–	5	pF
Delay between blanking input and one of the 4 amplifier outputs	t_d	–	40	100	ns

Notes to the characteristics

1. The maximum input voltage is permitted only if the input voltage minus the DC offset voltage = 2.1 V. If the input voltage minus the DC offset voltage = 1.6 V, the maximum input voltage is 1 V(p-p).
2. Over the range 2 to x 8, after that each channel is adjusted to 0. This is possible only if the blanking pulse is switched off and the DC input voltage is equal to V_{ref}.

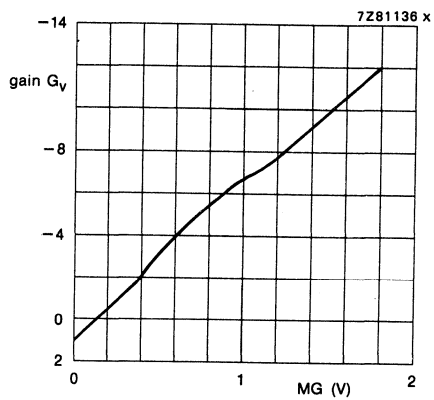


Fig.2 Gain as a function of V_{MG}.

SMALL SIGNAL COMBINATION IC FOR MONOCHROME TV

GENERAL DESCRIPTION

The TDA4500 combines all small signal functions (except the tuner) which are required for a monochrome television receiver.

For a complete monochrome television receiver only output stages are required to be added for horizontal and vertical deflection, video and sound. The TDA4500 can also be used in simple colour television receivers. In this application an external sandcastle pulse generator is required.

It incorporates the following functions:

- vertical sync separator/oscillator
- vertical output
- coincidence detector (sound mute)
- phase detector/frequency control
- a.g.c. detector
- sync separator
- horizontal oscillator
- synchronous demodulator
- vision i.f. amplifier
- tuner a.g.c.
- d.c. volume control
- a.f.c. detector
- video output
- sound demodulator
- audio output
- gate pulse generator
- sound limiter/feedback
- 90° phase shift
- overload detector
- horizontal output

QUICK REFERENCE DATA

Supply voltage	V_{7-10}, V_{22-10}	typ.	10,5	V
Supply current	I_7	typ.	75	mA
Supply current	I_{22}	typ.	4,5	mA
Operating ambient temperature range	T_{amb}		−25 to +65	°C
Storage temperature range	T_{stg}		−25 to +150	°C
Power dissipation	P_{tot}	max.	1,7	W

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT117).

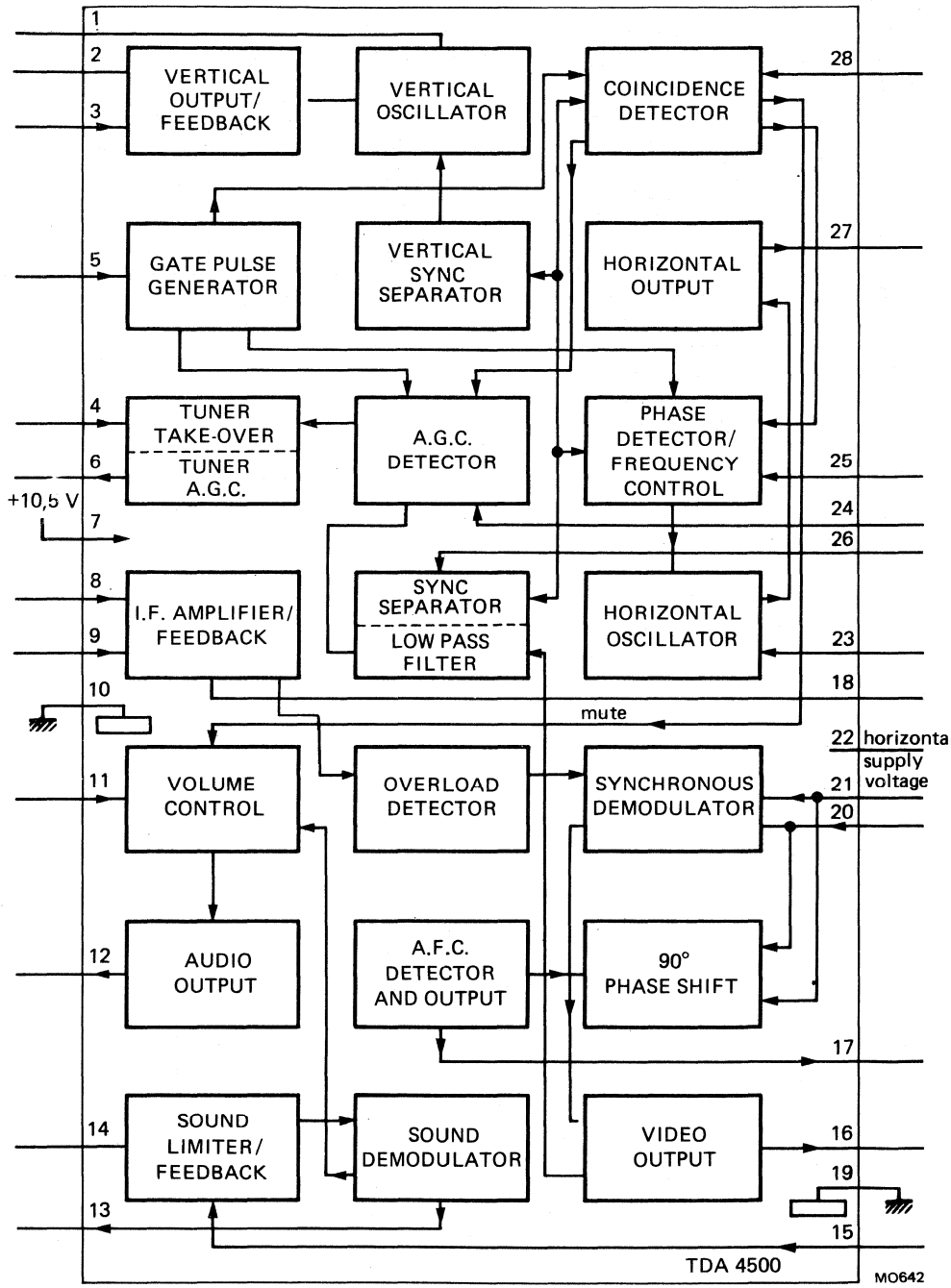


Fig. 1 Block diagram.

PINNING

Pin number	function	Pin number	function
1.	vertical oscillator	15.	sound i.f.
2.	vertical output	16.	video output
3.	vertical feedback	17.	a.f.c. output
4.	top linearity	18.	decoupling capacitor
5.	flyback pulse	19.	ground
6.	tuner a.g.c.	20.	38,5 MHz reference
7.	+10,5 V supply	21.	(38,9 MHz reference)
8.	i.f. input	22.	horizontal supply voltage
9.		23.	horizontal oscillator
10.	ground	24.	top sync detector
11.	volume control	25.	phase detector
12.	sound output	26.	sync separator
13.	6 MHz tuning (5,5 MHz tuning)	27.	horizontal output
14.	decoupling	28.	mute/coincidence detector

FUNCTIONAL DESCRIPTION (Fig. 1)

A complete black-and-white receiver can be built around this circuit by adding only the output stages for horizontal and vertical deflection with the video and sound output stages. The TDA4500 can also be used in simple colour television receivers using an external circuit to generate the sandcastle.

The block diagram (Fig. 1) depicts the various functions which are described briefly below.

The sensitivity of the i.f. amplifier is 70 μV for a peak-to-peak output voltage of 3 V (compare the TDA3541). This amplifier has a symmetrical input (pins 8 and 9) and is followed by a synchronous demodulator. The external tuned circuit is connected to pins 20 and 21. This circuit provides the information for the a.f.c. circuit, the 90^{o} phase shift being supplied by internal RC-networks. An a.f.c. output with a voltage swing of about 9 V is obtained from pin 17 (V_{7-10} = 10,5 V).

The a.g.c. detector is gated to reduce sensitivity to external electrical noise and the a.g.c. time constant network is connected to pin 24. Gain control range of the i.f. amplifier is greater than 60 dB. Adjustments of the tuner take-over point is made at pin 4. When the voltage at pin 4 is approximately 3,5 V the direction of the tuner control voltage is positive-going. When the voltage at pin 4 is approximately 8 V the direction of the tuner control voltage is negative-going.

An output signal of 3 V (p-p) is obtained from the video amplifier (top sync level 1,5 V) with negative-going sync. Since the sound signal is derived from pin 16 (see Fig. 4) the video output is not blanked during the flyback period. As shown in the application circuit (Fig. 4) the band-pass filter for the sound must be connected between video output (pin 16) and sound i.f. input (pin 15). Sound information passes through a sound limiter network and a sound demodulator circuit with an external tuned circuit for this stage connected to pin 13. The demodulator is followed by a volume control stage with a control range of 80 dB and an output amplifier with an audio output signal of 170 mV (r.m.s.) for a Δf of 7,5 kHz and at maximum volume setting.

The slicing level of the sync separator is referred to the top sync and is determined by the values of external resistors, the recommended slicing level being 30%. Noise protection is provided for the sync separator stage. Separated sync pulses are supplied to the gated phase detector which compare the sync pulses with the sawtooth voltage obtained from the horizontal flyback pulse (pin 5). During catching the gating of the phase detector is switched off and the phase detector output current is increased.

The in-sync or out-of-sync condition is detected with the coincidence detector which is also used for transmitter identification. Sound output is suppressed when no input signal is available. Clamping the voltage on pin 28 to a level of 3,5 V sets the phase detector to a high output current, short time constant mode. This is appropriate for the reception of VCR signals.

Phase detector output voltage levels maintain the horizontal oscillator at its correct operating frequency. The push-pull output (pin 27) has a typical duty cycle of 40%.

Vertical sync pulses are obtained from an internal integrating network with the vertical sawtooth being generated in the vertical oscillator. This sawtooth voltage is compared with the feedback voltage from the deflection coil via pin 3. The comparator generates the drive voltage for the vertical deflection output stage.

The TDA4500 has four supply pins. Pin 7 and pin 10 are for the main positive supply and circuit ground respectively.

Critical circuits are grounded by pin 19. Pin 22 is the supply for the horizontal oscillator. A low current supply (5 mA minimum) can be used to start the oscillator from an external high voltage supply rail.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_{7-10}, V_{22-10}	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		−25 to +65	°C

CHARACTERISTICS

V_{7-10} = 10,5 V, V_{22-10} = 10,5 V and T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{7-10}	9,5	10,5	13,2	V
Supply current	I_7	–	75	–	mA
Supply voltage (horizontal oscillator)	V_{22-10}	9,5	10,5	13,2	V
Supply current (horizontal oscillator, note 1)	I_{22}	–	4,5	–	mA
Power dissipation	P_{tot}	–	850	–	mW
Vision i.f. amplifier (pin 8)					
Input sensitivity (onset of a.g.c.) at 39,5 MHz (note 2)	$V_{i(rms)}$	–	70	–	μV
Differential input resistance (note 3)	R_i	–	800	–	Ω
Differential input capacitance (note 3)	C_i	–	6	–	pF
Gain control range	ΔG	–	56	–	dB
Output signal expansion for 50 dB input signal variation (note 4)	ΔV_o	–	1	–	dB
Maximum input signal	$V_{i\ max}$	–	50	–	mV
Video amplifier (note 5)					
Zero signal output level (note 6)	V_{16-10}	–	5	–	V
Top sync output level (note 7)	V_{16-10}	1,2	1,4	1,6	V
Video output signal amplitude (peak-to-peak value)	$V_{16-10(p-p)}$	2,75	3,0	3,25	V
Internal bias current of n-p-n emitter follower output transistor	I_B	1,4	2,0	–	mA
Bandwidth of demodulated output signal	B	5	6	–	MHz
Video non-linearity (note 8)		–	–	10	%

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuner a.g.c.					
Take-over voltage (pin 4) for positive-going tuner a.g.c. (n-p-n tuner)	V_{4-10}	–	3,5	–	V
Take-over voltage (pin 4) for negative-going tuner a.g.c. (p-n-p tuner)	V_{4-10}	–	8	–	V
Maximum tuner a.g.c. output swing	$I_{6\ max}$	2	3	–	mA
Output saturation voltage at I_6 = 2 mA	$V_{6-10(sat)}$	–	–	300	mV
Leakage current	I_6	–	–	1	μA
A.F.C. circuit (note 9)					
A.F.C. output voltage swing	V_{17-19}	9	–	10	V
Available output current	$\pm I_{17}$	–	1	–	mA
Output voltage at nominal tuning of the reference tuned circuit	V_{17-19}	–	5,25	–	V
Sound circuit					
Input limiting voltage when $V_O = V_{Omax} - 3$ dB (note 10)	$V_{14\ lim}$	–	400	–	μV
Input resistance at pin 15 (note 11)	R_i	–	3	–	kΩ
A.F. output signal at pin 12 (note 12) (r.m.s. value)	$V_{12-10(rms)}$	170	–	240	mV
Volume control (pin 11) (Fig. 3)					
Voltage with pin 11 disconnected	V_{11-10}	–	6,5	–	V
Current pin 11 short-circuited to ground	I_{11}	–	1	–	mA
Volume control characteristic (note 13)			See Fig. 3		
Value of external control resistor	R_{11-10}	–	5	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Horizontal synchronization circuit					
Slicing level sync separator (note 14)		–	30	–	%
Holding range PLL		–	±1000	–	Hz
Catching range PLL		–	±600	–	Hz
Control sensitivity video to flyback (note 15)		–	2	–	kHz/μs
Horizontal oscillator					
Free running frequency	f_{osc}	–	15625	–	Hz
Spread with fixed external components	Δf_{osc}	–	–	4	%
Frequency variations due to supply voltage changes (note 16)	$\Delta f_{osc}/\Delta V$	–	0	–	%
Frequency variation with temperature	$\Delta f_{osc}/\Delta T$	–	–	1×10^{-4}	K^{-1}
Maximum frequency shift	Δf_{osc}	–	–	10	%
Maximum frequency deviation between starting point output and nominal condition	Δf_{osc}	–	–	10	%
Horizontal (push-pull) output					
Output current	I_{27}	10	–	–	mA
Output impedance	R_{27-10}	–	200	–	Ω
Voltage when I_{27} = 10 mA	V_{27-10}	–	2	–	V
	V_{27-22}	–	3	–	V
Duty cycle of output pulse (note 17)	δ	0,35	0,40	0,45	
Flyback input (note 18)					
Minimum required input amplitude (peak-to-peak value)	$V_{5-10(p-p)}$	–	4	–	V
Phase detector switching voltage		–	0	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Coincidence detector (mute) (note 19)					
Voltage in synchronized condition	V_{28-19}	–	9,5	–	V
Voltage in non-synchronized condition (no-signal)	V_{28-19}	–	1,0	1,5	V
Switching level to switch phase detector from slow to fast	V_{28-19}	4,5	5,0	5,5	V
Switching level to activate the 'mute' function (transmitter identification)	V_{28-19}	2,25	2,5	2,75	V
Output current; in-sync (peak-to-peak value)	$I_{28(p-p)}$	–	1	–	mA
Vertical oscillator					
Free running frequency	f_{osc}	–	47,5	–	Hz
Spread with fixed external components	Δf_{osc}	–	–	4	%
Holding range at nominal frequency		52,5	–	–	Hz
Temperature coefficient	TC	–	1×10^{-4}	–	K^{-1}
Frequency shift due to a supply voltage change from 9,5 to 12 V	$\Delta f_{osc}/\Delta V$	–	5	–	%
Vertical output (pin 2)					
Output current	I_2	1	1,3	–	mA
Output resistance	R_{2-10}	–	2	–	kΩ
Feedback input (pin 3)					
D.C. input voltage	V_{3-10}	4,75	5	5,25	V
A.C. input voltage (peak-to-peak value)	$V_{3-10(p-p)}$	–	1,2	–	V
Input current	I_3	–	–	10	μA
Non-linearity of deflection current at V_P = 10,5 V		–	–	2,5	%

Notes to characteristics

1. It is possible to start the horizontal oscillator by supplying a current of 5 mA which can be taken from the mains rectifier, to pin 22. The main supply (pin 7) can then be derived from the horizontal output stage.
2. I.F. input voltage (r.m.s.) – value at top sync level at which the video amplitude has dropped 0,5 dB compared with the amplitude at an input signal of 10 mV.
3. The input impedance has been chosen such that a SAW-filter can be applied. 800 Ω is an acceptable compromise between the requirements for triple transient suppression and power loss.
4. Measured with 0 dB = 150 μV.
5. Measured at 10 mV(r.m.s.) top sync input signal.
6. With switched demodulator.
7. Signal with negative-going sync with top white being 10% of the top sync amplitude (Fig. 2).
8. This figure is valid for the complete video signal amplitude (peak-white to top sync).
9. Measured with an input signal (V_{8-9}) of 10 mV(r.m.s.); the a.f.c. output (pin 7) loaded with 2 x 100 kΩ between the supply and ground. The Q factor of the reference tuned circuit is 50.
10. Voltage at pin 15 is the r.m.s. value. Q_L of the demodulator tuned circuit is 20. Audio frequency is 1 kHz and the carrier frequency is 5,5 MHz.
11. Measured with an input signal of 1 mV(r.m.s.)
12. The tuned demodulator circuit must give an output level equal to that given in the "mute" condition.
13. Volume can be controlled using a variable resistor connected to ground (nominal 5 kΩ) or by means of a variable d.c. voltage. In this latter case the rather low impedance at pin 11 must be taken into account.

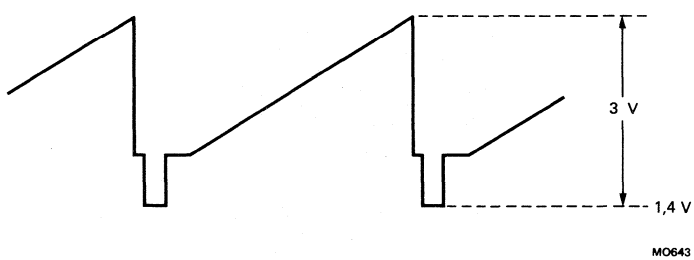


Fig. 2 Video output signal.

Notes to characteristics (continued)

14. The sync separator is noise gated. The slicing level is referred to top sync level and is independent of the video information. The value given is a percentage of the sync pulse amplitude. The slicing depends on the values of external resistors connected to pin 26.
15. Phase detector current increases by a factor of 7 during "catching" and when phase detector operates in the 'FAST' mode (pin 28). This ensures a high catching range and a higher dynamic loop gain.
16. Supply voltage variation in the range 8 to 12 V.
17. The negative-going edge of this pulse initiates the switch-off of the horizontal output transistor (simultaneous driver).
18. The circuit requires an integrated flyback pulse. The gate pulses for a.g.c. and the coincidence detector are obtained from the sawtooth.
19. The functions of in-sync/out-of-sync and transmitter identification have been combined on pin 28. For reception of VCR-signals the voltage on this pin must be fixed between 3 V and 4,5 V so that the time constant is fast and the sound is still available.

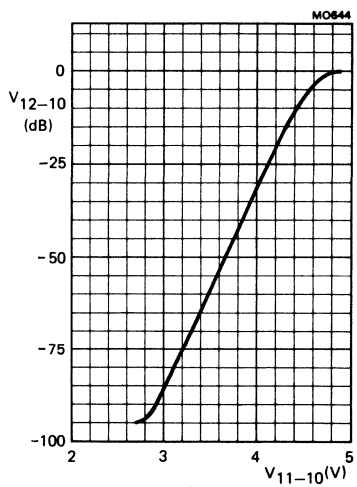


Fig. 3 Volume control characteristic at f = 1 kHz.

APPLICATION INFORMATION

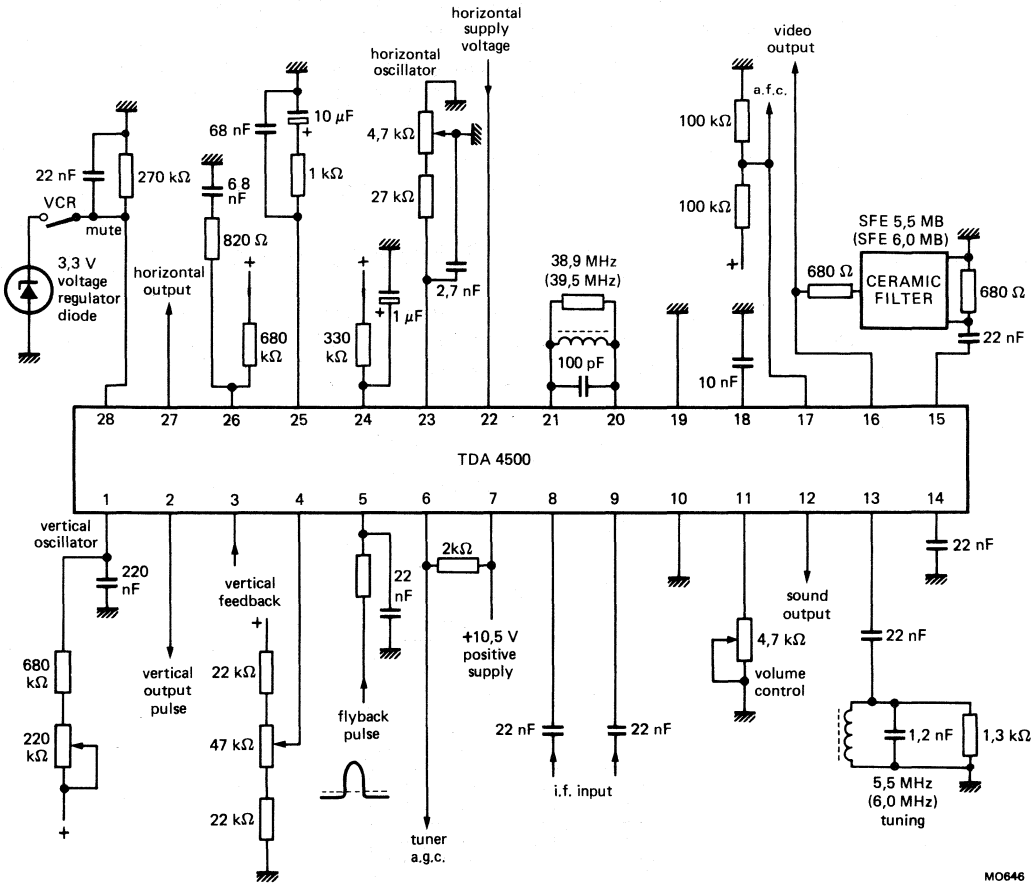


Fig. 4 Typical application circuit.

SMALL-SIGNAL COMBINATION IC FOR BLACK-AND-WHITE TV

GENERAL DESCRIPTION

This IC contains all small-signal functions required for black-and-white tv reception. The only additional circuits needed to complete the receiver are a tuner and the deflection output stages.

The IC includes a vision i.f. amplifier with synchronous demodulator and a.f.c. circuit, an a.g.c. detector with tuner output and fully synchronized vertical and horizontal drive outputs.

Sound signals are demodulated and amplified within the IC in a circuit which includes volume control and internal muting.

The TDA4503 may also be adapted for simple colour tv reception by the use of an external, three-level sandcastle pulse generator.

Features

- Vision i.f. amplifier with synchronous demodulator
- A.G.C. detector and amplifier with a.g.c. output to tuner
- A.F.C. circuit
- Video preamplifier
- Audio preamplifier
- Sound i.f. amplifier and demodulator
- D.C. volume control
- Horizontal synchronization circuit
- Transmitter identification and mute circuit
- Vertical synchronization circuit and sawtooth generator

QUICK REFERENCE DATA

Supply voltage (pin 7)	$V_{7\text{-}10}$	typ.	10,5	V
Supply current (pin 7)	I_7	typ.	82	mA
Supply voltage (pin 22)	$V_{22\text{-}10}$	typ.	10,5	V
Supply current (pin 22)	I_{22}	typ.	5	mA
Operating ambient temperature range	T_{amb}		−25 to + 65	°C
Storage temperature range	T_{stg}		−25 to +150	°C
Power dissipation	P_{tot}	typ.	920	mW

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117).

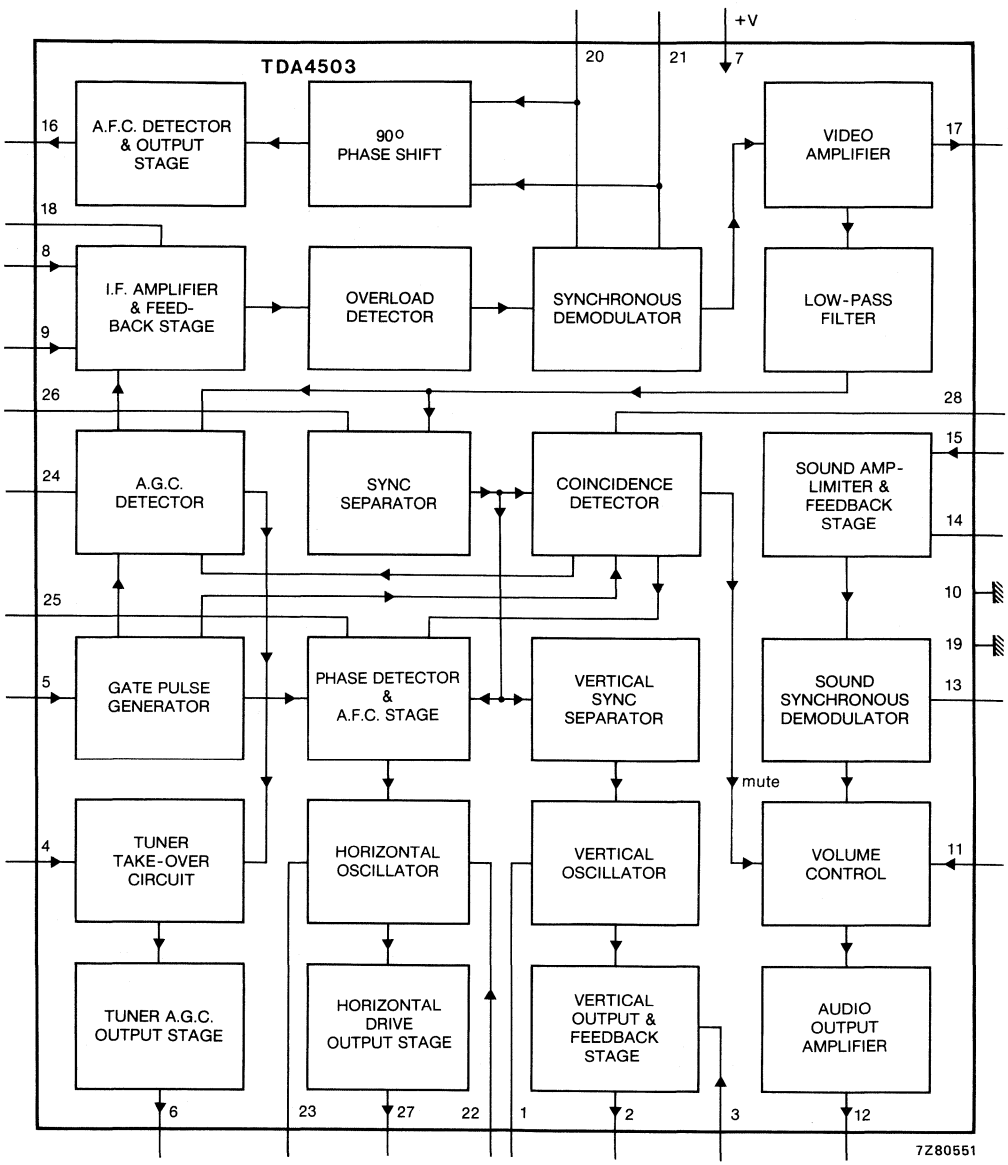


Fig. 1 Block diagram.

PINNING

1. Vertical oscillator input
2. Vertical drive output
3. Vertical drive feedback
4. Tuner take-over input
5. Flyback pulse input
6. A.G.C. output to tuner
7. Power supply input
8. I.F. input
9. I.F. input
10. Power supply return (ground)
11. Volume control
12. Audio output
13. Sound demodulator reference input
14. Sound i.f. decoupling
15. Sound i.f. input
16. A.F.C. output
17. Video output
18. I.F. amplifier decoupling
19. Ground (for critical circuits)
20. Synchronous demodulator
21. Synchronous demodulator
22. Horizontal oscillator start input
23. Horizontal oscillator
24. A.G.C. time constant
25. Horizontal phase detector filter
26. Sync separator slicing level
27. Horizontal drive output
28. Coincidence detector time constant

FUNCTIONAL DESCRIPTION

I.F. amplifier, demodulator and A.F.C.

The i.f. amplifier operates with symmetrical inputs at pins 8 and 9 and has an input impedance suitable for SAW filter application. The amplifier sensitivity gives a peak-to-peak output voltage of 3 V for an r.m.s. input of 70 μV. The demodulator and the a.f.c. circuit share an external reference tuned circuit (pins 20 and 21) and an internal RC-network provides the phase-shifting necessary for a.f.c. operation. The a.f.c. circuit provides a control voltage output with a (typical) swing of 9 V from pin 16 (V_P = 10,5 V).

A.G.C. circuit

Gating of the a.g.c. detector is performed to reduce sensitivity of the i.f. amplifier to external electrical noise. The a.g.c. time constant is provided by an RC-network connected to pin 24. The typical gain control range of the i.f. amplifier is 60 dB. Tuner a.g.c. voltage is supplied from pin 6 and is suitable for tuners with pnp or npn RF stages. The sense of the AGC (to incease in a positive or negative direction) and the point of tuner take-over are preset by the voltage level at pin 4 (V_4 = 3,5 V (typ) for positive a.g.c.; V_4 = 8 V (typ) for negative a.g.c.).

Video amplifier

The video signal output from pin 17 has a peak-to-peak value of 3 V (top sync level = 1,5 V) and carries negative-going sync. In order to retain sound information at pin 17, the video signal is not blanked during flyback periods.

Sound circuit

The sound i.f. signal present at the video output (pin 17) is coupled to the sound circuit by a band-pass filter to pin 15. The sound circuit has an amplifier-limiter stage, a synchronous demodulator with reference tuned circuit at pin 13, a volume control stage and an output amplifier. The volume control has a range of approximately 80 dB and the audio output signal at maximum volume and with Δf = 7,5 kHz is 320 mV (r.m.s. value). The sound output signal is suppressed when no input signal is detected.

Synchronization circuits

The sync separator slicing level is determined by an external resistor network at pin 26. The slicing level is referred to the top sync level and the recommended value for slicing is 30%. Internal protection from electrical noise is included.

A gated phase detector compares the phase of the separated sync pulses with a sawtooth waveform obtained from the flyback pulse at pin 5. In-sync and out-of-sync conditions are detected by the coincidence detector at pin 28 (this circuit also gives transmitter identification). During the out-of-sync condition, gating of the phase detector is switched off and the output current from the phase detector increases to give the detector a short time-constant and thus a fast response. This condition can be imposed by clamping the voltage at pin 28 to 3,5 V for the reception of VCR signals.

The horizontal oscillator frequency is controlled by the output voltage of the phase detector circuit. The horizontal drive output from pin 27 has a duty factor of 40%.

Vertical sync pulses are separated by an internal integrating network and are used to trigger the vertical oscillator. A comparator circuit compares the vertical sawtooth waveform, generated by the vertical oscillator, with feedback from the deflection coils and supplies the drive voltage for the output stage at pin 2.

Power supplies

The main supply is to pin 7 (positive supply) and pin 10 (ground). The horizontal oscillator is supplied from pin 22 to facilitate starting of the oscillator from a high-voltage rail. A special ground connection at pin 19 is used by critical voltage dividers in the feedback loops of the vision and sound i.f. circuits.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-10}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Operating ambient temperature range	T_{amb}		−25 to + 65 °C
Storage temperature range	T_{stg}		−25 to +150 °C

CHARACTERISTICS

V_{7-10} = 10,5 V; V_{22-10} = 10,5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 7)	V_{7-10}	9,5	10,5	13,2	V
Supply current (pin 7)	I_7	–	82	100	mA
Supply voltage (pin 22)	V_{22-10}	9,5	10,5	13,2	V
Supply current (pin 22) (note 1)	I_{22}	–	5	6,5	mA
Total power dissipation	P_{tot}	–	920	1150	mW
Vision i.f. amplifier (pins 8 and 9)					
Input sensitivity at 38,9 MHz (note 2)	V_{8-9}	40	80	120	μV
Input sensitivity at 45,75 MHz (note 2)	V_{8-9}	–	90	–	μV
Differential input resistance (pin 8 to 9)	R_{8-9}	–	1,3	–	kΩ
Differential input capacitance (pin 8 to 9)	C_{8-9}	–	5	–	pF
A.G.C. range		–	59	–	dB
Maximum input signal	V_{8-9}	50	70	–	mV
Expansion of output signal (pin 17) for 50 dB variation of input signal (pins 8 and 9) (note 3)	ΔV_{17-10}	–	0,5	1,0	dB
Video amplifier (note 4)					
Output level for zero signal input (zero point of switched demodulator)	V_{17-10}	4,2	4,5	4,8	V
Output signal top sync level (note 5)	V_{17-10}	1,25	1,45	1,65	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Amplitude of video output signal (peak-to-peak value)	$V_{17\text{-}10(p\text{-}p)}$	2,4	2,7	3,0	V
Internal bias current of output transistor (npn emitter follower)	$I_{17(int)}$	1,4	2,0	–	mA
Bandwidth of demodulated output signal	B	–	5	–	MHz
Differential gain (Fig. 4 and note 6)	G_{17}	–	6	–	%
Differential phase (Fig. 4 and note 6)		–	4	–	%
Video non-linearity over total video amplitude (peak white to black)		–	–	10	%
Intermodulation (Figs 5 and 6) at gain control = 45 dB					
f = 1,1 MHz; blue;		55	60	–	dB
f = 1,1 MHz; yellow;		50	54	–	dB
f = 3,3 MHz; blue;		60	66	–	dB
f = 3,3 MHz; yellow;		55	59	–	dB
Signal-to-noise ratio (note 7)					
at V_i = 10 mV	S/N	50	54	–	dB
at end of a.g.c. range	S/N	50	56	–	dB
as a function of input signal		see Fig. 7			
Residual A.M. of intercarrier output signal (note 8)		–	5	10	%
Residual carrier signal		–	7	30	mV
Residual 2nd harmonic of carrier signal		–	3	30	mV
Tuner a.g.c. (note 9)					
Take-over voltage (pin 4) for positive-going tuner a.g.c. (NPN tuner)	$V_{4\text{-}10}$	–	3,5	–	V
Starting point take-over at $V_{4\text{-}10}$ = 5 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	–	0,4	2,0	mV
Starting point take-over at $V_{4\text{-}10}$ = 1,2 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	50	70	–	mV
Take-over voltage (pin 1) for negative-going tuner a.g.c. (PNP tuner)	$V_{4\text{-}10}$	–	8	–	V
Starting point take over at $V_{4\text{-}10}$ = 9,5 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	–	0,3	2,0	mV
Starting point take over at $V_{4\text{-}10}$ = 5,6 V (r.m.s. value)	$V_{8\text{-}9(rms)}$	50	70	–	mV
Maximum tuner a.g.c. output swing	I_{6max}	2	3	–	mA
Output saturation voltage at I_6 = 2 mA	$V_{6\text{-}10(sat)}$	–	–	300	mV
Leakage current at pin 6	I_6	–	–	1	μA
Input signal variation required for complete tuner control	$\Delta V_{8\text{-}9}$	0,5	2	4	dB

parameter	symbol	min.	typ.	max.	unit
A.F.C. circuit (pin 16; note 10)					
A.F.C. output voltage swing (peak-to-peak value)	$V_{16\text{-}10(p\text{-}p)}$	9	–	10	V
Available output current	$\pm I_{16}$	–	1	–	mA
Control steepness at					
100% picture carrier		20	40	80	mV/kHz
10% picture carrier		–	15	–	mV/kHz
Output voltage at nominal tuning of the reference tuned circuit	$V_{16\text{-}10}$	–	5,25	–	V
Output voltage without input signal	$V_{16\text{-}10}$	2,7	6,0	8,5	V
Sound circuit					
Input limiting voltage (note 11) (r.m.s. value) at $V_o = V_{o\ max}$ - 3 dB	$V_{15\ lim}$	–	2	–	mV
Input resistance at $V_{i(rms)}$ = 1 mV	$R_{15\text{-}10}$	–	2,6	–	kΩ
input capacitance at $V_{i(rms)}$ = 1 mV	$C_{15\text{-}10}$	–	6	–	pF
A.M. rejection (Figs 8 and 9) at					
V_i = 10 mV	AMR	–	35	–	dB
V_i = 50 mV	AMR	–	43	–	dB
A.F. output signal (note 12) (r.m.s. value)	$V_{12\text{-}6(rms)}$	220	320	–	mV
A.F. output impedance	$Z_{12\text{-}10}$	–	150	–	Ω
Total harmonic distortion (note 12)	THD	–	1	–	%
Ripple rejection at					
f_k = 100 Hz, volume control 20 dB	RR	–	22	–	dB
when muted	RR	–	26	–	dB
Output voltage in mute condition	$V_{12\text{-}10}$	–	2,6	–	V
Signal-to-noise ratio; weighted noise (CCIR 468)	S/N	–	47	–	dB
Volume control					
Voltage (pin 11 disconnected)	$V_{11\text{-}10}$	–	6,9	–	V
Current (pin 11 connected to ground)	I_{11}	–	1	–	mA
External control resistor (note 13)	$R_{11\text{-}10}$	–	5	–	kΩ
Suppression of output signal during mute condition		–	66	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Horizontal synchronization					
Slicing level sync separator (note 14)		–	30	–	%
Phase-lock loop holding range		±800	±1100	±1500	Hz
Phase-lock loop catching range		±600	1000	–	Hz
Control sensitivity video to flyback (note 15)		–	2,3	–	kHz/μs
Delay between leading edge of sync pulse and zero cross-over of sawtooth (pin 5)		–	3	–	μs
Horizontal oscillator (pin 23)					
Free-running frequency R = 35 kΩ; C = 2,7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		–	–	4	%
Frequency variation due to change of supply voltage from 8 to 12 V	Δf_{fr}	–	0	0,5	%
Temperature coefficient	TC	–	–	1×10^{-4}	K^{-1}
Maximum frequency shift	Δf_{fr}	–	–	10	%
Maximum frequency deviation(V_{7-10} = 8 V)	Δf_{fr}	–	–	10	%
Horizontal output (pin 27)					
Output current	I_{27}	5	–	–	mA
Output impedance	R_{27}	–	200	–	Ω
Output voltage at I_{27} = 5 mA	V_{27-10}	–	1,4	–	V
	V_{27-22}	–	2,5	–	V
Duty factor of horizontal output signal (note 16)	α	0,35	0,40	0,45	%
Rise and fall times of output pulse	t_r, t_f	–	400	–	ns
Flyback input (pin 5)					
Amplitude of input pulse	V_5	2	4	6	V
Voltage at which gate pulse generator changes state (note 17)	V_5	–	0	–	V

parameter	symbol	min.	typ.	max.	unit
Coincidence detector mute output (pin 28) (note 18)					
Voltage for in-sync condition	V_{28-10}	–	9,5	–	V
Voltage for no-sync condition (no input signal)	V_{28-10}	–	1,0	1,5	V
Voltage level for phase detector to switch from slow to fast	V_{28-10}	3,7	4,1	4,5	V
Fast-to-slow hysteresis		–	1	–	V
Voltage level to activate mute function (transmitter identification)	V_{28-10}	2,25	2,5	2,75	V
Output current for in-sync condition (peak-to-peak value)	$I_{22(p-p)}$	0,7	1,0	–	mA
Vertical oscillator (pin 1)					
Free-running frequency at C = 220 nF; R = 560 kΩ	f_{fr}	–	47,5	–	Hz
Spread with fixed external components		–	–	4	%
Holding range at nominal frequency		52,5	–	–	Hz
Temperature coefficient	TC	–	–	$2x10^{-4}$	K^{-1}
Frequency variation due to change of supply voltage from 9,5 to 12 V	Δf_{fr}	–	3	5	%
Leakage current at pin 1	I_1	–	–	1,6	μA
Vertical output (pin 2)					
Output current	I_2	1	1,3	–	mA
Output resistance	R_2	–	2	–	kΩ
Feedback input (pin 3)					
Input voltage d.c. component a.c. component (peak-to-peak value)	 V_{3-10} $V_{3-10(p-p)}$	 4,0 –	 5,0 1,2	 5,5 –	 V V
Input current	I_3	–	–	12	μA
Non-linearity of deflection current at V_{7-10} = 10,5 V	ΔI_3	–	–	2,5	%
Delay between leading edge of vertical sync and start of vertical oscillator flyback		6	–	10	μs

Notes to the characteristics

1. The horizontal oscillator can be started by supplying a current of 6 mA to pin 22. Taking this current from the mains rectifier allows the positive supply voltage to pin 7 to be derived from the horizontal output stage (the load current of pin 27 is additional to the 6 mA quoted).
2. At start of a.g.c.
3. Measured with 0 dB = 200 μV.
4. Measured at 10 mV (rms) top sync output signal.
5. Signal with negative-going sync; top white = 10% of the top sync amplitude.
6. Measured with test line as shown in Fig. 4. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest values relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angles.
7. Measured with a source impedance of 75 Ω.

$$\text{Signal-to-noise ratio} = 20\log \frac{V_o \text{ black-to-white}}{V_{i(rms)} \text{ at B = 5 MHz}}.$$

8. Measured with a sawtooth-modulated input signal: m = 90%; $V_{i(rms)}$ = 10 mV;

$$\text{Amplitude modulation} = \frac{V_o \text{ SC at top sync} - V_o \text{ SC at white}}{V_o \text{ SC at top sync} + V_o \text{ SC at white}} \times 100\%.$$

(SC = sound carrier)

9. Starting point of tuner take-over for an npn tuner is when I_6 = 1,8 mA, and for a pnp tuner is when I_6 = 0,2 mA.
10. Measured at $V_{8\text{-}9(rms)}$ = 10 mV and pin 16 loaded with 2 x 100 kΩ between V_7 and ground. Reference tuned circuit Q-factor = 36.
11. Reference tuned circuit Q-factor = 16; audio frequency = 1 kHz; carrier frequency = 5,5 MHz.
12. The demodulator tuned circuit must be tuned for minimum distortion; output signal is measured at Δf = 7,5 kHz; other measurements are at Δf = 27,5 kHz.
13. Volume control can be realized by a variable resistor (5 kΩ) connected between pin 11 and ground, or by a variable voltage direct to pin 11 (the low value of input impedance to pin 11 must be taken into account).
14. The sync separator is noise-gated; the slicing level is referred to the top sync level and is independent of the video signal. The value stated is a percentage of the sync pulse amplitude, the level being dependent on external resistors connected to pin 26.
15. The phase detector current is increased by a factor of 7 during catching and when the phase detector is switched to 'fast' via pin 28, thus ensuring a wide catching range and a high dynamic loop gain.
16. The negative-going edge initiates switching-off of the line output transistor (simultaneous driver).
17. The circuit requires an integrated flyback pulse. Gate pulses for a.g.c. and coincidence detectors are obtained from the sawtooth waveform.
18. The functions of in-sync, out-of-sync and transmitter identification are combined on pin 28. For the reception of VCR signals, V_{28} must be fixed between 3 V and 4,5 V so that the time constant is fast and sound information is preserved.

APPLICATION INFORMATION

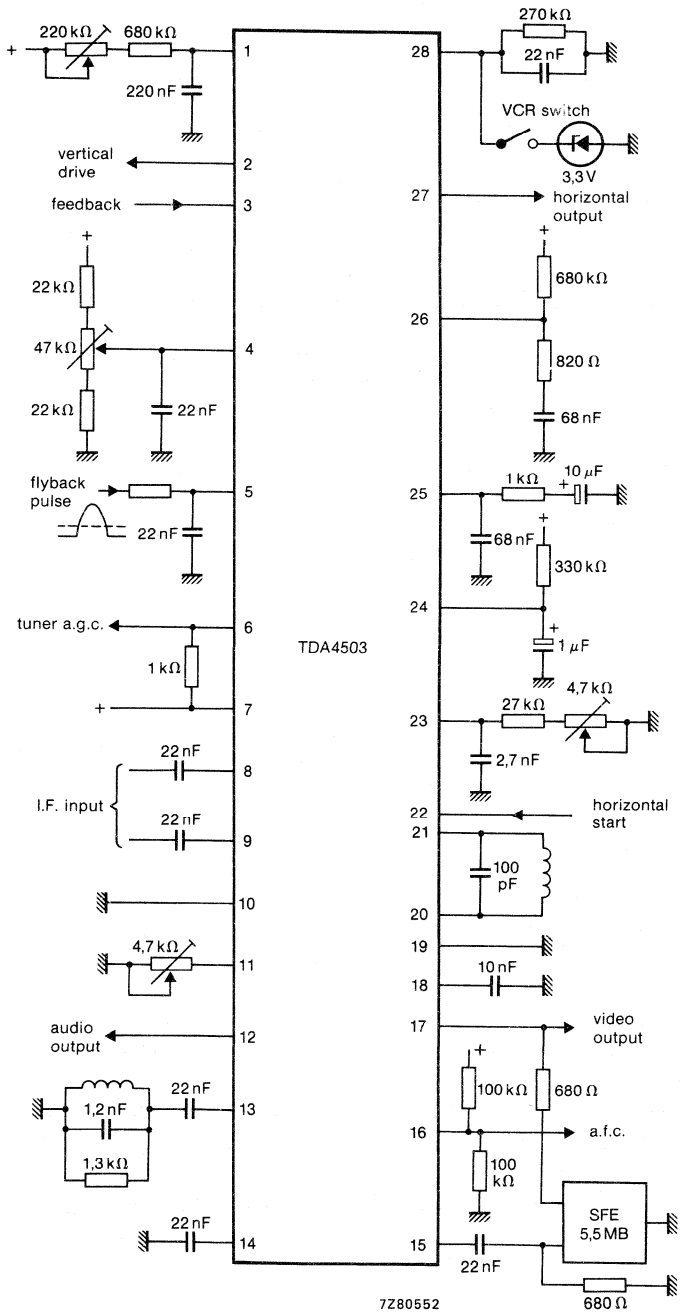


Fig. 2 Application circuit diagram.

APPLICATION INFORMATION (continued)

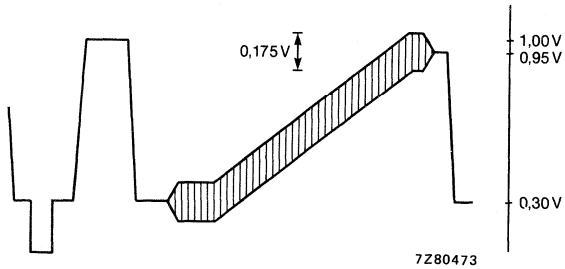


Fig. 3 Video output signal.

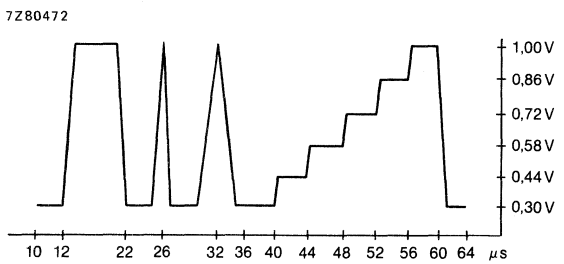


Fig. 4 E.B.U. test signal - line 330.

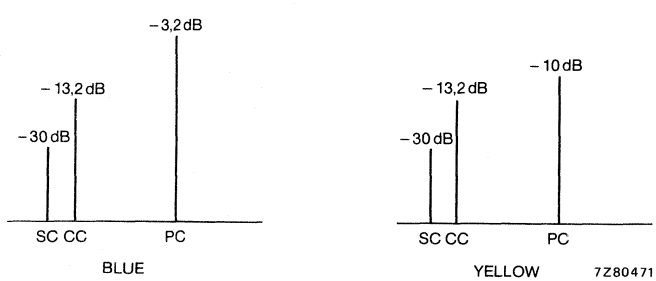


Fig. 5 Input signal conditions for intermodulation test: SC = sound carrier; CC = chrominance carrier; PC = picture carrier; all values are with respect to the top sync level.

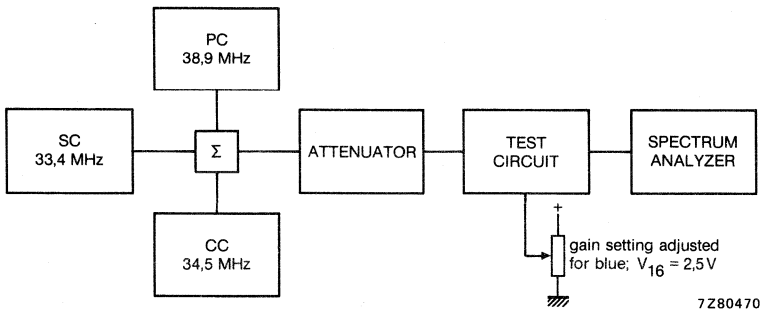


Fig. 6 Circuit for intermodulation test:

$$\text{value at 1,1 MHz} = 20\log \frac{V_o \text{ at 4,4 MHz}}{V_o \text{ at 1,1 MHz}} + 3{,}6 \text{ dB};$$

$$\text{value at 3,3 MHz} = 20\log \frac{V_o \text{ at 4,4 MHz}}{V_o \text{ at 3,3 MHz}}.$$

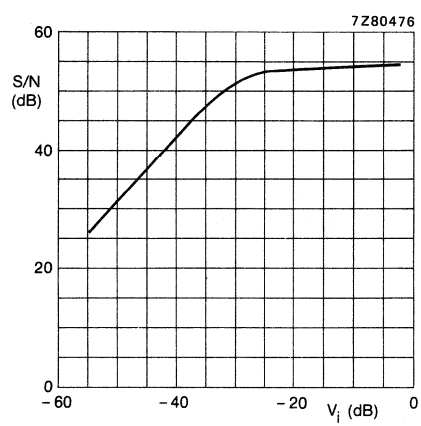


Fig. 7 Signal-to-noise ratio as a function of input voltage.

APPLICATION INFORMATION (continued)

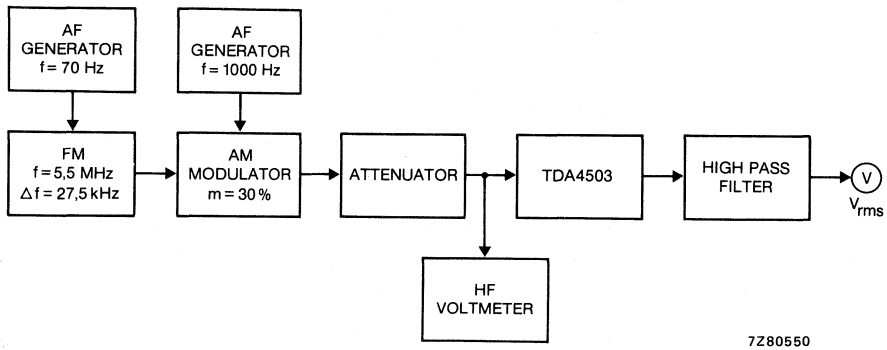


Fig. 8 Circuit for amplitude modulation rejection test.

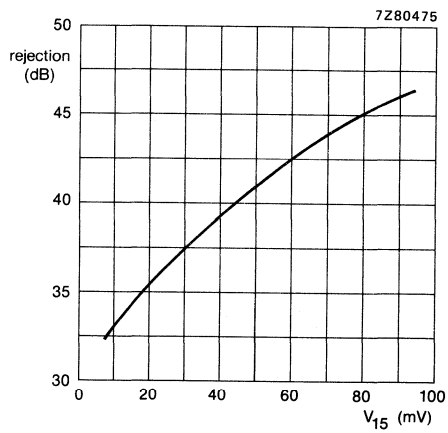


Fig. 9 Typical amplitude modulation rejection curve.

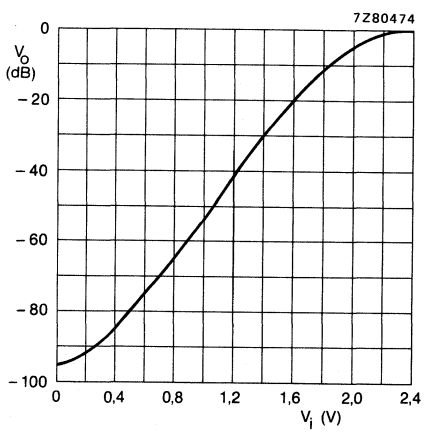


Fig. 10 Volume control characteristic.

Small signal combination for multistandard colour TV

TDA4504B

FEATURES

- Gain controlled vision IF amplifier
- Synchronous demodulator for negative and positive demodulation
- AGC detector operating on peak sync amplitude for negative demodulation and on peak white level for positive demodulation
- Tuner AGC
- AFC circuit with two control polarities and on/off-switch
- Video preamplifier
- Video switch to select either the internal video signal or an external video signal
- Horizontal oscillator and synchronization circuit with two control loops
- Vertical synchronization (divider system), ramp generator and driver with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Sandcastle pulse generation
- VCR/auto VCR switch
- Start-up circuit
- Vertical guard

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4504B	32	DIL	plastic	SOT201

GENERAL DESCRIPTION

Having the capability to demodulate IF signals with either positive or negative-going video information, the TDA4504B (Fig.1) is contained within a 32 pin encapsulation. It includes a three-stage vision IF amplifier, mute circuit, AFC and AGC circuitry, fully synchronised horizontal and vertical timebases with drive circuits and integral three-level sandcastle pulse generator. A functional colour tv receiver can thus be realized with the addition of a tuner, audio demodulator and amplifier, chroma decoder and respective line and field deflection circuitry.

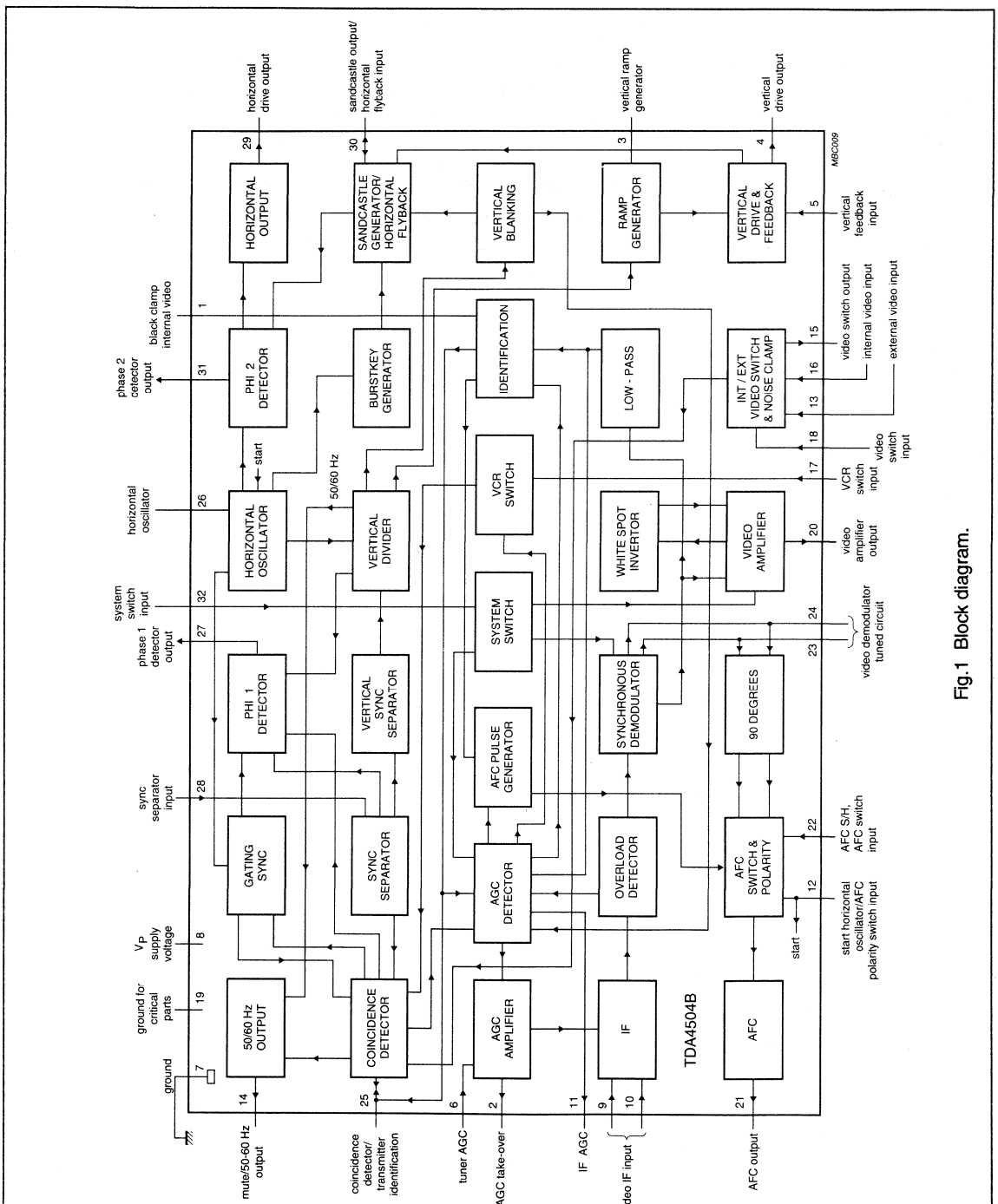


Fig.1 Block diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_8	positive supply voltage pin 8		10	12	13.2	V
I_8	supply current pin 8		90	115	140	mA
I_{12}	start current pin 12		–	6.5	9	mA
Video						
$V_{9\text{-}10}$	IF sensitivity (RMS value)		25	40	65	μV
$G_{9\text{-}10}$	IF gain control range		-	74	-	dB
S/N	signal to noise ratio	V_i input signal = 10 mV	-	58	-	dB
V_{21}	AFC output voltage swing		10.5	-	11.5	V
	video output amplitude		-	2	-	V
Video switch						
$16_{(p\text{-}p)}$	internal video input		-	2	-	V
$V_{13(p\text{-}p)}$	external video input		-	1	-	V
$V_{15(p\text{-}p)}$	video output		-	2.5	-	V
Sync						
V_{28}	sync pulse input amplitude (p-p)		200	-	-	mV
I_{30}	flyback input current		0.1	-	2	mA
V_{30}	sandcastle output during burst key		8	-	-	V
	- during hor. blanking		4	4.4	5	V
	- during vert. blanking		2.1	3.3	3.7	
V_{14}	video transmitter identification					
	- no signal condition		-	0.3	-	V
	- 50 Hz signal		-	12	-	V
	- 60 Hz signal		-	9	-	V
V_5	vert. feedback					
	- DC voltage		2.9	3.3	3.7	V
$V_{5(p\text{-}p)}$	- AC voltage		-	1	-	V

PINNING

PIN	DESCRIPTION
1	black level internal video
2	AGC take over (output)
3	vertical ramp generator (output)
4	vertical drive (output)
5	vertical feedback (input)
6	tuner AGC (input)
7	ground
8	supply voltage
9	vision IF (input)
10	vision IF (input)
11	IF AGC (output)
12	start horizontal oscillator (output)/AFC polarity switch (input)
13	external video (input)
14	mute/50 / 60 Hz (output)
15	video switch (output)
16	internal video (input)
17	VCR switch (input)
18	video switch (input)
19	ground for some critical parts
20	video amplifier (output)
21	AFC (output)
22	AFC S/H, AFC switch (input)
23	vision demodulator tuned circuit
24	vision demodulator tuned circuit
25	coincidence detector/transmitter identification
26	horizontal oscillator
27	phase 1 detector (output)
28	sync separator (input)
29	horizontal drive (output)
30	sandcastle output/horizontal flyback (input)
31	phase 2 detector (output)
32	AGC system switch (input)

FUNCTIONAL DESCRIPTION

Vision IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permit the omission of DC feedback and possess a control range in excess of 20 dB.

The IF amplifier, which is completely symmetrical, is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator.

A noise clamp circuit is provided at the video input (pin 16) to limit interference pulses below the sync tip level and is more efficient than a noise inverter in providing improved picture stability during the presence of interference.

The video amplifier has good linearity and bandwidth figures.

AFC-circuit

Obtaining the AFC reference signal from the demodulator tuned circuit presents the advantage of utilizing a single tuned circuit and one adjustment. However, since the frequency spectrum of the signal applied to the demodulator is determind by the characteristic of the SAW filter, the resultant asymmetrical spectrum with respect to the vision carrier causes the AFC output voltage to be dependent upon the video signal. The TDA4504B thus contains a sample-and-hold circuit.

With negative-going vision signals the AFC is active only during the sync pulse period. When positive-going signals are applied to the device, however, the AFC is continuously active but filtered to ensure only a small by-pass current is present in the sample-and-hold circuit.

With weak input signals the drive signal will contain considerable noise which also possesses an asymmetrical frequency spectrum and could create an offset in the AFC output voltage. The inclusion of a notch in the demodulator tuned circuit minimises this effect.

The sample-and-hold circuit is followed by a high impedance output amplifier. Thus the AFC control gradient depends upon the load impedance.

The AFC polarity switch is combined with the start circuit (pin 12). It has a negative slope when pin 12 is open or connected to the main supply and a positive slope when pin 12 is grounded. The AFC is disabled when the sample connection (pin 22) is grounded.

AGC circuit

For signals employing negative modulation the AGC detector operates on peak sync level but upon peak white content with those having positive modulation. Selection is facilitated by the system switch (pin 32):

pin 32	HIGH/open:	positive modulation
pin 32	LOW:	negative modulation

The AGC detector currents are:

	positive modulation	negative modulation
charge	1 μA	55 μA
discharge	3 mA	1.5 mA

With a 6.8 μF AGC capacitor, the video tilt will be < 10% for positively modulated signals and < 2% for negative modulation.

To obtain a rapid AGC action when executing a search tuning operation with the circuit set for peak white AGC, the charge current is held at 55 μA until the detection of a transmitted signal.

The transmitter identification

A mute signal is generated to disable the audio preamplifier of an audio demodulator during the absence of a transmission signal. When the video switch is in the internal mode, the identification of a transmitted signal is derived from the coincidence detector.
In the external mode the IF part of the circuit has its own identification system. The system relies upon the detection of sync. pulses on the incoming IF signal. The separated horizontal sync pulse charges the capacitor on pin 25 which drives the mute output (pin 14).

The connection of a 1 MΩ resistor between pin 25 and V_{CC} results in the mute information being overruled by the 50/60 Hz information derived from the internal vertical divider section (see 50/60 Hz truth table).

MUTE Truth Table:

Input signal Pins 9 and 10	50 Hz	60 Hz	none	50/60 Hz	50/60 Hz	50/60 Hz	none
pin 25	9.5 V	9.5 V	0.3 V	9.5	9.5	9.5	0.3
pin 28	50 Hz	60 Hz	none	50 Hz	60 Hz	none	50/60 Hz
pin 18	LOW	LOW	LOW/ HIGH	HIGH	HIGH	HIGH	HIGH
pin 14	12 V	9 V	0.3 V	12 V	9 V	12 V	0.3 V

50/60 Hz Information

In the external video mode and with a resistor of 1 MΩ from pin 25 to V_{CC} the mute is overruled by the 50/60 Hz information from the divider system.

50/60 Hz Truth Table:

Input Signal / Pin 9/10	50 Hz	60 Hz	None	Don't care	Don't care	Don't care
Pin 25	9.5	9.5	0.3	9.5	9.5	9.5
Pin 28	**50 Hz**	**60 Hz**	**None**	**50 Hz**	**60 Hz**	**None**
Pin 18	LOW	LOW	LOW	HIGH	HIGH	HIGH
Pin 14	12	9	0.3	12	9	12

VCR switch

Flywheel horizontal synchronization is desirable when receiving weak signals marred by noise but is usually unnecessary when receiving stronger off-air signals unless certain types of interference or multipath reception are apparent. Due to the inherent instability of VCR signals, however, the horizontal time constant should be shorter to prevent loss of horizontal synchronization in the early part of the scan. Provision is therefore incorporated to automatically switch the short time constant such that a strong signal instigates the 'VCR' mode and a weak signal triggers the 'TV' mode. The connection of a switch to pin 17 provides for this to be accomplished manually and may take the form of an auxiliary switching function associated with a designated program selector button.

Video-switch

Video output from the demodulator is filtered to remove the audio carrier and DC-coupled to pin 16. If AC-coupling is employed the internal noise clamp will operate on sync. tips.

The TDA4504B provides the opportunity for a direct video connection (e.g. via a peritel connector) to be made to the device at pin 13. Selection between internal and external video is made by applying a switching potential to pin 18.

Video switch:

pin 18	LOW:	internal video
pin 18	HIGH:	external video

Gain reduction

To prevent crosstalk between the IF stages and the horizontal oscillator when the device is operated in its external video mode with no RF input, the TDA4504B incorporates an option to reduce IF gain by 20 dB. This is accomplished by connecting a 39 kΩ resistor between pin 17 and ground. Omission of this component results in the IF amplifier remaining at full gain.

In the internal video mode the resistor must be disconnected to achieve the auto-VCR mode.

The TDA4504B has a separate pin (pin 17) for the VCR switch:

pin 17	HIGH:	VCR mode	fast time constant; ungated
pin 17	n.c.:	auto VCR mode	
pin 17	LOW:	TV mode	slow time constant; gated

Horizontal synchronization

The horizontal synchronization circuit of the TDA4504B has been designed as follows:

- The retrace of the horizontal oscillator occurs during the horizontal retrace and not during the scan period. This has the advantage that no interference will be visible on the screen when receiving weak input signals. Video crosstalk will not disturb the phase of the horizontal locking.
- Reduced frequency shift of the horizontal oscillator due to noise since the horizontal phase detector reference signal is more symmetrical and independent of the supply voltage and temperature.
- The phase detector current ratio for strong and weak signals is increased to obtain a better performance during both VCR playback and weak signal reception. The switching level is also independent of temperature and supply voltage.

Vertical synchronization

Generation of the vertical sawtooth (pin 3) is accomplished by a divider that permits the production of a vertical frequency of either 50 Hz or 60 Hz with freedom from adjustment, amplitude correction and maximum interference/disturbance protection.

A discriminator window checks the vertical trigger pulse. When the trigger pulse occurs before count 576, the divider system operates in the 60 Hz mode otherwise the 50 Hz mode is selected. (2 clock pulses equal one horizontal line).

The divider section operates with different reset windows. These windows are activated via an up/down counter. This increases its count by 1 for each occasion the separated vertical sync pulse is within the selected window. On each occasion the vertical sync. pulse is not within the selected window, the count is reduced by 1.

LARGE (SEARCH) WINDOW; DIVIDER RATIO BETWEEN 488 - 722

This mode is valid for the following conditions:

1 divider locking to another transmitter
2 divider ratio found, not within the narrow window limits
3 up/down counter value of the divider system operating in narrow window mode, count falls below 10.

NARROW WINDOW; DIVIDER RATIO BETWEEN 522 - 528 (60 Hz) OR 622 - 628 (50 Hz)

The divider switches to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the count lowered by 1. At a counter value below 10, the divider switches to the large window mode.

An anti-top flutter pulse is also generated by the divider system. This inhibits the horizontal phase-1 detector during the vertical sync pulse. The width of this pulse depends upon the divider mode. For the large window mode the start is generated at the divider reset. In the narrow window mode the anti-top flutter pulse starts at the beginning of the first equalizing pulse. The anti-top flutter pulse ends at count 10 for 50 Hz and count 12 for 60 Hz.

When out-of-sync is detected by the coincidence detector, the divider is switched to count 625. This results in a stable vertical amplitude when no input signal is available.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{stg}	storage temperature range	– 55	+ 150	°C
T_{amb}	operating ambient temperature range	– 25	+ 65	°C
V_P	positive supply voltage (pin 8)	–	13.2	V
P_{tot}	total power dissipation	–	2.3	W

ESD

All pins meet:

2000 V, 100 pF, 1500 Ω

200 V, 200 pF, 0 Ω

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	30 K/W

CHARACTERISTICS

T_{amb} = 25 °C; supply 12 V; carrier 38.9 MHz negative modulation, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range (pin 8)		10	12	13.2	V
I_P	supply current (pin 8)	no input	90	115	140	mA
I_{12}	start current (pin 12)	note 1	–	6.5	9	mA
V_{12}	start protection level (pin 12)	I_{12} = 12 mA	–	–	16.5	V
IF Amplifier						
$V_{9\text{-}10(RMS)}$	input sensitivity (RMS–value)	note 2	25	40	65	μV
$R_{9\text{-}10}$	differential input resistance	note 3	–	1300	–	Ω
$C_{9\text{-}10}$	differential input capacitance	note 3	–	5	–	pF
$G_{9\text{-}10}$	gain control range		–	74	–	dB
ΔV_{20}	output signal expansion for 46 dB input signal variation	note 4	–	1	–	dB
$V_{9\text{-}10}$	maximum input signal		100	170	–	mV
$V_{9\text{-}10}$	input sensitivity at gain reduction	note 2	250	400	650	μV_{RMS}
Video Amplifier (note 5)						
	Zero signal output level	note 6				
V_{20}	negative modulation		4.7	4.9	5.1	V
V_{20}	positive modulation		2.5	2.7	2.9	V
V_{20}	sync tip (negative modulation)	note 7	2.5	2.7	2.9	V
V_{20}	white level (positive modulation)	note 7	4.5	4.7	4.9	V
V_{20}	white spot threshold level		–	5.5	–	V
V_{20}	white spot insertion level		–	4	–	V
Z_{20}	video output impedance		–	25	–	Ω
$I_{20(int)}$	internal bias current of NPN emitter follower output transistor		1.4	1.8	–	mA
I_{source}	maximum source current		10	–	–	mA
B	bandwidth of demodulated output signal		5	6	–	MHz
G_d	differential gain	note 8	–	2	5	%
φd	differential phase	note 8	–	2	5	°
NL	video non linearity	note 9	–	2	5	%
	intermodulation	note 10				
	1.1 MHz; blue		50	60	–	dB
	1.1 MHz; yellow		50	60	–	dB
	3.3 MHz; blue		55	65	–	dB
	3.3 MHz; yellow		55	65	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	note 11 see Fig.5				
	V_i = 10 mV input signal		52	57	–	dB
	end of gain control range		57	62	–	dB
V_{20}	residual carrier signal		–	2	10	mV
V_{20}	residual 2nd harmonic of carrier signal		–	2	10	mV
AGC						
I_{C11}	allowed leakage of the AGC capacitor		-	-	700	nA
System switch (note 13)						
	AGC on sync tip level for negative modulation signals					
V_{32}	control voltage		0	–	0.8	V
I_{32}	input current		–100	–	–500	µA
	AGC on white level for positive modulation signals					
V_{32}	control voltage		2	–	12	V
I_{32}	input current		0	–	1	mA
IF sync separator						
I_I	input current		0.4	0.6	0.8	mA
I_O	output current		22	27	32	µA
V_1	clamp level		–	3.3	–	V
Tuner AGC						
$V_{9\text{-}10\ (RMS)}$	minimum starting point for tuner take-over (RMS value)		–	–	0.2	mV
$V_{9\text{-}10(RMS)}$	maximum starting point for tuner take-over (RMS value)		100	150	–	mV
I_6	maximum tuner AGC output swing	V_6 = 3 V	4	–	–	mA
V_6	output saturation voltage	I_6 = 2 mA	–	–	300	mV
I_6	leakage current		–	–	1	µA
Δ	input signal variation complete tuner control	ΔI_6 = 2 mA	0.2	2	4	dB
V_2	minimum voltage tuner take-over		–	–	1	V
Video Switching Circuit (note 14)						
EXTERNAL POSITIVE VIDEO INPUT						
$V_{13(p\text{-}p)}$	input signal (peak-to-peak value)	$V_O = 2.5\ V_{(p\text{-}p)}$	–	1	–	V
I_{13}	input current		–	1.5	5	µA
V_{13}	sync tip clamping at 1 mA level		1.65	1.85	2.05	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INTERNAL VIDEO INPUT						
16(p-p)	Internal video input signal (peak-to-peak value)	V_O = 2.5 V (p-p)	–	2	–	V
I_{16}	input current		–	1.5	5	µA
V_{16}	noise clampling at 1 mA level		2.2	2.4	2.6	V
VIDEO OUTPUT (POSITIVE VIDEO)						
$V_{15(p-p)}$	positive video output signal (peak-to-peak value)		2.3	2.5	2.7	V
V_{15}	sync tip signal		–	3	–	V
I_{bias}	internal bias current		1	1.5	–	mA
I_O	maximum output current		5	–	–	mA
α	crosstalk external to internal	notes 12 and 15	–	55	–	dB
α	crosstalk internal to external	notes 12 and 15	–	55	–	dB
Video switch						
V_{18}	input voltage for internal video		–	–	0.8	V
V_{18}	input voltage for external video		2	–	V_P	V
I_{18}	maximum current	pin 18 = 0 V pin 18 = 12 V	– –	0.05 0.25	0.2 1	mA mA
AFC-circuit (note 16)						
I_{22}	AFC sample and hold switch-off current		0.1	–	–	mA
I_O	output current	V_{22} = 0 V	0.2	0.4	0.8	mA
I_{IL}	leakage current		–	–	1	µA
V_{21}	AFC output voltage swing		10.5	–	11.5	V
I_{21}	available output current		±0.2	–	–	mA
	control slope		–	100	–	mV/kHz
V_{21}	output voltage	AFC off	5.5	6	6.5	V
R_O	AFC output resistance	measured at an input signal amplitude of 150 µV(RMS)	–	40	–	kΩ
$V_{21(p-p)}$	output voltage swing	note 12	–	11	–	V
	control slope	note 12	–	80	–	mV/kHz
V_{21}	output voltage shift with respect to V_I = 10 $mV_{(RMS)}$	note 12	–	–2	–	V
AFC polarity switch						
I_{12}	sink current for negative slope		–	–	1	µA
I_{12}	sink current for positive slope		0.1	–	–	mA
I_{12}	maximum current	V_{12} = 0 V	–	–	1	mA
V_{12}	switching level		5	–	7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sync separator (see Fig.6)						
V_{28}	required sync pulse amplitude	note 17	200	750	–	mV
I_{28}	input current	V_{28} = 5 V V_{28} = 0 V	– –	8 –10	– –	µA mA
First control loop						
Δf_{RX}	PLL holding range		–	±1500	±2000	Hz
Δf_{XL}	PLL catching range		±600	±1500	–	Hz
	control sensitivity to oscillator	note 18	see Fig.7			
Second control loop (positive edge)						
Δtd/Δto	control sensitivity	note 19	–	100	–	
td	control range		–	25	–	µs
Phase adjustment (via second control loop)						
	control sensitivity		–	25	–	µA/µs
α	maximum allowed phase shift		–	±2	–	µs
Horizontal oscillator (note 19)						
f_{ft}	free running frequency	R = 34.3 kΩ C = 2.7 nF	–	15625	–	Hz
Δf_{osc}	spread with fixed external components		–	–	4	%
Δf_{osc}	frequency variations with supply voltage from 10 to 13.2 V		–	–	2	%
ΔfT	frequency variation with temperature	note 12	–	–1.6	–	Hz/K
Δf_{fr}	maximum frequency deviation at start of Horizontal output		–	–	10	%
Δf_{osc}	frequency variation when only noise is received	note 12	–	–	500	Hz
Horizontal output (open collector)						
V_{29}	output limiting voltage		–	–	16.5	V
V_{OL}	output voltage LOW	I_{sink} = 10 mA	–	0.3	0.5	V
I_{sink}	maximum sink current		10	–	–	mA
S	output signal duty factor		–	46	–	%
t_r	rise time output pulse		–	260	–	ns
t_f	fall times output pulse		–	100	–	ns
Flyback input and sandcastle output (note 22, Fig. 6)						
I_{30}	required input current during flyback pulse		0.1	–	2	mA
V_{30}	output voltage during burstkey horizontal blanking during vertical blanking		 8 4 2.1	 – 4.4 2.5	 – 5 2.9	 V V V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback input and sandcastle output (note 22, Fig. 6)						
t_W	pulse width burst key at: 60 Hz 50 Hz	 60 Hz 50 Hz	 2.9 3.2	 3.3 3.6	 3.7 4	 µs µs
	horizontal blanking		flyback pulse			
	vertical blanking					
T_1	divider in search window	50 Hz	–	21	–	lines
		60 Hz	–	17	–	lines
T_2	divider in narrow window	50 Hz	–	25	–	lines
		60 Hz	–	21	–	lines
	delay between the start of the sync pulse at the video output and the burst key pulse					
t_{Bkl}	trailing edge	60 Hz	–	–	9.4	µs
t_{Bkr}	rising edge		4.7	5.4	6.1	µs
VCR switch (non-VCR mode; V_{17} < 5 V)						
R_{17}	resistance to ground		–	–	5	kΩ
I_{17}	output current	pin 17 = 0 V	–	–	0.5	mA
VCR switch (auto-VCR mode)						
I_{17}	source current		–	–	30	µA
I_{17}	sink current		–	–	30	µA
VCR switch (VCR mode; V_{17} > 7 V)						
R_{17}	resistance to V_{CC}		–	–	5	kΩ
I_{17}	input current	$V_{17} = V_{CC}$	–	–	1	mA
$V_{9\text{-}10(rms)}$	IF input signal for switching from fast to slow in auto VCR mode (RMS value)		–	2.2	–	mV
Vertical ramp generator (note 21)						
I_3	input current during scan		–	–	2	µA
I_3	discharge current during retrace		–	0.8	–	mA
$V_{3(p\text{-}p)}$	sawtooth amplitude (peak-to-peak value)		–	1.9	–	V
t	interlace timing of the internal pulses	note 12	30	32	34	µs
Vertical output						
I_4	available output current	V_4 = 4 V	–	–	3	mA
V_4	maximum available output voltage	I_4 = 0.1 mA	4.4	5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical feedback input						
V_5	DC input voltage		2.9	3.3	3.7	V
$V_{5(p-p)}$	AC input voltage (peak-to-peak value)		–	1	–	V
I_5	input current		–	–	12	μA
Δ_{tp}	internal pre-correction to sawtooth		–	3	–	%
	deviation amplitude	50/60 Hz	–	–	2	%
	temperature dependency of the amplitude	note 12 ΔT = 45 °C	–	–	2	%
Vertical guard ($V_{pin\ 30}$ = 2.5 V)						
ΔV_5	active switch level at a deviation with respect to the DC feedback level	note 22				
	guard level LOW		–	1.5	–	V
	guard level HIGH		–	2	–	V
Coincidence detector/transmitter identification (note 23)						
V_{25}	voltage for in-sync condition		–	9.8	–	V
V_{25}	voltage for no-sync condition	no signal	–	0.3	–	V
V_{25}	switching level to switch the phase detector from fast to slow		6.2	6.7	7.2	V
V_{25}	hysteresis slow to fast		–	0.6	–	V
V_{25}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{25}	hysteresis mute function		–	2.5	–	V
Video transmitter identification output						
V_{14}	output voltage active	no sync; I = 1 mA	–	0.3	0.5	V
I_{14}	sink current active		–	–	5	mA
I_{14}	output current inactive (transmitter present)		–	–	1	μA
50/60 Hz identification (note 24)						
V_{14}	output voltage at 50 Hz		–	V_s	–	V
V_{14}	output voltage at 60 Hz		–	9	–	V

Notes to the Characteristics

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_p) is obtained from the horizontal output stage. The load current of the driver must be added to the value given above.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 μV.
5. Measured at 10 mV (RMS) 100% input signal.
6. Projected zero point; i.e. with switched demodulator.

7. The output signal amplitude is determined by the AGC detector. For negative modulation the sync tip level is used as reference. With positive modulation the white level is stabilized.
8. Measured according to the test line given in Fig.3.
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   - The differential phase is defined as the difference in degrees between the largest and smallest phase angle.
   - The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white to black). The non-linearity is expressed as a percentage of the maximum devatiation of a luminance step from the mean step, with respect to the mean step.
10. The test set-up and input conditions are given in Fig.5. The figures are measured at an input signal of 10 mV (RMS).
11. Measure with a source impedance of 75 Ω.

$$\textit{The signal-to-noise ratio} = 20 \log \frac{V_O \textit{ black-to-white}}{V_{n(RMS)} \textit{ at } B = 5 \textit{ MHz}}$$

12. These figures are based on sample tests.
13. By means of the system switch, two conditions can be obtained. Negative modulation with sync tip level AGC. This is obtained with pin 32 connected to ground. Positive modulation with peak white AGC. This is obtained with pin 32 connected to the positive supply.
14. When the video switch is in the external mode the first control loop in the synchronization circuit is not switched to a long time constant when weak signals are received.
15. Defined as $20 \log \frac{V_O \textit{ unwanted video black-to-white}}{V_O \textit{ wanted video-black-to-white}}$; measured at 4.4 MHz.
16. The indicated figures are measured at an input signal of 10 mV RMS. The unloaded Q-factor of the reference tuned circuit is 70.

    With very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has a asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built into the demodulator tuned circuit. The characteristics given for weak signals are measured without a notch circuit, with a SAW filter connected in front of the IC input signal such that the input signal of the IC is 150 µV (RMS value).
17. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
18. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 28) to $+V_P$. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to get a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head-errors of the VCR are compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.
19. This figure is valid for an external load impedance of 82 Ω from pin 31 to the shift adjustment potentiometer.
20. The flyback input and sandcastle output have been combined on one pin. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
21. The vertical scan is synchronized by means of a divider system. Therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.

22. To avoid CRT screen burn due to a collapse of the vertical deflection a continuous blanking level is inserted in the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
23. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin.
    The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 / µs) and the sync pulse in the internal video mode. When the circuit is in the external mode the capacitor is charged by the horizontal sync pulse and discharged continuously with a small current.
24. When the mute is active no 50/60 Hz information is available.

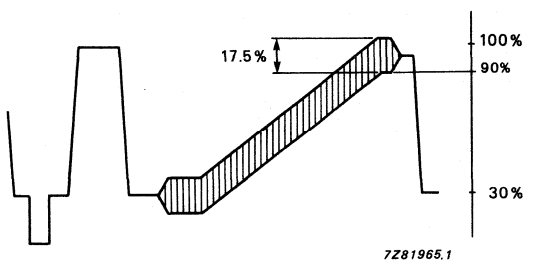


Fig.2 Video output signal.

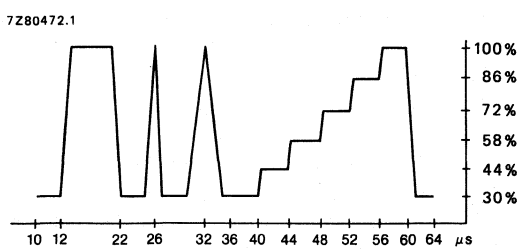
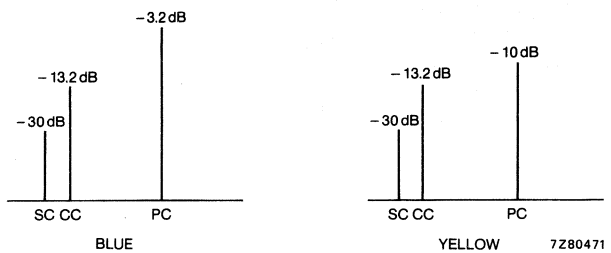
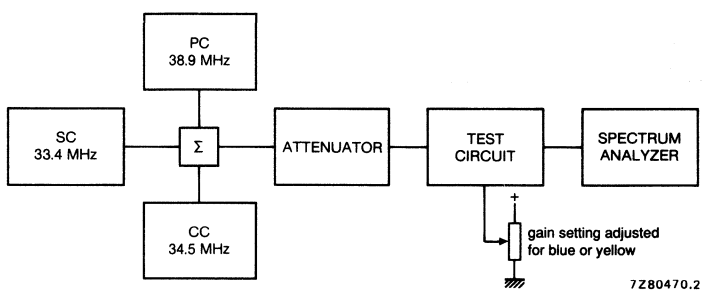


Fig.3 EBU test signal waveform (line 17).





Input signal conditons

SC = Sound carrier

CC = Chrominance carrier

PC = Picture carrier

All with respect to top sync level

$$\textit{Value at } 1.1\textit{MHz}: 20 \log \frac{V_o \textit{ at } 4.4\textit{MHz}}{V_o \textit{ at } 1.1\textit{MHz}} + 3.6\textit{dB}$$

$$\textit{Value at } 3.3\textit{MHz}: 20 \log \frac{V_o \textit{ at } 4.4\textit{MHz}}{V_o \textit{ at } 3.3\textit{MHz}}$$

Fig.4 Test set-up intermodulation.

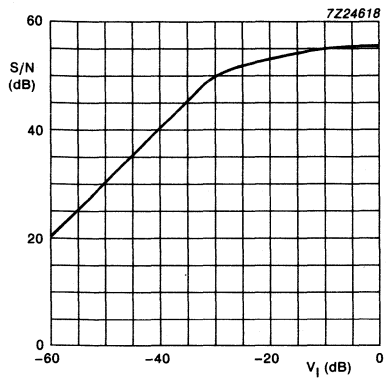
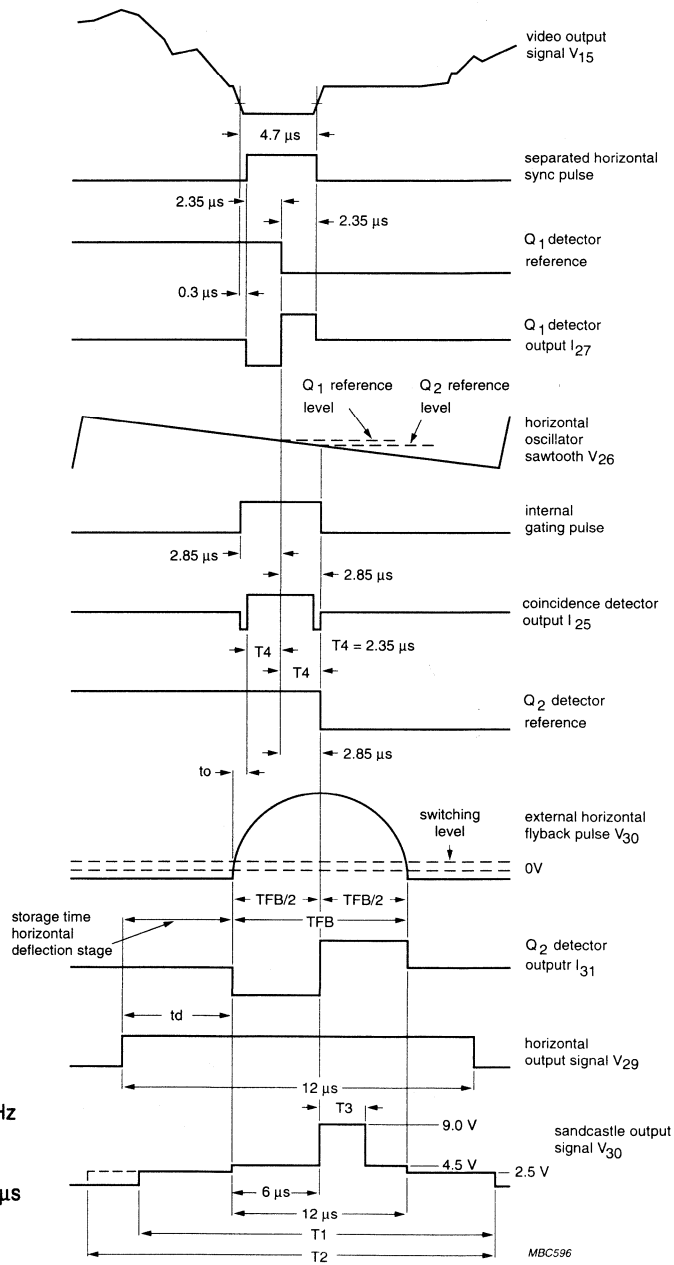


Fig.5 Signal-to noise ratio as a function of the input voltage (0 dB = 100 mV).



	50 Hz	60 Hz
T_1 - search window -	42 p	34 p
T_2 - narrow window -	50 p	42 p
T_3 - burst key pulse -	3.6 µs	3.3 µs

$(p = \frac{1}{2f_H})$

Fig.6 Timing diagram.

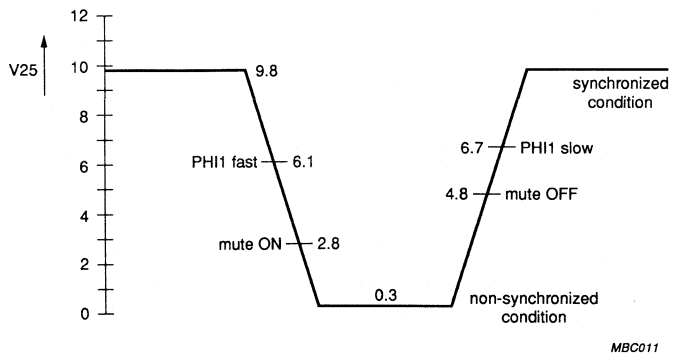


Fig.7 Switching levels coincidence detector.

COINCIDENCE DETECTOR SWITCHING LEVELS

CONDITION PIN 18 VIDEO SWITCH	CONDITION PIN 17 VCR SWITCH	CONDITION V_{25}	CONTROL SENSITIVITY HOR.OSCILLATOR kHz / µs	
			T2 – T1	T3 = SCAN
Low internal video	floating automatic VCR	V_{25} > 6.7 V and		
		strong signal	11.3	7.6
		weak signal	1.3	1.3
		V_{25} < 6.1 V and		
		strong signal	11.3	7.6
		weak signal	11.3	7.6
	HIGH forced VCR	don't care	11.3	7.6
	LOW T.V. mode	V_{25} > 6.7 V	1.3	1.3
		V_{25} < 6.1 V	11.3	7.6
HIGH or floating external video	don't care	don't care	11.3	7.6

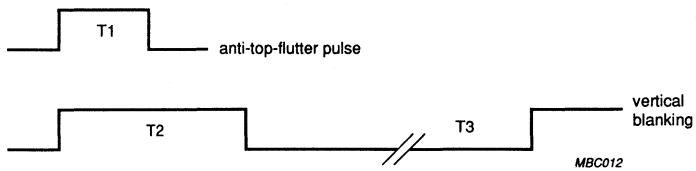


Fig.8 Horizontal oscillator control sensitivity.

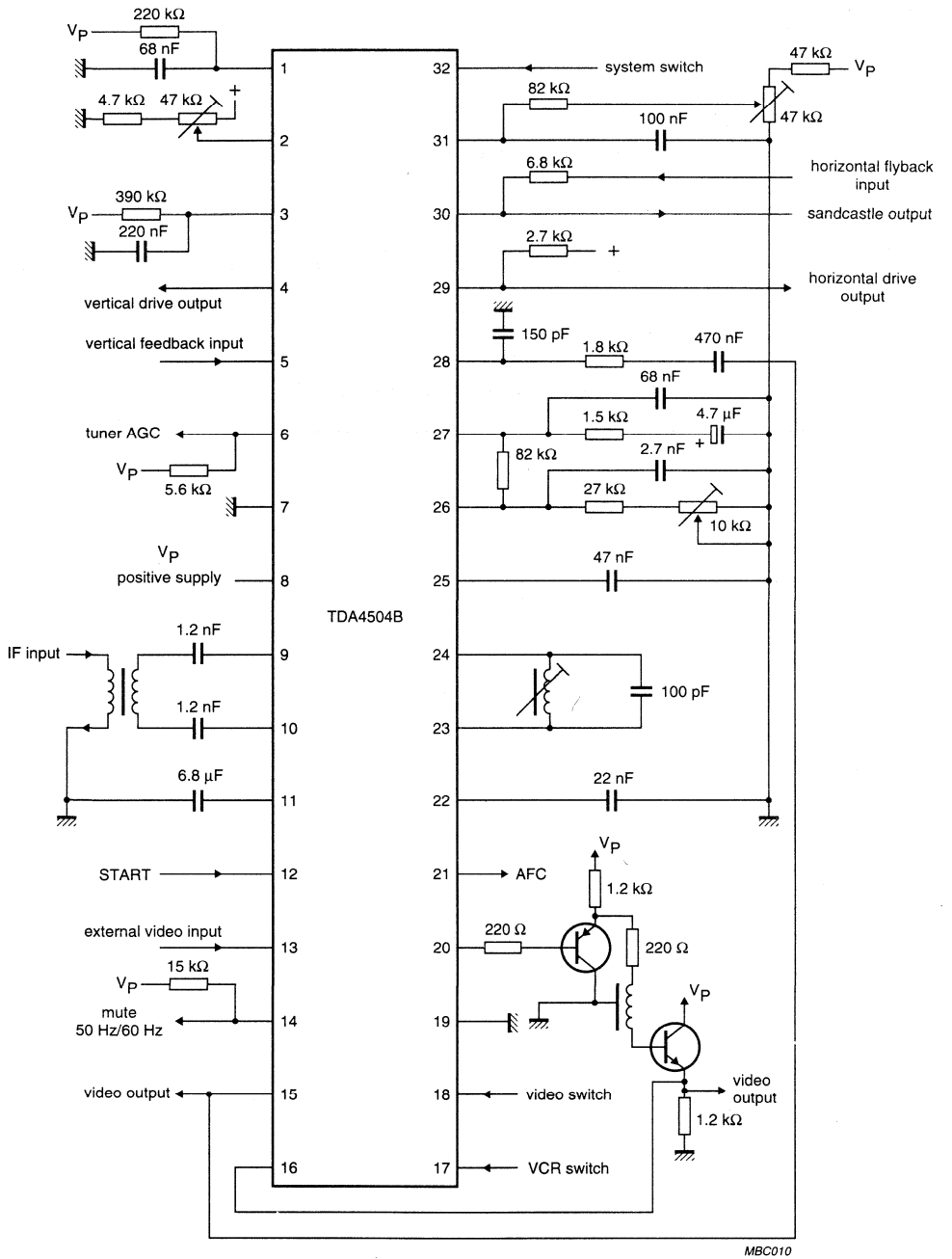


Fig.9 Application diagram.

PAL DECODER

The TDA4510 is a colour decoder for the PAL standard, which is pin sequent compatible with multi-standard decoder TDA4555 and also pin compatible with NTSC decoder TDA4570. It incorporates the following functions:

Chrominance part

- Gain controlled chrominance amplifier with operating point control stage
- Chrominance output stage for driving the 64 μs delay line
- Blanking circuit for the colour burst signal
- Automatic chrominance control (ACC) with sampled rectifier during burst-key

Oscillator and control voltage part

- Reference oscillator for double subcarrier frequency
- Gated phase comparison
- Identification demodulator and automatic colour killer
- Sandcastle pulse detector
- Service switch

Demodulator part

- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- PAL flip-flop and PAL switch
- Colour switching stages
- Separate colour switching output
- (B-Y) and (R-Y) signal output stages
- Internal filtering of residual carrier

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{7-3}$	typ.	12 V
Supply current	$I_P = I_7$	typ.	50 mA
Chrominance input signal (peak-to-peak)	$V_{9-3(p-p)}$		10 to 400 mV
Chrominance output signal (peak-to-peak)	$V_{6-3(p-p)}$	typ.	1,6 V
Colour difference output signals (peak-to-peak values)			
−(R-Y) signal	$V_{1-3(p-p)}$	typ.	1,05 V ± 2 dB
−(B-Y) signal	$V_{2-3(p-p)}$	typ.	1,33 V ± 2 dB
Sandcastle pulse, required amplitude for			
burst gating level	V_{15-3}	typ.	7,7 V
horizontal pulse separation	V_{15-3}	typ.	4,5 V
vertical and horizontal pulse separation	V_{15-3}	typ.	2,5 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

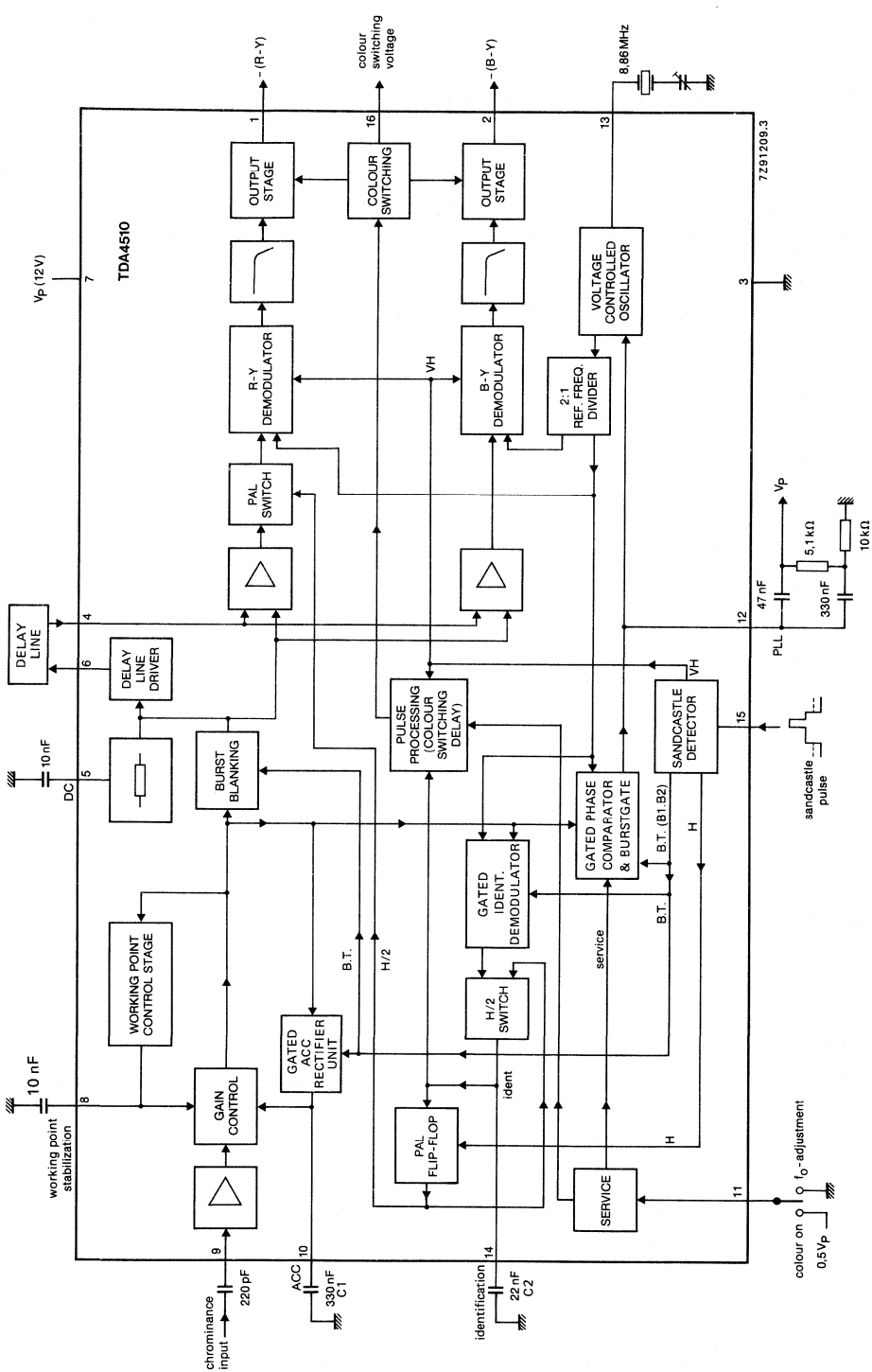


Fig. 1 Block diagram.

External capacitors in Fig. 1

C1 filter capacitor for control voltage (pin 10)

C2 filter capacitor for identification signal (pin 14)

FUNCTIONAL DESCRIPTION

DIVIDER STAGES

The divider stages provide −(R-Y) and −(B-Y) reference signals with the correct 90 degrees relation for the demodulators.

PHASE COMPARATOR

The phase comparator compares the −(R-Y) reference signal with the burst pulse and controls the frequency and phase of the reference oscillator.

IDENTIFICATION DEMODULATOR

The identification demodulator delivers a positive going identification signal for PAL-signals at pin 14, also used for the automatic colour-killer.

SERVICE SWITCH

The service switch has two functions. The first position ($V_{14-3} < 1$ V) allows the adjustment of the reference oscillator. Therefore the colour is switched on and the burst for the oscillator PLL is switched off. The second position ($V_{14-3} > 5$ V) switches the colour on and the output signals can be observed.

SANDCASTLE PULSE DETECTOR

Sandcastle pulse detector for burst-gate, line and blanking (horizontal and vertical) pulse detection. The vertical part of the sandcastle pulse is needed for the internal colour-on and colour-off delay.

PULSE PROCESSING PART

Pulse processing part which shall prevent a premature switching on of the colour. The colour-on delay, two or three field periods after identification of the PAL signal, is achieved by a counter. The colour is switched off immediately or at the latest one field period after disappearance of the identification voltage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{7-3}$	10,8 to 13,2		V
Currents				
at pins 1 and 2	$-I_{1,2}$	max.	5	mA
at pin 6	$-I_6$	max.	15	mA
at pin 16	$-I_{16}$	max.	5	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}	−25 to + 150		°C
Operating ambient temperature	T_{amb}	0 to + 70		°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 2 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current	I_7	–	50	–	mA
Chrominance part					
Input voltage range (peak-to-peak value)	$V_{9\text{-}3(p\text{-}p)}$	10	–	400	mV
Nominal input voltage (peak-to-peak value) with 75% colour bar signal	$V_{9\text{-}3(p\text{-}p)}$	–	100	–	mV
Input impedance	$Z_{9\text{-}3}$	–	3,3	–	kΩ
Input capacitance	$C_{9\text{-}3}$	–	4	–	pF
Colour ON					
Chrominance output voltage (peak-to-peak) with 75% colour bar signal	$V_{6\text{-}3(p\text{-}p)}$	–	1,6	–	V
d.c. voltage at chrominance output	$V_{6\text{-}3}$	–	8,2	–	V
Oscillator and control voltage part					
Oscillator frequency	f_o	–	8,8	–	MHz
Input resistance	$R_{13\text{-}3}$	–	350	–	Ω
Catching range (depending on RC-network at pin 12)	f	± 400	–	–	Hz
Control voltage					
without burst signal	$V_{14\text{-}3}$	–	6,0	–	V
colour on switching threshold	$V_{14\text{-}3}$	–	6,6	–	V
hysteresis of colour switching	$V_{14\text{-}3}$	–	150	–	mV
flip-flop correction (FFC) voltage	$V_{14\text{-}3}$	–	5,5	–	V
hysteresis of FFC	$V_{14\text{-}3}$	–	170	–	mV
Colour-on delay		2	–	3	f.p.*
Colour-off delay		0	–	1	f.p.*
First service position (PLL is inactive for oscillator adjustment, colour on)	$V_{11\text{-}3}$	0	–	1	V
second service position (colour on)	$V_{11\text{-}3}$	5	–	–	V
Colour switching output (open npn emitter)					
output current	$-I_{16}$	–	–	5	mA
colour-on voltage	$V_{16\text{-}3}$	–	6	–	V
colour-off voltage	$V_{16\text{-}3}$	–	0	–	V
Demodulator part					
Delayed chrominance input signal (peak-to-peak value) with 75% colour bar signal	$V_{4\text{-}3(p\text{-}p)}$	–	200	–	mV
Colour difference output signals (peak-to-peak value)					
–(R-Y) signal	$V_{1\text{-}3(p\text{-}p)}$	0,84	1,05	1,32	V
–(B-Y) signal	$V_{2\text{-}3(p\text{-}p)}$	1,06	1,33	1,67	V

parameter	symbol	min.	typ.	max.	unit
Ratio of colour difference output signals (R-Y)/(B-Y)	V_{1-3}/V_{2-3}	0,71	0,79	0,87	V
D.C. voltage at colour difference outputs	$V_{1;\,2-3}$	–	7,7	–	V
Residual carrier voltage at colour difference outputs					
1 x subcarrier frequency (4,4 MHz)	$V_{1,2-3(p-p)}$	–	–	20	mV
2 x subcarrier frequency (8,8 MHz)	$V_{1,2-3(p-p)}$	–	–	20	mV
Sandcastle pulse detector					
Thresholds:					
Field- and line-pulse separation pulse ON	V_{15-3}	1,3	1,6	1,9	V
Required pulse amplitude	V_{15-3}	2,0	2,5	3,0	V
Line pulse separation; pulse ON	V_{15-3}	3,3	3,6	3,9	V
Required pulse amplitude	V_{15-3}	4,1	4,5	4,9	V
Burst pulse separation; pulse ON	V_{15-3}	6,6	7,1	7,6	V
Required pulse amplitude	V_{15-3}	7,7	–	–	V
Input voltage during horizontal scanning	V_{15-3}	–	–	1,1	V
Input current	$-I_{15}$	–	–	100	μA

* f.p. is shortening for field periods in this case.

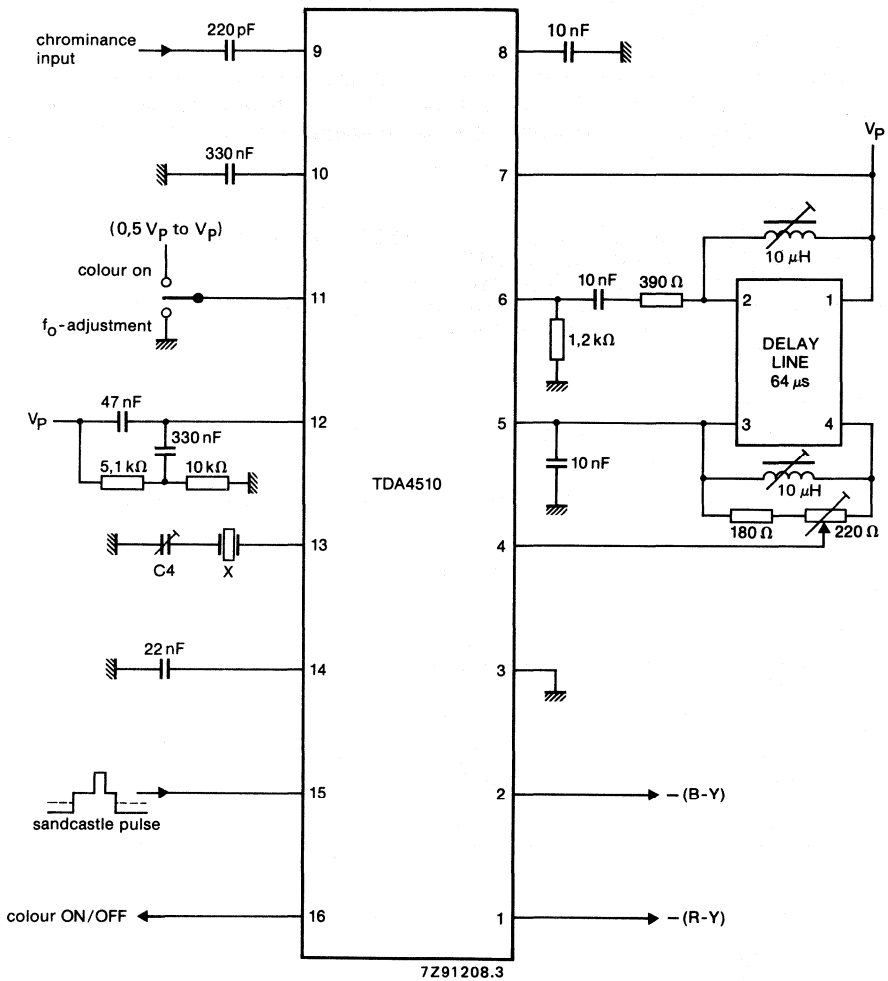


Fig. 2 Application information and test circuit.

C4 = 5 to 27 pF, X = 8,8 MHz; nominal frequency 8,867 238 MHz; resonance resistance 60 Ω, load capacitance 20 pF, dynamic capacitance 22 fF and static capacitance 5,5 pF.

MULTISTANDARD DECODER

GENERAL DESCRIPTION

The TDA4555 and TDA4556 are monolithic integrated multistandard colour decoders for the PAL, SECAM, NTSC 3,58 MHz and NTSC 4,43 MHz standards. The difference between the TDA4555 and the TDA4556 is the polarity of the colour difference output signals (B-Y) and (R-Y).

Features

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 μs glass delay line
- Chrominance output stage for driving the 64 μs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the two synchronous demodulators (PAL, NTSC)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)
- Insertion of reference voltages as achromatic value (SECAM) in the (B-Y) and (R-Y) colour difference output stages (blanking)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-9}$	typ.	12 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	65 mA
Chrominance input signal (peak-to-peak)	$V_{15-9(p-p)}$		20 to 200 mV
Chrominance output signal (peak-to-peak)	$V_{12-9(p-p)}$	typ.	1,6 V
Colour difference output signals (peak-to-peak values)			
TDA4555: –(R-Y); **TDA4556:** + (R-Y)	$V_{1-9(p-p)}$	typ.	1,05 V ± 2 dB
TDA4555: –(B-Y); **TDA4556:** + (B-Y)	$V_{3-9(p-p)}$	typ.	1,33 V ± 2 dB
Sandcastle pulse; required amplitude for			
vertical and horizontal pulse separation	V_{24-9}	typ.	2,5 V
horizontal pulse separation	V_{24-9}	typ.	4,5 V
burst gating	V_{24-9}	typ.	7,7 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

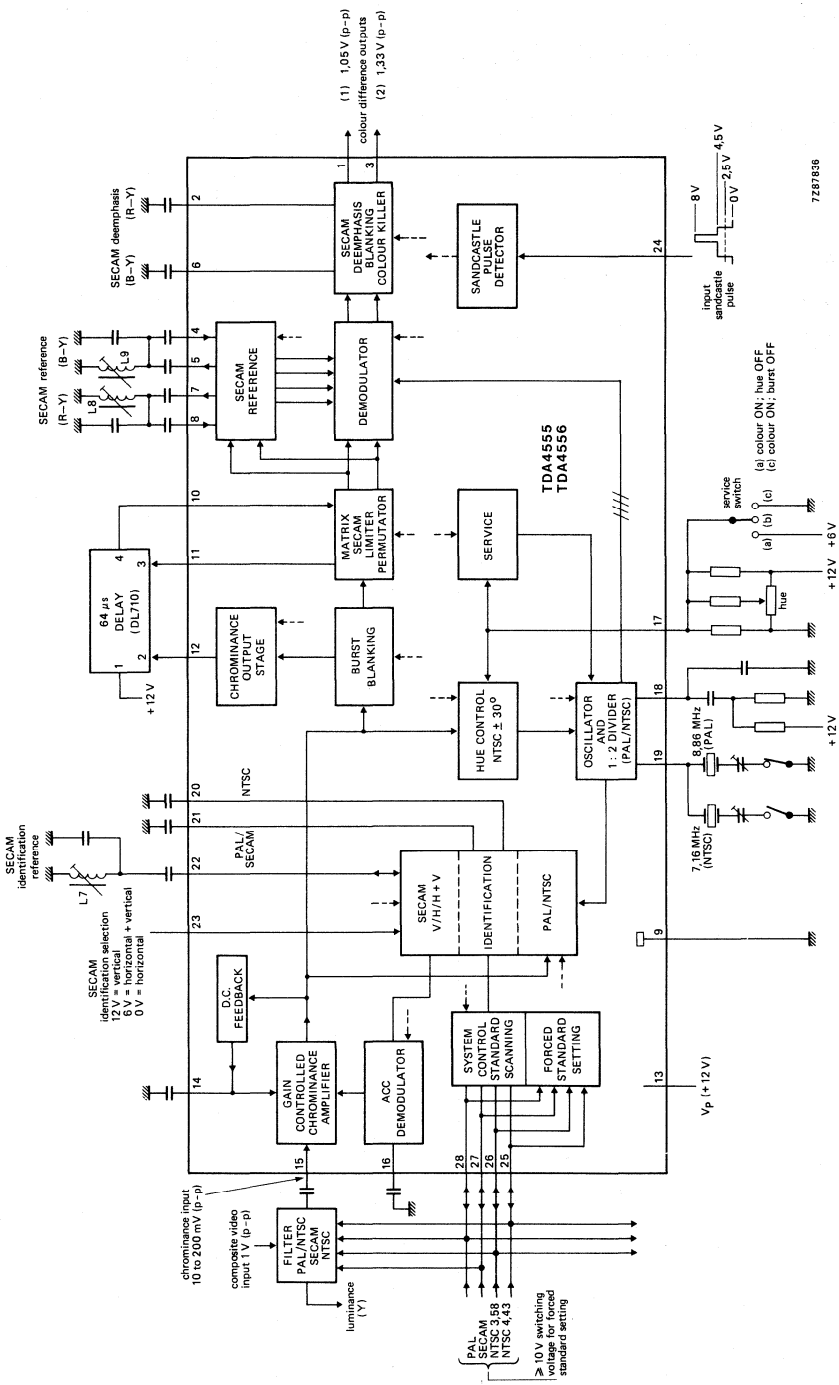


Fig. 1 Block diagram.

(1) TDA4555: —(R-Y); TDA4556: + (R-Y)
(2) TDA4555: —(B-Y); TDA4556: + (B-Y)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-9}$	max.	13,2 V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	V_{n-9}		0 to V_P V
Current at pin 12	I_{12}	max.	8 mA
Peak value	I_{12M}	max.	15 mA
Total power dissipation	P_{tot}	max.	1,4 W
Storage temperature range	T_{stg}		−25 to +150 °C
Operating ambient temperature range	T_{amb}		0 to +70 °C

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-9}$	10,8	–	13,2	V
Supply current	$I_P = I_{13}$	–	65	–	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15-9(p-p)}$	20	100	200	mV
input impedance	$\|Z_{15-9}\|$	2,3	3,3	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12-9(p-p)}$	–	1,6	–	V
output impedance (n-p-n emitter follower)	$\|Z_{12-9}\|$	–	–	20	Ω
d.c. output voltage	V_{12-9}	–	8,2	–	V
Input for delayed signal (pin 10)					
d.c. input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (proportional to V_{13-9}) (peak-to-peak value)					
TDA4555					
– (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33 V ± 2 dB	–	V
TDA4556					
+ (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05 V ± 2 dB	–	V
+ (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33 V ± 2 dB	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0,79 ± 10%	–	
Residual carrier (subcarrier frequency) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	–	30	mV
Residual carrier (PAL only) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	10	–	mV
H/2 ripple at (R-Y) output (pin 1) (peak-to-peak value) without input signal	$V_{1-9(p-p)}$	–	–	10	mV
D.C. output voltage					
n-p-n emitter follower with internal current source of 0,3 mA	$V_{1,3-9}$	–	7,7	–	V
output impedance	$\|Z_{1,3-9}\|$	–	–	150	Ω

parameter	symbol	min.	typ.	max.	unit
Demodulator part (SECAM)					
Colour difference signals (see note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value) TDA4555					
–(R-Y) signal (pin 1	$V_{1-9(p-p)}$	–	1,05	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
TDA4556					
+ (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05	–	V
+ (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0,79* ± 10%	–	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	20	30	mV
H/2 ripple at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3-9(p-p)}$	–	–	20	mV
D.C. output voltage	$V_{1,3-9}$	–	7,7	–	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T$(R-Y)	–	–0,55	–	mV/K
	$\Delta V/\Delta T$(B-Y)	–	+0,25	–	mV/K
HUE control (NTSC)/service switch					
Phase shift of reference carrier at V_{17-9} = 2 V	$-\phi$	–	30**	–	deg
at V_{17-9} = 3 V	ϕ	–	0	–	deg
at V_{17-9} = 4 V	$+\phi$	–	30**	–	deg
Input resistance	R_{17-9}	–	5	–	kΩ
Service position					
Switching voltage (pin 17) burst OFF; colour ON (for oscillator adjustment)	V_{17-9}	–	–	0,5	V
HUE control OFF; colour ON (for forced colour ON)	V_{17-9}	6	–	–	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency input resistance	R_{19-9}	–	350	–	Ω
lock-in-range referred to subcarrier frequency	Δf	± 400	–	–	Hz

* Value measured without influence of external circuitry.

** Relative to phase at V_{17-9} = 3 V.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification part					
Switching voltages for chrominance filters and crystals at pin 28 (PAL) at pin 27 (SECAM) at pin 26 (NTSC 3,58 MHz) at pin 25 (NTSC 4,43 MHz)					
Control voltage OFF state	$V_{25,26,27,28-9}$	–	–	0,5	V
Control voltage ON state					
during scanning; colour OFF	$V_{25,26,27,28-9}$	–	2,45	–	V
colour ON	$V_{25,26,27,28-9}$	–	5,8	–	V
Output current	$-I_{25,26,27,28-9}$	–	–	3	mA
Voltage for forced switching ON					
PAL	V_{28-9}	9	–	–	V
SECAM	V_{27-9}	9	–	–	V
NTSC 3,58 MHz	V_{26-9}	9	–	–	V
NTSC 4,43 MHz	V_{25-9}	9	–	–	V
Delay time for					
restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for					
horizontal identification (H)	V_{23-9}	–	–	2	V
vertical identification (V)	V_{23-9}	10	–	–	V
combined (H) and (V) identification	V_{23-9}	–	6*	–	V
Sequence of standard inquiry PAL-SECAM-NTSC 3,58 MHz-NTSC 4,43 MHz Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

* Or not connected.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (see note 2)					
Input voltage pulse levels (pin 24) to separate vertical and horizontal blanking pulses	$V_{24\text{-}9}$	1,2	–	2,0	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	2,0	–	3,0	V
to separate horizontal blanking pulse	$V_{24\text{-}9}$	3,2	–	4,0	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	4,0	–	5,0	V
to separate burst gating pulse	$V_{24\text{-}9}$	6,5	–	7,7	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	7,7	–	V_P	V
Input voltage during horizontal scanning	$V_{24\text{-}9}$	–	–	1,0	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference signals (R-Y) and B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

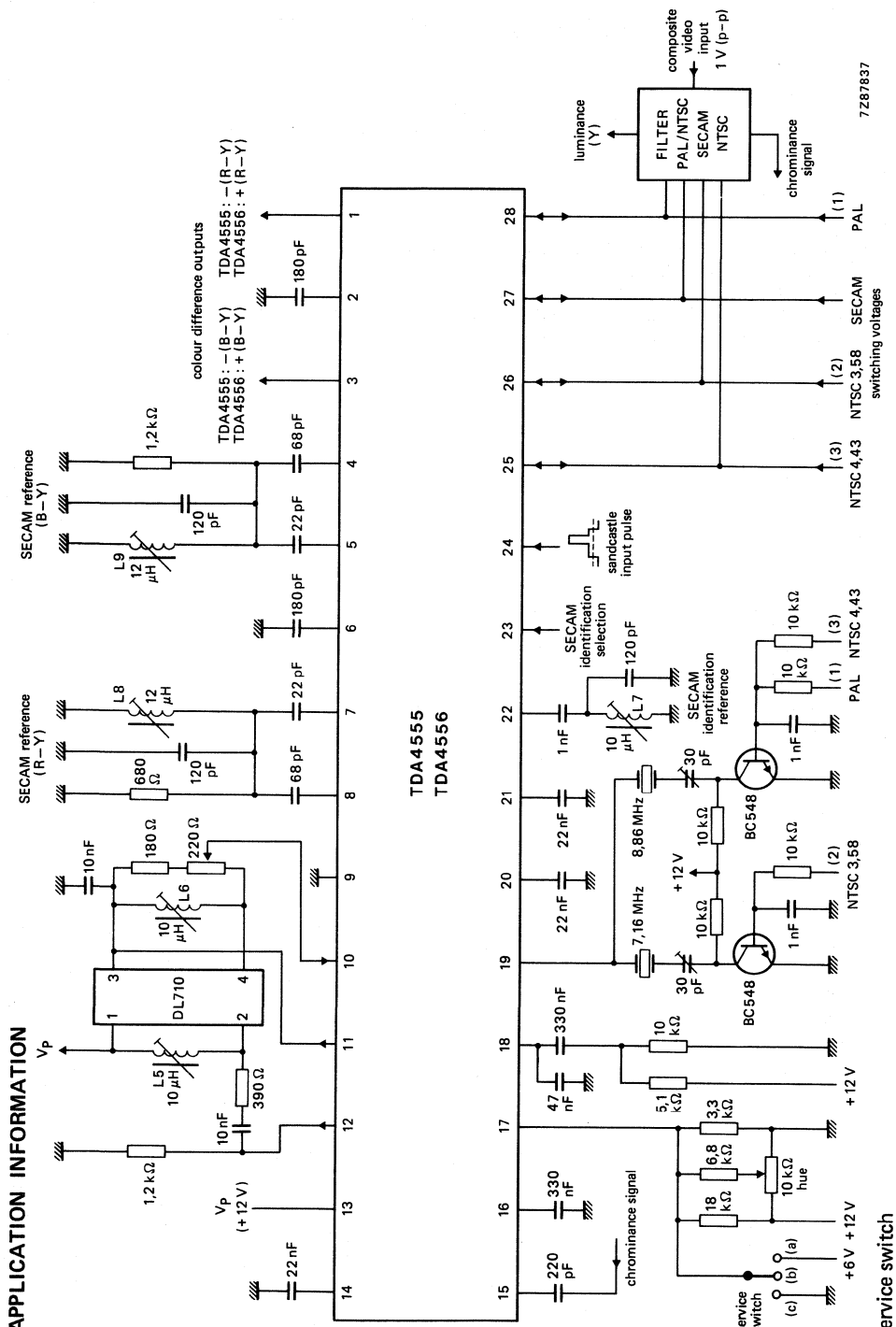


Fig. 2 Application diagram.

MULTISTANDARD DECODER

GENERAL DESCRIPTION

The TDA4557 is a monolithic integrated multistandard colour decoder for the PAL, SECAM, NTSC 3.58 MHz and NTSC 4.43 MHz standards.

Features

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 μs glass delay line
- Chrominance output stage for driving the 64 μs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the demodulators (PAL, NTSC, SECAM)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit and 50/60 Hz recognition
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_P	10.8	12.0	13.2	V
Supply current (pin 13)	I_P	–	65	–	mA
Chrominance input voltage (peak-to-peak value)	$V_{15(p-p)}$	20	100	400	mV
Chrominance output voltage (peak-to-peak value)	$V_{12(p-p)}$	–	1.6	–	V
Colour difference output voltages (peak-to-peak values)					
–(R-Y)	$V_{1(p-p)}$	–	1.05 V ± 2 dB	–	V
–(B-Y)	$V_{3(p-p)}$	–	1.33 V ± 2 dB	–	V
Sandcastle pulse (pin 24)					
Required amplitude to separate vertical and horizontal pulse	$V_{24(p-p)}$	2.0	2.5	3.0	V
horizontal pulse	$V_{24(p-p)}$	4.1	4.5	4.9	V
burst gating pulse	$V_{24(p-p)}$	7.7	–	V_P	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

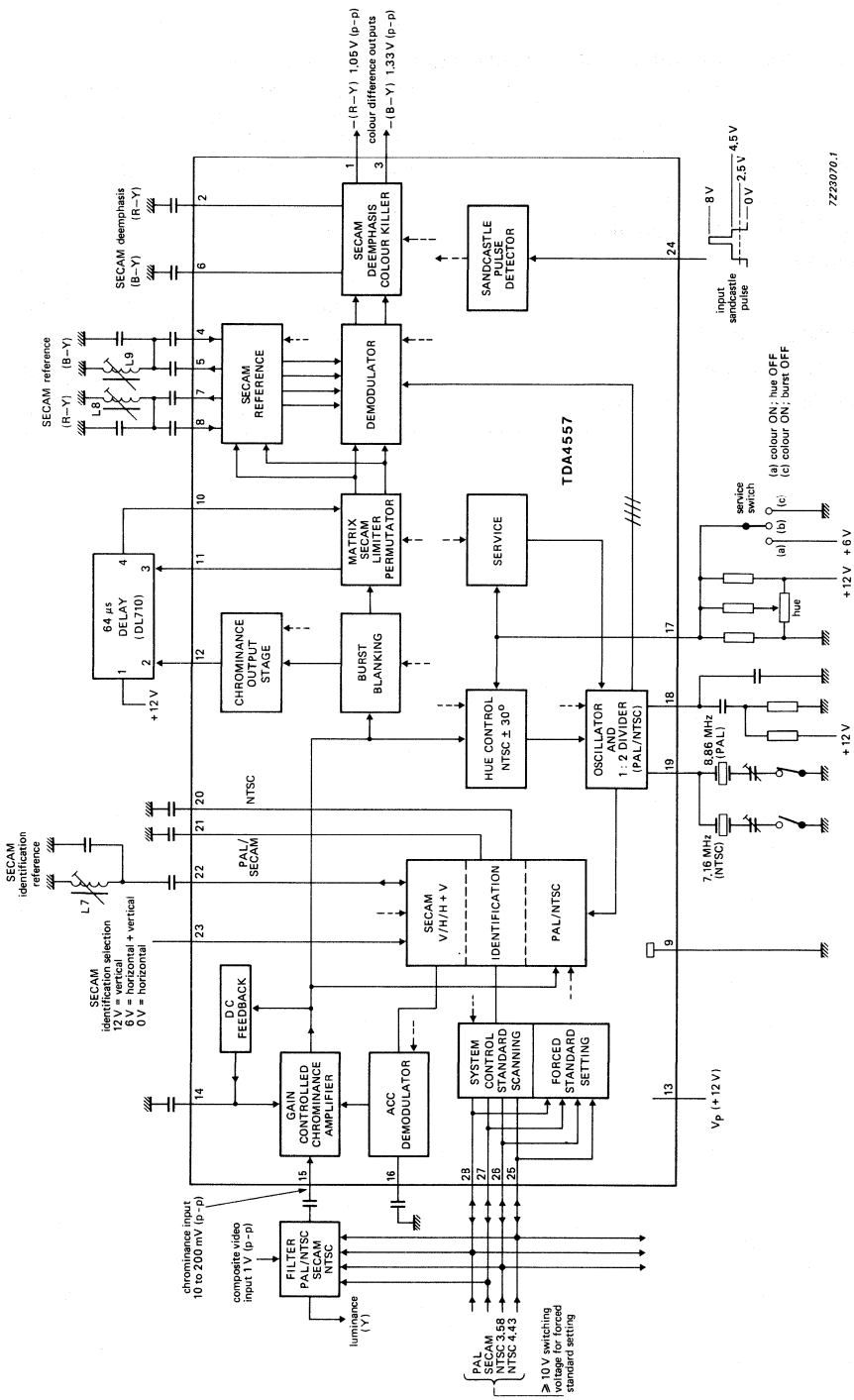


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 13)	V_P	–	13.2	V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	$V_{n\text{-}9}$	0	V_P	V
Current at pin 12	I_{12}	–	8	mA
Peak value	I_{12M}	–	15	mA
Total power dissipation	P_{tot}	–	1.4	W
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	V_P	10.8	1.2	13.2	V
Supply current	I_P	50	65	80	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15(p-p)}$	20	100	400	mV
input impedance	$\|Z_{15-9}\|$	7	10	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12(p-p)}$	1.1	1.6	1.75	V
output impedance (npn emitter follower)	$\|Z_{12-9}\|$	–	–	20	Ω
DC output voltage	V_{12-9}	7.3	8.2	9.0	V
Input for delayed signal (pin 10)					
DC input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (proportional to V_{13-9}) (peak-to-peak value)					
– (R-Y) signal (pin 1)	$V_{1(p-p)}$	–	1.05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3(p-p)}$	–	1.33 V ± 2 dB	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0.79 ± 10%	–	
Residual carrier (subcarrier frequency) (peak-to-peak value)	$V_{1,3(p-p)}$	–	–	30	mV
Residual carrier (PAL only) (peak-to-peak value)	$V_{1,3(p-p)}$	–	10	–	mV
H/2 ripple at (R-Y) output (pin 1) (peak-to-peak value) without input signal	$V_{1(p-p)}$	–	–	10	mV
DC output voltage					
npn emitter follower with internal current source of 0.3 mA	$V_{1,3-9}$	7.0	7.7	8.4	V
output impedance	$\|Z_{1,3-9}\|$	–	–	150	Ω

parameter	symbol	min.	typ.	max.	unit
Demodulator part (SECAM)					
Colour difference signals (see note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value)					
–(R-Y) signal (pin 1	$V_{1(p-p)}$	–	1.05	–	V
– (B-Y) signal (pin 3)	$V_{3(p-p)}$	–	1.33	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0.79* ± 10%	–	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,3(p-p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,3(p-p)}$	–	20	30	mV
H/2 ripple at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3(p-p)}$	–	–	30	mV
DC output voltage	$V_{1,3-9}$	7.0	7.7	8.4	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T(R-Y)$	–	0.5	0.6	mV/K
	$\Delta V/\Delta V_P$	–	8	–	mV/V
HUE control (NTSC)/service switch					
Phase shift of reference carrier at V_{17-9} = 2 V	$-\phi$	30	40	–	deg
at V_{17-9} = 3 V	ϕ	–	0	–	deg
at V_{17-9} = 4 V	$+\phi$	30	40	–	deg
Input resistance	R_{17-9}	–	5	–	kΩ
Service position					
Switching voltage (pin 17) burst OFF; colour ON (for oscillator adjustment)	V_{17-9}	0	–	0.5	V
HUE control OFF; colour ON (for forced colour ON)	V_{17-9}	6	–	V_P	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency input resistance	R_{19-9}	–	350	–	Ω
lock-in-range referred to subcarrier frequency	Δf	± 400	–	–	Hz

* Value measured without influence of external circuitry.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification part					
Switching voltages for chrominance filters and crystals at pin 28 (PAL) at pin 27 (SECAM) at pin 26 (NTSC 3.58 MHz) at pin 25 (NTSC 4.43 MHz)					
Control voltage OFF state	$V_{25,26,27,28-9}$	–	–	0.5	V
Control voltage ON state					
during scanning; colour OFF	$V_{25,26,27,28-9}$	2.1	2.45	2.7	V
colour ON	$V_{25,26,27,28-9}$	5.5	5.8	6.2	V
Output current	$-I_{25,26,27,28-9}$	–	–	3	mA
Voltage for forced switching ON					
PAL	V_{28-9}	9	–	V_P	V
SECAM	V_{27-9}	9	–	V_P	V
NTSC 3.58 MHz	V_{26-9}	9	–	V_P	V
NTSC 4.43 MHz	V_{25-9}	9	–	V_P	V
Delay time for					
restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for					
horizontal identification (H)	V_{23-9}	0	–	2	V
vertical identification (V)	V_{23-9}	10	–	V_P	V
combined (H) and (V) identification	V_{23-9}	–	6*	–	V
Sequence of standard inquiry PAL-SECAM-NTSC 3.58 MHz-NTSC 4.43 MHz					
Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

* Or not connected.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (see note 2)					
Input voltage pulse levels (pin 24) to separate vertical and horizontal blanking pulses	$V_{24\text{-}9}$	1.3	1.6	1.9	V
required pulse amplitude	$V_{24(p\text{-}p)}$	2.0	2.5	3.0	V
to separate horizontal blanking pulse	$V_{24\text{-}9}$	3.3	3.6	3.9	V
required pulse amplitude	$V_{24(p\text{-}p)}$	4.1	4.5	4.9	V
to separate burst gating pulse	$V_{24\text{-}9}$	6.6	7.1	7.6	V
required pulse amplitude	$V_{24(p\text{-}p)}$	7.7	–	V_P	V
Input voltage during horizontal scanning	$V_{24\text{-}9}$	–	–	1.0	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference signals (R-Y) and B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

APPLICATION INFORMATION

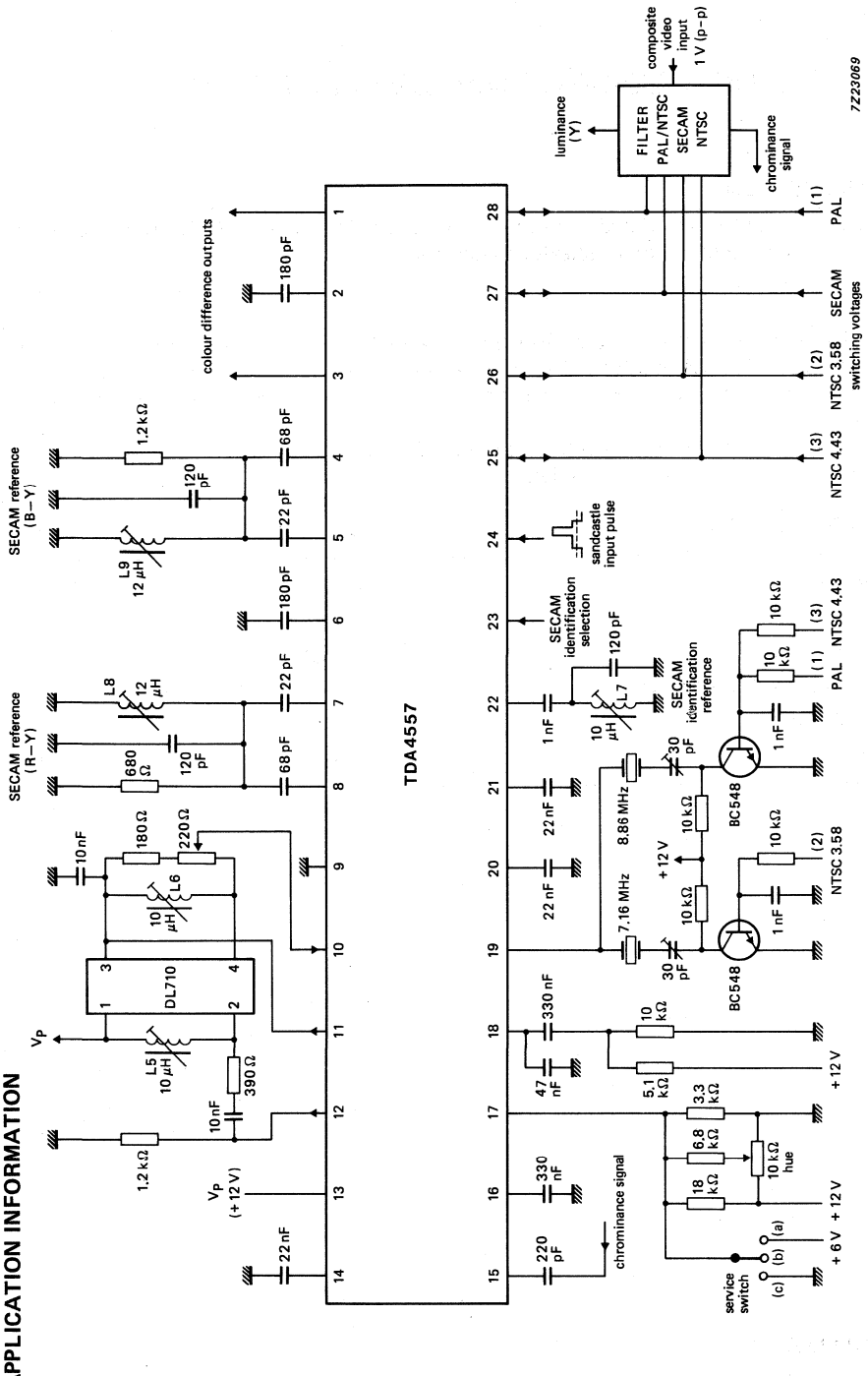


Fig. 2 Application diagram.

Service switch

(a) colour ON; hue OFF
(c) colour ON; burst OFF

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4560 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 720 ns to 1035 ns in steps of 45 ns
- Output for the option of velocity modulation

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10\text{-}18}$	typ.	12	V
Supply current (pin 10)	$I_P = I_{10}$	typ.	35	mA
(R-Y) and (B-Y) attenuation	α_{cd}	typ.	0	dB
(R-Y) and (B-Y) output transient time	t_{tr}	typ.	150	ns
Adjustable Y-delay time	t_d	720 to	1035	ns
Y-attenuation	α_y	typ.	7	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

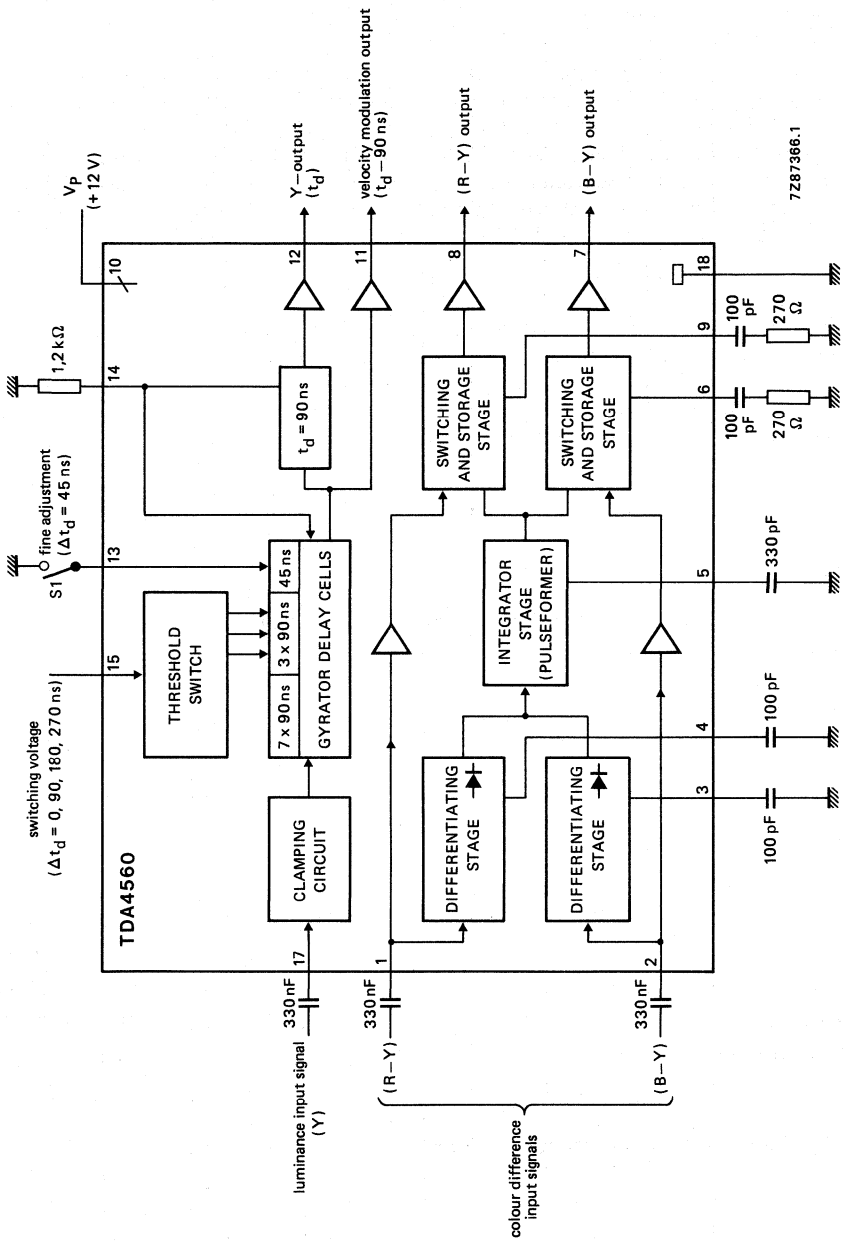


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The IC consists of two colour difference channels (B-Y) and (R-Y) and a luminance signal path (Y) as shown in Fig. 1.

Colour difference channels

The (B-Y) and (R-Y) colour difference channels consist of a buffer amplifier at the input, a switching stage and an output amplifier. The switching stages, which are controlled by transient detecting stages (differentiators), switch to a value that has been stored at the beginning of the transients. The differentiating stages get their signal direct from the colour difference detecting signal (pins 1 and 2). Two parallel storage stages are incorporated in which the colour difference signals are stored during the transient time of the signal. After a time of about 600 ns they are switched immediately (transient time of 150 ns) to the outputs. The colour difference channels are not attenuated.

Y-signal path

The Y-signal input (pin 17) is capacitively coupled to an input clamping circuit. Gyrator delay cells provide a maximum delay of 1035 ns including an additional delay of 45 ns via the fine adjustment switch (S1) at pin 13. Three delay cells are switched with two interstage switches dependent on the voltage at pin 15. Thus three switchable delay times of 90 ns, 180 ns or 270 ns less than the maximum delay time are available. A tuning compensation circuit ensures accuracy of delay time despite process tolerances. The Y-signal path has a 7 dB attenuation as a normal Y-delay coil and can replace this completely. The output is fed to pin 12 via a buffer amplifier. An additional output stage provides a signal of 90 ns less delay at pin 11 for the option of velocity modulation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC)

Supply voltage (pin 10)	$V_P = V_{10-18}$	max. 13,2	V
Voltage ranges to pin 18 (ground)			
at pins 1,2,12,15	V_{n-18}	0 to V_P	V
at pin 11	V_{11-18}	0 to (V_P–3V)	V
at pin 17	V_{17-18}	0 to 7	V
Voltage ranges			
at pin 7 to pin 6	V_{7-6}	0 to 5	V
at pin 8 to pin 9	V_{8-9}	0 to 5	V
Currents			
at pins 6,9	$\pm I_{6,9}$	max. 15	mA
at I_7, I_8, I_{11}, I_{12}		internally limited	
Total power dissipation	P_{tot}	max. 1,1	W
Storage temperature range	T_{stg}	–25 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

Note

Pins 3, 4, 5, 6, 9, 13 and 14 d.c. potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage	$V_P = V_{10-18}$	10,8	12	13,2	V
Supply current	$I_P = I_{10}$	–	35	50	mA
Colour difference channels (pins 1 and 2);					
(R-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{1-18}	–	1,05	–	V
(B-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{2-18}	–	1,33	–	V
Input resistance	$R_{1,\,2-18}$	–	12	–	kΩ
Internal bias (input)	$V_{1,\,2-18}$	–	4,3	–	V
(B-Y), (R-Y) signal attenuation $\frac{V_8}{V_1}, \frac{V_7}{V_2}$	α_{cd}	–	0	–	dB
Output voltage (d.c.)	$V_{7,\,8-18}$	–	4,4	–	V
Output current (emitter follower with constant current source 0,65 mA)	$-I_{7,8}$	–	1,2	–	mA
(R-Y) and B-Y) output signal transient time	t_{tr}	–	150	–	ns
Y-signal path (pin 17)					
Y-input voltage (composite signal) (peak-to-peak value)	$V_{17-18(p-p)}$	–	1	–	V
Internal bias voltage (during clamping)	V_{17-18}	–	1,5	–	V
Input current during picture content	I_{17}	–	8	–	μA
during synchronizing pulse	$-I_{17}$	–	100	–	μA
Y-signal attenuation $\frac{V_{11}}{V_{17}}$	α_Y	–	8	–	dB
Y-signal attenuation $\frac{V_{12}}{V_{17}}$	α_Y	–	7	–	dB
Output voltage (d.c.)	V_{11-18}	–	2,3	–	V
Output voltage (d.c.)	V_{12-18}	–	10,3	–	V
Output current (emitter follower with constant current source 0,45 mA)	$-I_{11,12}$	–	1,2	–	mA
Frequency response (note 1) $R_{14-18} = 1{,}2$ kΩ; $V_{15-18} = 12$ V	f_{12-17}	–	5	–	MHz

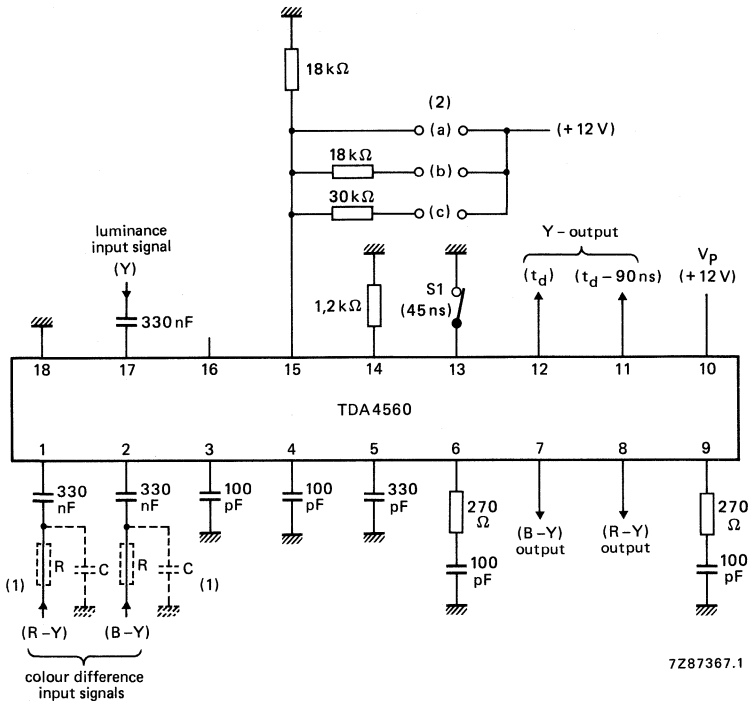
CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Y-signal path (pin 17)					
Adjustable delay (note 2) (switch open)					
at $V_{15\text{-}18}$ = 0 to 2,5 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	720	–	ns
at $V_{15\text{-}18}$ = 3,5 to 5,5 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	810	–	ns
at $V_{15\text{-}18}$ = 6,5 to 8,5 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	900	–	ns
at $V_{15\text{-}18}$ = 9,5 to 12 V; $R_{14\text{-}18}$ = 1,2 kΩ	t_d	–	990	–	ns
Fine adjustment delay (switch S1 closed)					
at $V_{13\text{-}18}$ = 0 V	Δt_d	–	45	–	ns
Signal delay for velocity modulation (pin 11)	t		t_d – 90 ns		
Thermal resistance					
From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	–	–	70	K/W

NOTES TO THE CHARACTERISTICS

1. $R_{14\text{-}18}$ influences the bandwidth.
2. Delay time is proportional to resistor $R_{14\text{-}18}$.

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.

Fig. 2 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
O	O	O	0 to 2,5 V	720
O	O	X	3,5 to 5,5 V	810
O	X	X	6,5 to 8,5 V	900
X	X	X	9,5 to 12 V	990

Where: X = connection closed; O = connection open.

* When switch (S1) is closed the delay time is increased by 45 ns.

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4565 is a monolithic integrated circuit for coulour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 730 ns to 1000 ns in steps of 90 ns and additional fine adjustment of 50 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	35	50	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	760	820	880	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	850	910	970	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	940	1000	1060	ns
Y-signal attenuation	0.5 MHz	α_Y	0	6.5	8.0	dB
(R-Y) and (B-Y) signal attenuation		α_{cd}	−1	0	+1	dB
output transient time		t_{tr}	–	100	200	ns

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

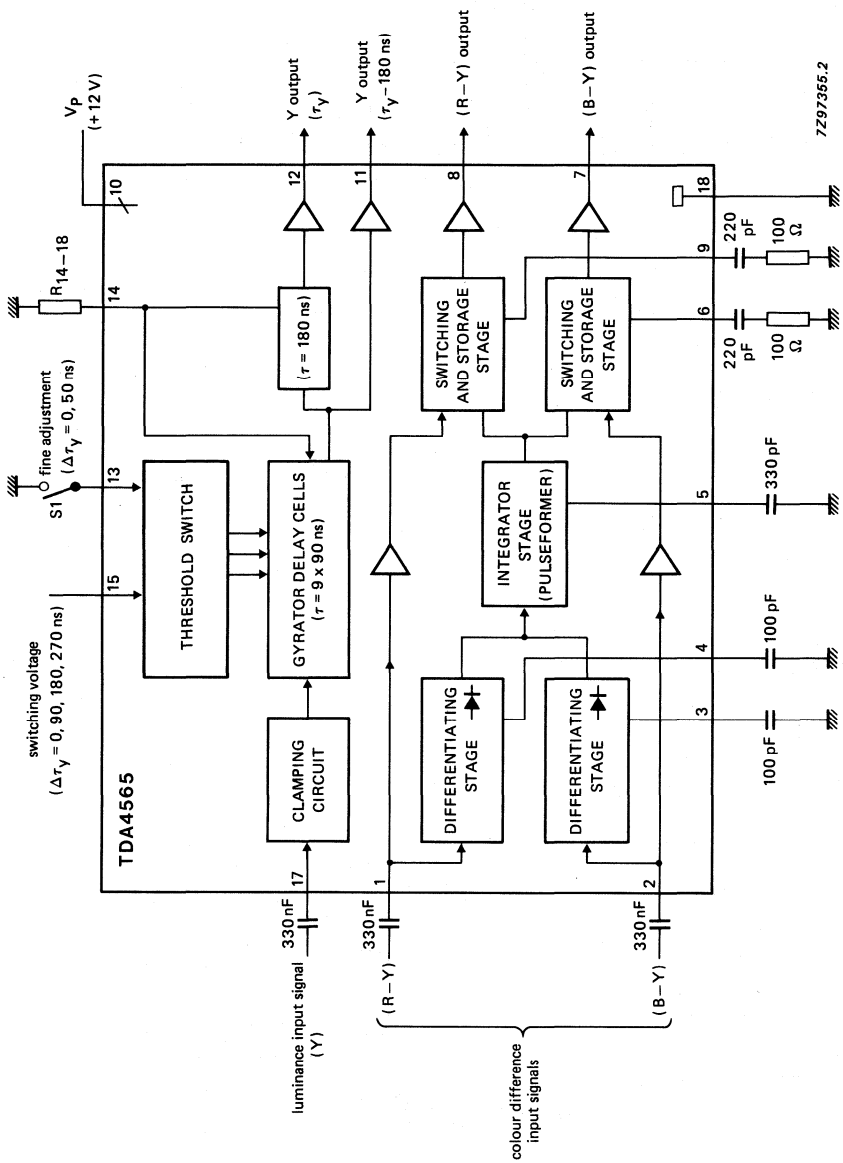


Fig.1 Block diagram.

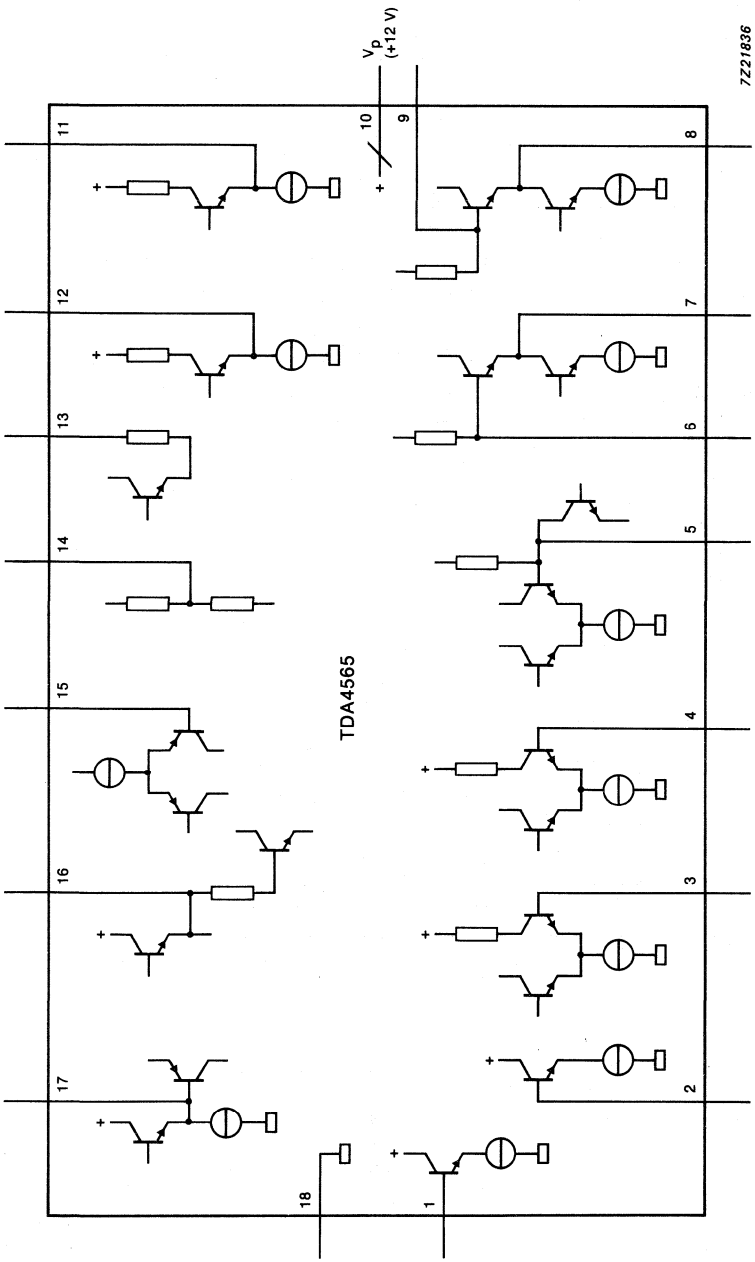


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_P = V_{10-18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12 and 15	V_{n-18}	0	V_p	V
at pin 11	V_{11-18}	0	$(V_p - 3\ V)$	V
at pin 17	V_{17-18}	0	7	V
Voltage ranges				
at pin 7 to pin 6	V_{7-6}	0	5	V
at pin 8 to pin 9	V_{8-9}	0	5	V
Currents				
at pins 6, 9	$I_{6, 9}$	−10	+10	mA
at pins 7, 8, 11 and 12	$I_{7, 8, 11, 12}$	internally limited		
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	−	1.1	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j-a}$ = 70 K/W

Note

Pins 3, 4, 5, 6, 9, 13 and 14 DC potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_P	10.8	12	13.2	V
Supply current		I_P	–	35	50	mA
Colour difference paths						
(R-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{1(p-p)}$	–	1.05	1.5	V
(B-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{2(p-p)}$	–	1.33	1.9	V
Input resistance						
(R-Y)		R_{1-18}	8	12	16	kΩ
(B-Y)		R_{2-18}	8	12	16	kΩ
Internal bias voltage						
(R-Y)		V_{1-18}	3.8	4.3	4.8	V
(B-Y)		V_{1-18}	3.8	4.3	4.8	V
Signal attenuation						
(R-Y)		V_8/V_1	−1	0	+1	dB
(B-Y)		V_7/V_2	−1	0	+1	dB
Output transient time	note 1	t_{tr}	–	100	200	ns
Output resistance						
(B-Y)		R_{7-18}	–	100	–	Ω
(R-Y)		R_{8-18}	–	100	–	Ω
DC output voltage						
(B-Y)		V_{7-18}	3.8	4.3	4.8	V
(R-Y)		V_{8-18}	3.8	4.3	4.8	V
Output current	note 2					
source		$I_{7,8}$	0.4	–	–	mA
sink		$-I_{7,8}$	1.0	–	–	mA

CHARACTERISTICS (continued)

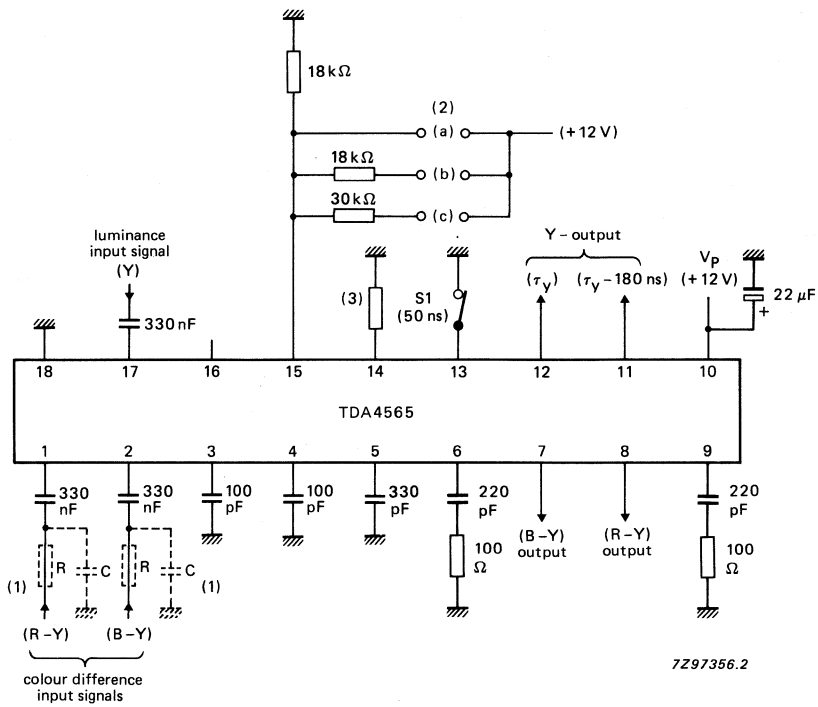
parameter	conditions	symbol	min.	typ.	max.	unit
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p\text{-}p)}$	–	1	1.4	V
Internal bias voltage	during clamping	$V_{17\text{-}18}$	1.3	1.5	1.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; R_{14} = 1.2 kΩ; notes 3 and 4)					
at $V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}18}$	670	730	790	ns
at $V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}18}$	760	820	880	ns
at $V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}18}$	850	910	970	ns
at $V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}18}$	940	1000	1060	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	$t_{17\text{-}12}$	30	50	70	ns
Signal delay between pin 11 and pin 12	S1 open	$t_{11\text{-}12}$	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17\text{-}12}}{t_{17\text{-}12}.\Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17\text{-}12}}{t_{17\text{-}12}.\Delta V_p}$	–	–0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	5.0	6.5	8.0	dB
pin 12 from pin 17		V_{12}/V_{17}	5.0	6.5	8.0	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB
Frequency response at 5 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	–3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz}{V_{12}\ (0.5\ MHz)}$	–3.0	–	2.0	dB

parameter	conditions	symbol	min.	typ.	max.	unit
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 2					
source		$I_{11, 12}$	–	–	0.4	mA
sink		$-I_{11, 12}$	–	–	1.0	mA

Notes to the characteristics

1. Output signal transient time measured with $C_{6\text{-}18} = C_{9\text{-}18} = 220$ pF without resistor (see Fig.3).
2. Output current measured with emitter follower with constant current source of 0.6 mA.
3. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
4. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18} = 1.2$ kΩ.
5. Frequency response measured with $V_{15\text{-}18} = 9.5$ V and switch S1 open.

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.
(3) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4565
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4565A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	730
0	0	X	3.5 to 5.5 V	820
0	X	X	6.5 to 8.5 V	910
X	X	X	9.5 to 12 V	1000

Where: X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 50 ns.

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4566 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 550 ns to 820 ns in steps of 90 ns and additional fine adjustment of 37 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	35	50	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	490	550	610	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	580	640	700	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	760	820	880	ns
Y-signal amplification	0.5 MHz	α_Y	0	1	2	dB
(R-Y) and (B-Y) signal attenuation		α_{cd}	−1	0	+ 1	dB
output transient time		t_{tr}	–	100	200	ns

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

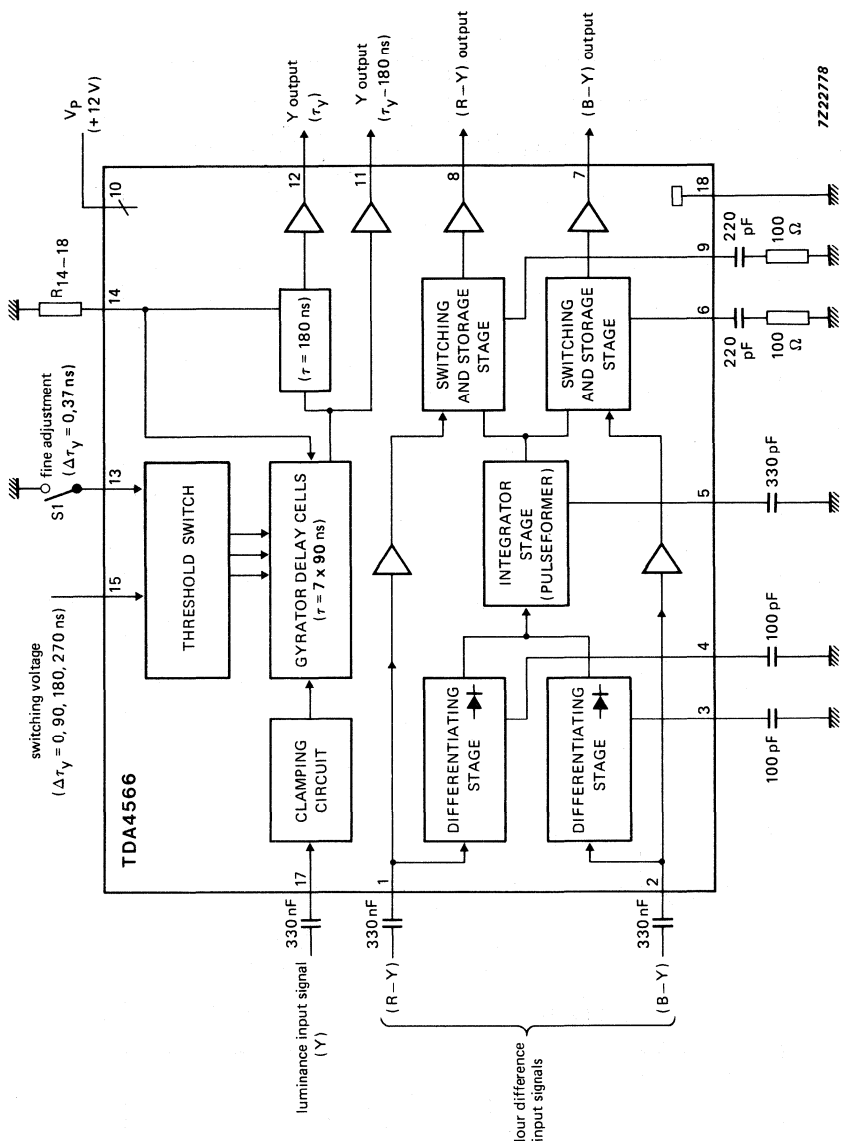


Fig.1 Block diagram.

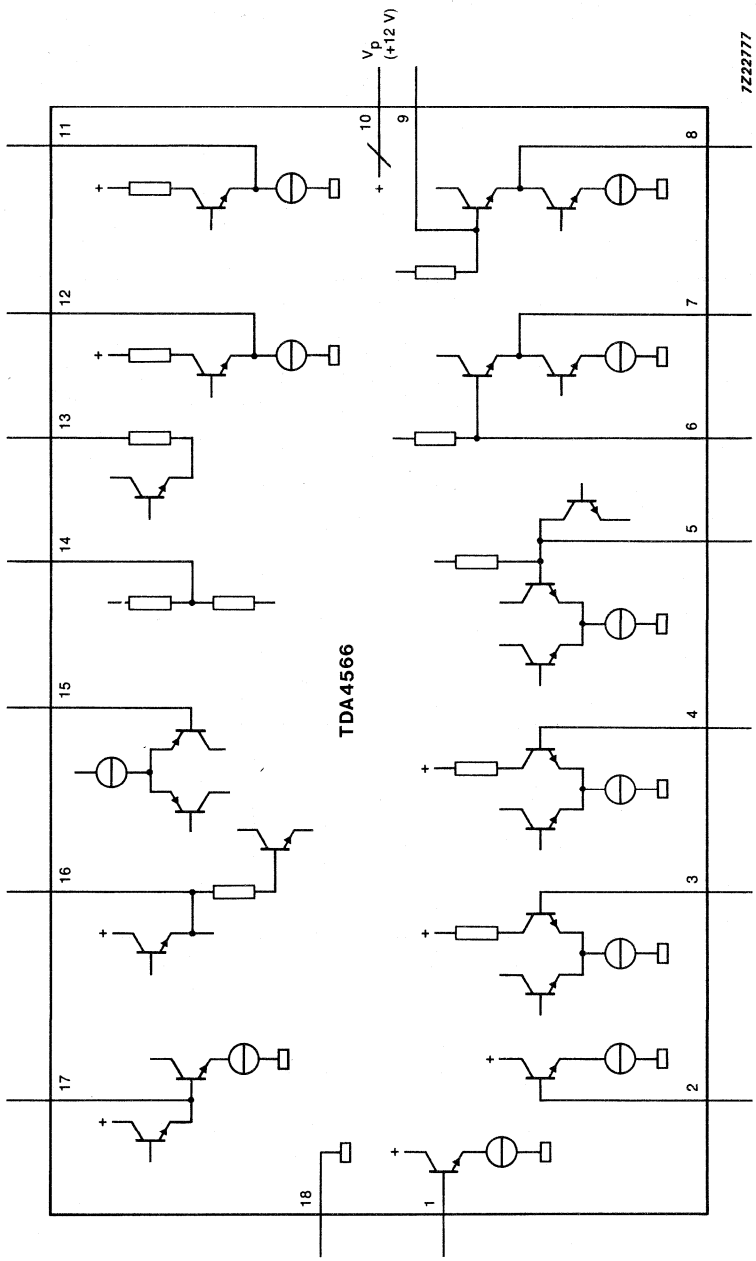


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_P = V_{10-18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12 and 15	V_{n-18}	0	V_P	V
at pin 11	V_{11-18}	0	(V_P–3 V)	V
at pin 17	V_{17-18}	0	7	V
Voltage ranges				
at pin 7 to pin 6	V_{7-6}	0	5	V
at pin 8 to pin 9	V_{8-9}	0	5	V
Currents				
at pins 6, 9	$I_{6,9}$	–10	+ 10	mA
at pins 7, 8, 11 and 12	$I_{7,8,11,12}$	internally limited		
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	–	1.1	W
Storage temperature range	T_{stg}	–25	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j-a}$ = 70 K/W

Note

Pins 3, 4, 5, 6, 9, 13 and 14 DC potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_P	10.8	12	13.2	V
Supply current		I_P	–	35	50	mA
Colour difference paths						
(R-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{1(p-p)}$	–	0.63	1.5	V
(B-Y) input voltage (75% colour bar signal) (peak-to-peak value)		$V_{2(p-p)}$	–	0.8	1.9	V
Input resistance						
(R-Y)		R_{1-18}	8	12	16	kΩ
(B-Y)		R_{2-18}	8	12	16	kΩ
Internal bias voltage						
(R-Y)		V_{1-18}	3.8	4.3	4.8	V
(B-Y)		V_{1-18}	3.8	4.3	4.8	V
Signal attenuation						
(R-Y)		V_8/V_1	−1	0	+ 1	dB
(B-Y)		V_7/V_2	−1	0	+ 1	dB
Output transient time	note 1	t_{tr}	–	100	200	ns
Output resistance						
(B-Y)		R_{7-18}	–	100	–	Ω
(R-Y)		R_{8-18}	–	100	–	Ω
DC output voltage						
(B-Y)		V_{7-18}	3.8	4.3	4.8	V
(R-Y)		V_{8-18}	3.8	4.3	4.8	V
Output current	note 2					
source		$I_{7,8}$	0.4	–	–	mA
sink		$-I_{7,8}$	1.0	–	–	mA

CHARACTERISTICS (continued)

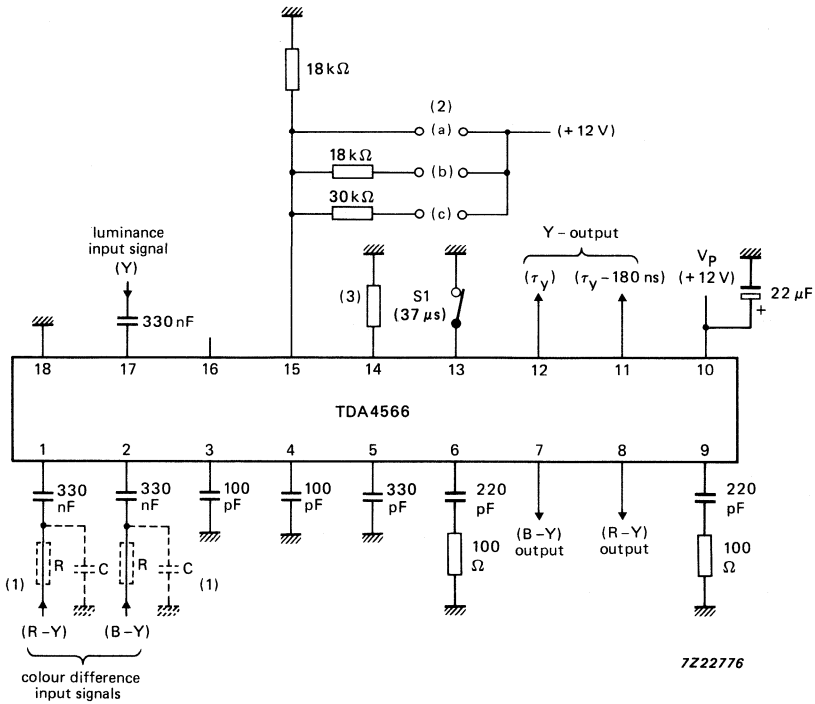
parameter	conditions	symbol	min.	typ.	max.	unit
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p\text{-}p)}$	–	0.45	0.62	V
Internal bias voltage	during clamping	$V_{17\text{-}18}$	2.1	2.4	2.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; R_{14} = 1.2 kΩ; notes 3 and 4					
at $V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}18}$	490	550	610	ns
at $V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}18}$	580	640	700	ns
at $V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}18}$	670	730	790	ns
at $V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}18}$	760	820	880	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	$t_{17\text{-}12}$	–	37	–	ns
Signal delay between pin 11 and pin 12	S1 open	$t_{11\text{-}12}$	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17\text{-}12}}{t_{17\text{-}12} \cdot \Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17\text{-}12}}{t_{17\text{-}12} \cdot \Delta V_P}$	–	–0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	–1	0	+ 1	dB
pin 12 from pin 17		V_{12}/V_{17}	0	+ 1	+ 2	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency response at 5 MHz referred to 0.5 MHz	note 5					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz)}{V_{12}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 2					
source		$I_{11,\ 12}$	–	–	0.4	mA
sink		$-I_{11,\ 12}$	–	–	1.0	mA

Notes to the characteristics

1. Output signal transient time measured with $C_{6\text{-}18} = C_{9\text{-}18} = 220$ pF without resistor (see Fig.3).
2. Output current measured with emitter follower with constant current source of 0.6 mA.
3. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
4. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18} = 1.2$ kΩ.
5. Frequency response measured with $V_{15\text{-}18} = 9.5$ V and switch S1 open.

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.
(3) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4566.
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4566A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	550
0	0	X	3.5 to 5.5 V	640
0	X	X	6.5 to 8.5 V	730
X	X	X	9.5 to 12 V	820

Where : X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 37 ns.

LUMINANCE SIGNAL DELAY CIRCUIT

GENERAL DESCRIPTION

The TDA4568 is an integrated circuit that provides the luminance signal delay in colour television receivers.

Features

- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 550 ns to 820 ns in steps of 90 ns and additional fine adjustment of 37 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)		V_P	10.8	12	13.2	V
Supply current (pin 10)		I_P	–	22	–	mA
Y-signal delay at pin 12	S1 open; $R_{14\text{-}18}$ = 1.2 kΩ*					
$V_{15\text{-}18}$ = 0 to 2.5 V		$t_{17\text{-}12}$	490	550	610	ns
$V_{15\text{-}18}$ = 3.5 to 5.5 V		$t_{17\text{-}12}$	580	640	700	ns
$V_{15\text{-}18}$ = 6.5 to 8.5 V		$t_{17\text{-}12}$	670	730	790	ns
$V_{15\text{-}18}$ = 9.5 to 12 V		$t_{17\text{-}12}$	760	820	880	ns
Y-signal amplification	0.5 MHz	α_Y	0	1	2	dB

* Delay time is proportional to resistor $R_{14\text{-}18}$.
$R_{14\text{-}18}$ also influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

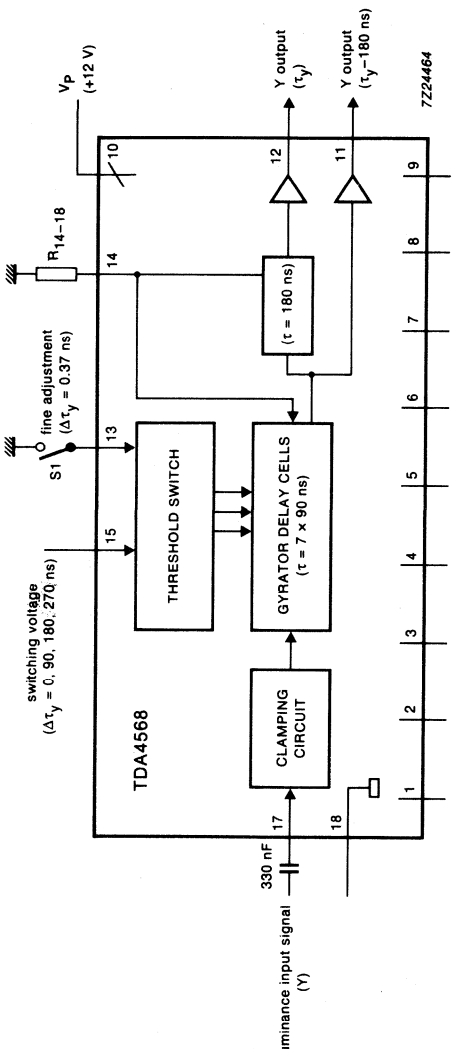


Fig.1 Block diagram.

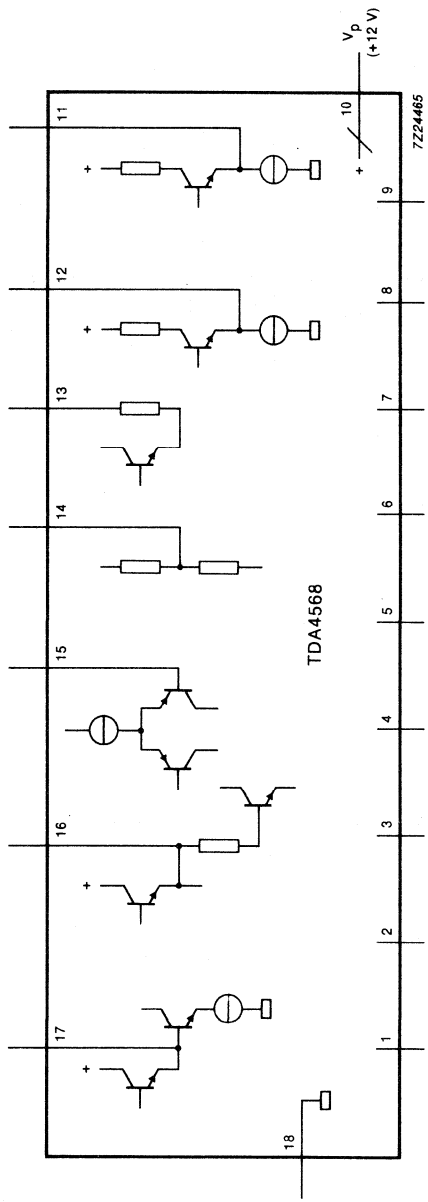


Fig.2 Internal pin circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 10)	$V_P = V_{10-18}$	0	13.2	V
Voltage ranges to pin 18 (ground)				
at pin 15	V_{15-18}	0	V_P	V
at pin 17	V_{17-18}	0	7	V
Current range at pins 11 and 12	$I_{11, 12}$		internally limited	
Total power dissipation (T_j = 150 °C; T_{amb} = 70 °C)	P_{tot}	–	1.1	W
Storage temperature range	T_{stg}	–25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a} = 70$ K/W

Note

Pins 13 and 14, DC potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 10)						
Supply voltage		V_P	10.8	12	13.2	V
Supply current		I_P	–	22	–	mA
Y-signal path						
Y-input voltage (composite signal) (peak-to-peak value)	capacitive coupling	$V_{17(p-p)}$	–	0.45	0.62	V
Internal bias voltage	during clamping	V_{17-18}	2.1	2.4	2.7	V
Input current						
during picture content		I_{17}	–	8	12	μA
during sync. pulse		$-I_{17}$	–	100	150	μA
Y-signal delay at pin 12	S1 open; $R_{14} = 1.2$ kΩ; notes 1 and 2					
at $V_{15-18} = 0$ to 2.5 V		t_{17-18}	490	550	610	ns
at $V_{15-18} = 3.5$ to 5.5 V		t_{17-18}	580	640	700	ns
at $V_{15-18} = 6.5$ to 8.5 V		t_{17-18}	670	730	790	ns
at $V_{15-18} = 9.5$ to 12 V		t_{17-18}	760	820	880	ns
Fine adjustment of Y-signal delay for all 4 steps	S1 closed	t_{17-12}	–	37	–	ns
Signal delay between pin 11 and pin 12	S1 open	t_{11-12}	160	180	200	ns
Dependency of delay time						
on temperature		$\frac{\Delta t_{17-12}}{t_{17-12} \cdot \Delta T_j}$	–	0.001	–	K^{-1}
on supply voltage		$\frac{\Delta t_{17-12}}{t_{17-12} \cdot \Delta V_P}$	–	–0.03	–	V^{-1}
Input switching current		$-I_{15}$	–	15	25	μA
Y-signal attenuation	f = 0.5 MHz					
pin 11 from pin 17		V_{11}/V_{17}	–1	0	+ 1	dB
pin 12 from pin 17		V_{12}/V_{17}	0	+ 1	+ 2	dB
Frequency response at 3 MHz referred to 0.5 MHz	note 3					
pin 11		$\frac{V_{11}\ (3\ MHz)}{V_{11}\ (0.5\ MHz)}$	0	–	3.0	dB
pin 12		$\frac{V_{12}\ (3\ MHz)}{V_{12}\ (0.5\ MHz)}$	0	–	3.0	dB

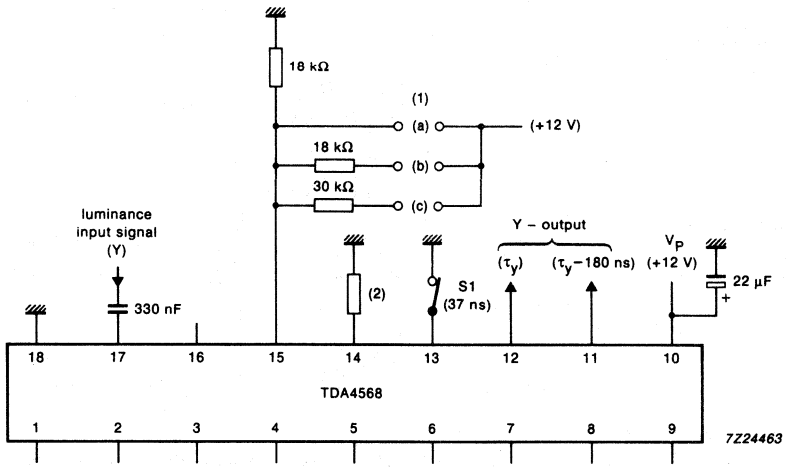
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency response at 5 MHz referred to 0.5 MHz	note 3					
pin 11		$\frac{V_{11}\ (5\ MHz)}{V_{11}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
pin 12		$\frac{V_{12}\ (5\ MHz)}{V_{12}\ (0.5\ MHz)}$	−3.0	–	2.0	dB
DC output voltage						
pin 11		$V_{11\text{-}18}$	1.8	2.3	2.6	V
pin 12		$V_{12\text{-}18}$	9.8	10.3	10.8	V
Output current	note 4					
source		$I_{11,\ 12}$	–	–	0.4	mA
sink		$-I_{11,\ 12}$	–	–	1.0	mA

Notes to the characteristics

1. $R_{14\text{-}18}$ influences the bandwidth; a value of 1.2 kΩ results in a bandwidth of 5 MHz (typ.).
2. Delay time is proportional to resistor $R_{14\text{-}18}$. Devices with suffix "A" require the value of the resistor to be 1.15 kΩ; a 27 kΩ resistor connected in parallel with $R_{14\text{-}18}$ = 1.2 kΩ.
3. Frequency response measured with $V_{15\text{-}18}$ = 9.5 V and switch S1 open.
4. Output current measured with emitter follower with constant current source of 0.6 mA.

APPLICATION INFORMATION



DEVELOPMENT DATA

(1) Switching sequence for delay times shown in Table 1.
(2) $R_{14\text{-}18}$ = 1.2 kΩ for TDA4568.
$R_{14\text{-}18}$ = 1.15 kΩ for TDA4568A (27 kΩ resistor connected in parallel to 1.2 kΩ).

Fig.3 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
0	0	0	0 to 2.5 V	550
0	0	X	3.5 to 5.5 V	640
0	X	X	6.5 to 8.5 V	730
X	X	X	9.5 to 12 V	820

Where : X = connection closed; 0 = connection open.

* When switch (S1) is closed the delay time is increased by 37 ns.

NTSC DECODER

GENERAL DESCRIPTION

The TDA4570 is an integrated 3,58 MHz or 4,43 MHz NTSC decoder. It is pin sequence compatible with multi-standard decoder TDA4555 and pin compatible with the PAL decoder TDA4510.

Features:

Chrominance part

- Gain controlled amplifier with operating point control stage
- ACC (automatic chrominance control) with sampled rectification during burst-key signal
- Blanking circuit for the colour burst signal

Oscillator and control voltage part

- Voltage controlled reference oscillator for double subcarrier frequency
- Divider stages which provide the correct 90° phase between −(R-Y) and −(B-Y) reference signals for the demodulators
- Phase comparator which controls the frequency and phase of the reference oscillator and compares the (R-Y) reference with the burst pulse
- HUE control stage provides phase shifting via the combined service and hue control input (pin 11)
- Identification demodulator provides a positive-going identification signal at pin 14 for NTSC signals and acts as the automatic colour killer
- Two-function service switch:
  position one ($V_{14-3} < 1$ V): switches the colour-ON and switches the hue control and burst for the PLL oscillator-OFF, allowing the adjustment of the reference oscillator
  position two ($V_{14-3} > 5$ V): switches the colour-ON, the hue control OFF and allows the output signal to be observed
- Sandcastle pulse detector for burst-gate, horizontal and horizontal/vertical blanking pulse detection. The vertical part of the sandcastle pulse is used for the internal colour-ON and colour-OFF delay
- Pulse processing part for the prevention of premature switching ON of the colour. The colour-ON delay, two or three field periods after identification of the NTSC signal, is achieved by a counter. When there is no identification voltage present the colour is switched OFF immediately or, at the most, one field period later.

Demodulator part

- Two synchronous demodulators for the (R-Y) and (B-Y) signals, which incorporate stages for the blanking during line and field flyback
- Internal filtering of the residual carrier in the demodulated colour difference signals
- Colour switching stages controlled by the pulse processing part in front of the output stages
- The output stages for (R-Y) and (B-Y) signals are low resistance n-p-n emitter followers
- Separate colour switching output

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

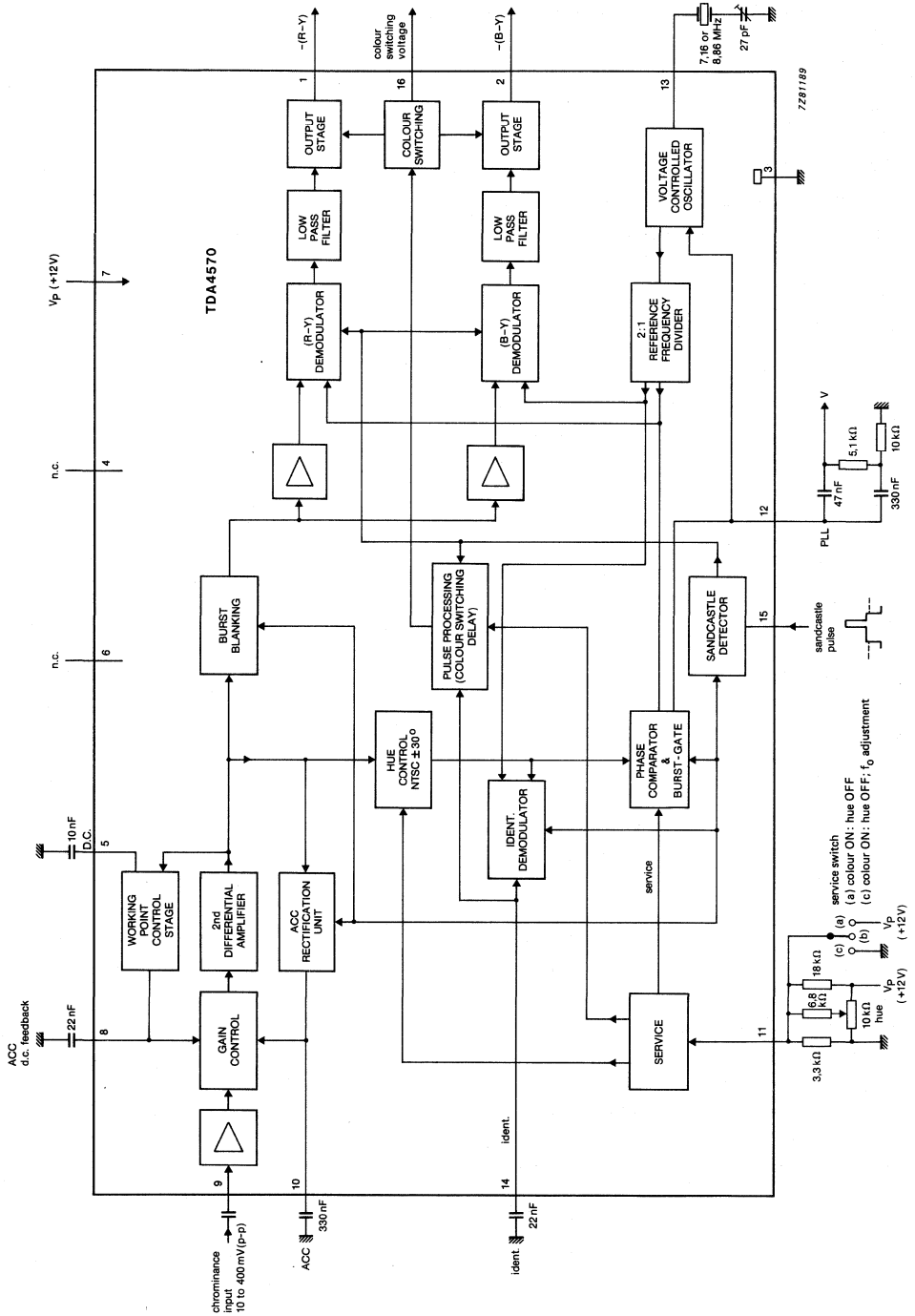


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{7-3}$	10,8 to 13,2		V
Currents at:				
pins 1 and 2	$-I_{1,2}$	max.	5	mA
pin 16	$-I_{16}$	max.	5	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−25 to + 150		°C
Operating ambient temperature range	T_{amb}	0 to + 70		°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	max.	80	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 2 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current	$I_P = I_7$	–	50	–	mA
Chrominance part					
Input voltage range (peak-to-peak value)	$V_{9-3(p-p)}$	10	–	400	mV
Nominal input voltage (peak-to-peak value) with 75% colour bar signal	$V_{9-3(p-p)}$	–	100	–	mV
Input impedance	$\lvert Z_{9-3}\rvert$	–	3,3	–	kΩ
Input capacitance	C_{9-3}	–	4,0	–	pF
Oscillator and control voltage part					
Oscillator frequency for subcarrier frequency					
3,58 MHz	f_{osc}	–	7,16	–	MHz
4,43 MHz	f_{osc}	–	8,86	–	MHz
Input resistance	R_{13-3}	–	350	–	Ω
Catching range (depending on RC network between pins 12 and 3)	Δf	± 300	–	–	Hz
Control voltage					
without burst signal	V_{14-3}	–	6,0	–	V
colour switching threshold	V_{14-3}	–	6,6	–	V
hysteresis of colour switching	V_{14-3}	–	150	–	mV
Colour-ON delay	$t_{d\ on}$	–	–	3	*
Colour-OFF delay	$t_{d\ off}$	–	–	1	*

* Expressed as field periods.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Colour switching output (open n-p-n emitter)					
output current	$-I_{16}$	–	–	5,0	mA
colour-ON voltage	V_{16-3}	–	6,0	–	V
colour-OFF voltage	V_{16-3}	–	0	–	V
HUE control and service switches					
Phase shift of reference carrier relative to the input signal V_{11-3} = 3 V	ϕ	–5	0	+ 5	deg
Phase shift of reference carrier relative to phase at V_{11-3} = 3 V					
V_{11-3} = 2 V	$-\phi$	30	–	–	deg
V_{11-3} = 4 V	$+\phi$	30	–	–	deg
Internal source (open pin)		–	3	–	V
First service position (PLL is inactive for oscillator adjustment, colour ON, HUE OFF)	V_{11-3}	0	–	1	V
Second service position (colour ON, HUE OFF)	V_{11-3}	5	–	V_P	V
Demodulator part					
Colour difference signals output voltage (peak-to-peak value)					
–(R-Y) signal	$V_{1-3(p-p)}$	0,84	1,05	1,32	V
–(B-Y) signal	$V_{2-3(p-p)}$	1,06	1,33	1,67	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$\frac{V_{1-3}}{V_{2-3}}$	0,71	0,79	0,87	
D.C. voltage at colour difference outputs	$V_{1,\,2-3}$	–	7,7	–	V
Residual carrier at colour difference outputs (peak-to-peak value)					
(1 x subcarrier frequency)	$V_{1,\,2-3(p-p)}$	–	–	20	mV
(2 x subcarrier frequency)	$V_{1,\,2-3(p-p)}$	–	–	30	mV

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (note 1)					
Input voltage level (pin 15)					
to separate vertical and horizontal blanking pulses	V_{15-3}	1,3	1,6	1,9	V
required pulse amplitude	V_{15-3}	2,0	2,5	3,0	V
to separate horizontal blanking pulse	V_{15-3}	3,3	3,6	3,9	V
required pulse amplitude	V_{15-3}	4,1	4,5	4,9	V
to separate burst gating pulse	V_{15-3}	6,6	7,1	7,6	V
required pulse amplitude	V_{15-3}	7,7	–	–	V
Input voltage during horizontal scanning	V_{15-3}	–	–	1,1	V
Input current	$-I_{15}$	–	–	100	μA

Note

1. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

APPLICATION INFORMATION

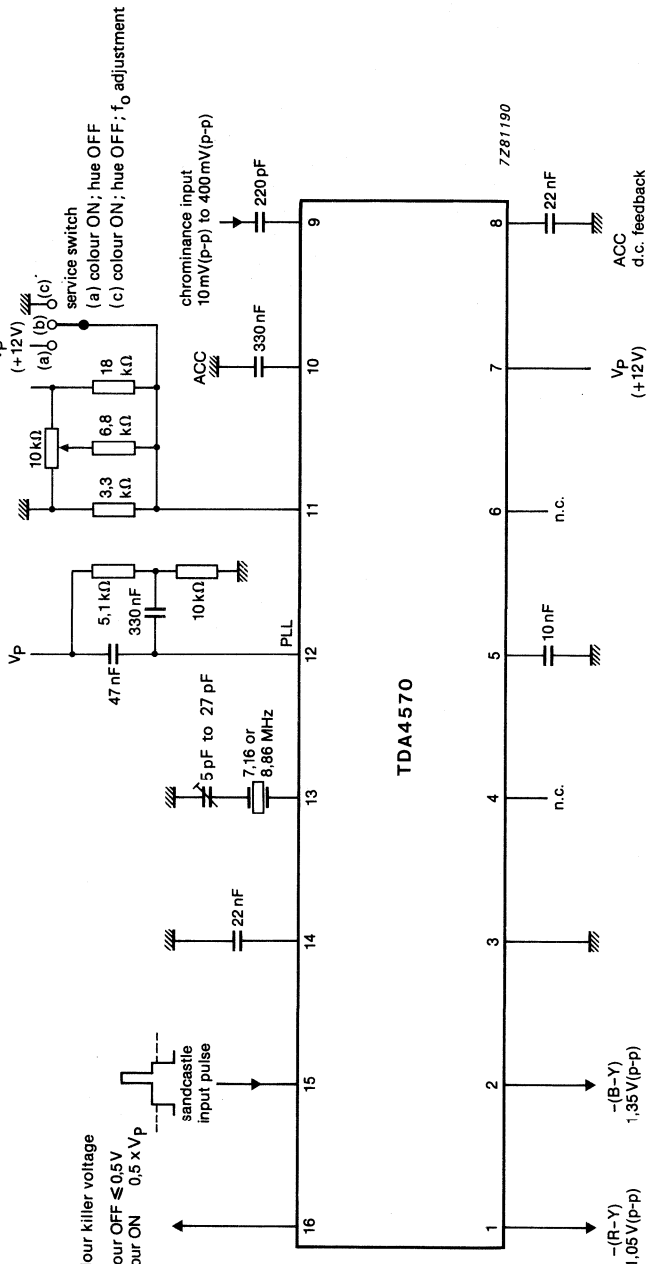


Fig. 2 Application diagram.

Crystal frequency 7, 16 or 8,86 MHz; resonance resistance 60 Ω; load capacitance 20 pF; dynamic capacitance 22 fF and static capacitance 5,5 pF.

VIDEO CONTROL COMBINATION CIRCUIT

with automatic cut-off control

GENERAL DESCRIPTION

The TDA4580 is a monolithic integrated circuit which performs video control functions in television receivers with a colour difference interface. For example it operates in conjunction the multistandard colour decoder TDA4555. The required input signals are: luminance and negative colour difference −(R-Y) and −(B-Y), and a 3-level sandcastle pulse for control purposes. Analogue RGB signals can be inserted from two sources. One with full performance adjustment possibilities. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

Features

- Capacitive coupling of the colour difference, luminance and RGB input signals with black level clamping
- Two sets of analogue RGB inputs via fast switch 1 and fast switch 2
- First RGB inputs and fast switch 1 in accordance with peritelevision connector specification
- Saturation, contrast and brightness control acting on first RGB inputs
- Brightness control acting on second RGB inputs
- Equal black levels for television and inserted signals
- Clamping, horizontal and vertical blanking, and timing of automatic cut-off, controlled by a 3-level sandcastle pulse
- Automatic cut-off control with compensation for leakage current of the picture tube
- Measuring pulses of cut-off control start immediately after end of vertical part of sandcastle pulse
- Three selectable blanking intervals for PAL, SECAM and NTSC/PAL-M
- Two switch-on delays for run-in without discolouration
- Adjustable peak drive limiter
- Average beam current limiter
- G-Y and RGB matrix coefficients selectable for PAL/SECAM and NTSC (correction for FCC primaries)
- Bandwidth 10 MHz (typ.)
- Emitter-follower outputs for driving the RGB output stages

QUICK REFERENCE DATA

Supply voltage (pin 6)	$V_P = V_{6-24}$	typ.	12 V
Supply current (pin 6)	$I_P = I_6$	typ.	110 mA
Luminance input (pin 15)			
Composite video input signal (VBS) (peak-to-peak value)	$V_{15-24(p-p)}$	typ.	0,45 V
Colour difference input signals (peak-to-peak values)			
−(B-Y)	$V_{18-24(p-p)}$	typ.	1,33 V
−(R-Y)	$V_{17-24(p-p)}$	typ.	1,05 V
Inserted RGB signals (black to white values)	$V_{14, 13, 12-24}$	typ.	0,7 V
Inserted RGB signals for teletext use (black to white values)	$V_{23, 22, 21-24}$	typ.	1 V
Three-level sandcastle pulse (required input voltage)	V_{10-24}	typ.	2,5/4,5/8,0 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

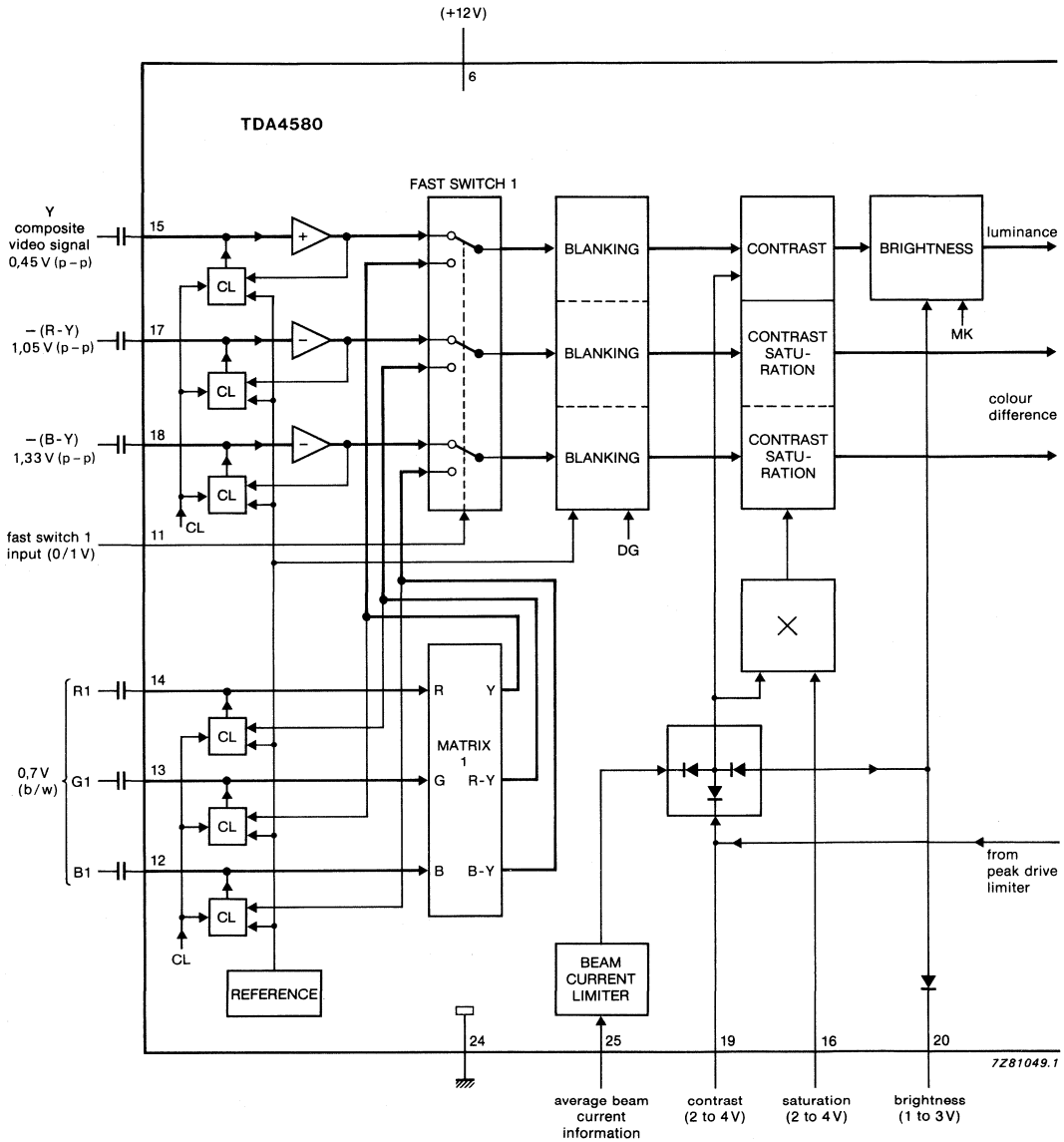


Fig. 1a Part of block diagram; continued in Fig. 1b.

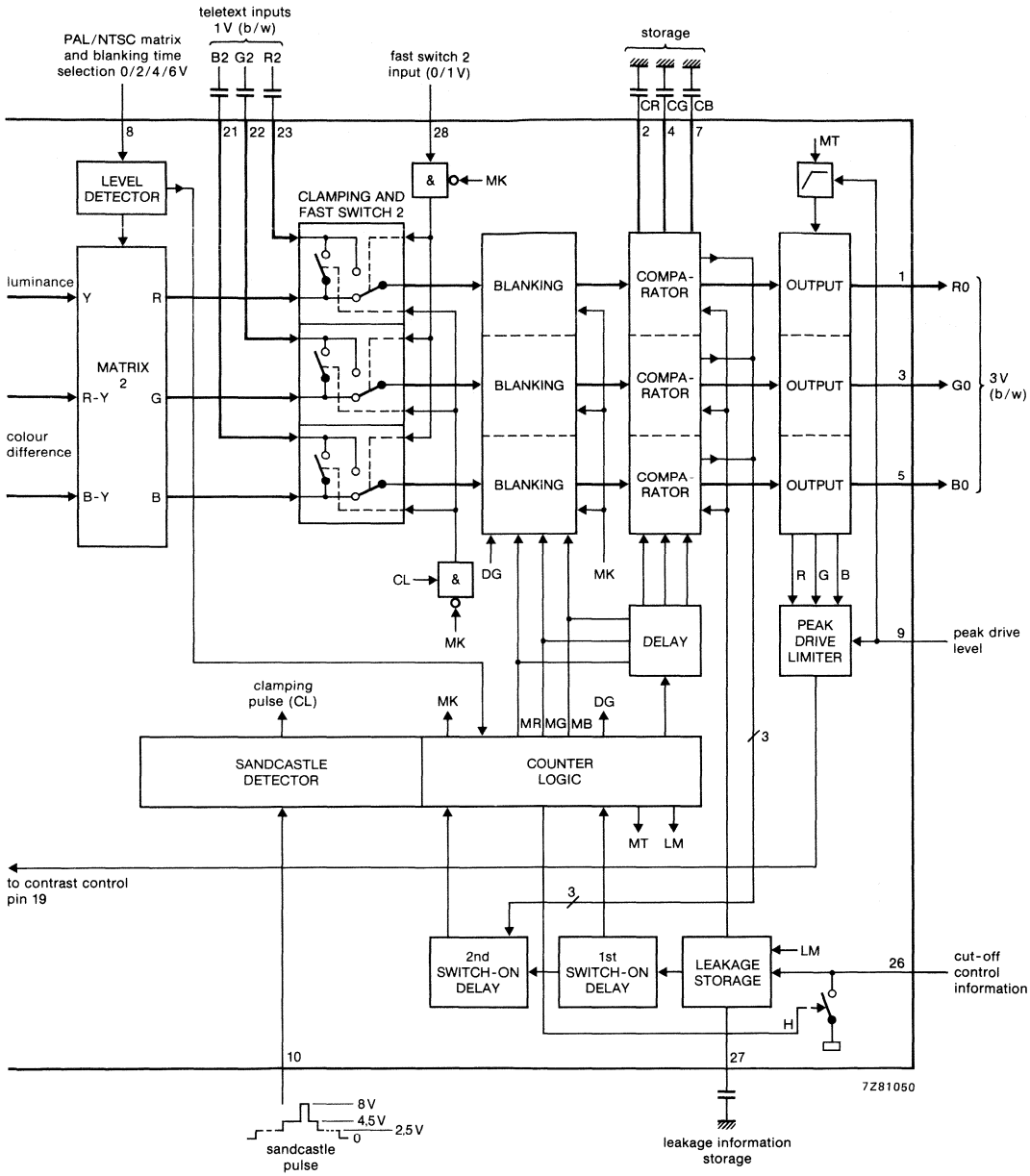


Fig. 1b Part of block diagram; continued from Fig. 1a.

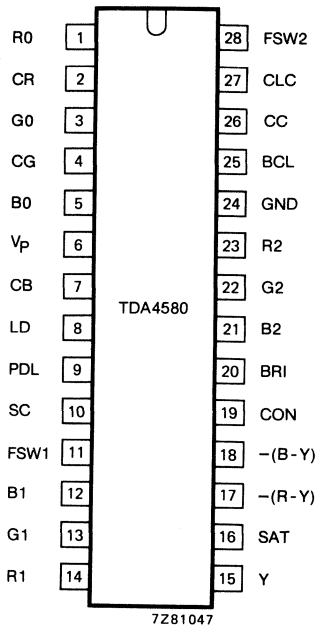


Fig. 2 Pinning diagram.

PINNING

pin no.	mnemonic	description
1	R0	Red output
2	CR	Red storage capacitor for cut-off control
3	G0	Green output
4	CG	Green storage capacitor for cut-off control
5	B0	Blue output
6	V_P	Positive supply voltage (+ 12 V)
7	CB	Blue storage capacitor for cut-off control
8	LD	PAL/NTSC matrix and blanking time level detector input
9	PDL	Peak drive limiting input
10	SC	Sandcastle pulse input
11	FSW1	Fast switch 1 for Y, CD and RGB inputs
12	B1	Blue input (external signal)
13	G1	Green input (external signal)
14	R1	Red input (external signal)
15	Y	Luminance input
16	SAT	Saturation control input
17	−(R-Y)	Colour difference input −(R-Y)
18	−(B-Y)	Colour difference input −(B-Y)
19	CON	Contrast control input
20	BRI	Brightness control input
21	B2	Teletext blue input
22	G2	Teletext green input
23	R2	Teletext red input
24	GND	Ground
25	BCL	Average beam current limiting input
26	CC	Automatic cut-off control input
27	CLC	Storage capacitor for leakage current
28	FSW2	Fast switch 2 for teletext inputs

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 6)	$V_P = V_{6-24}$		0 to 13,2	V
Voltage range at pins 2, 4, 7, 9, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 25, 27 to pin 24 (ground)	V_{n-24}		0 to V_P	V
Voltages ranges				
at pins 8, 11, 28	$V_{8, 11, 28-24}$		−0,5 to V_P	V
at pin 10	V_{10-24}		0 to V_P + 0,7	V
at pin 26	V_{26-24}		−0,7 to V_P + 0,7	V
Currents				
at pins 1, 3, 5 (average)	$-I_{1, 3, 5(AV)}$	max.	3	mA
at pins 1, 3, 5 (peak)	$-I_{1, 3, 5(M)}$	max.	10	mA
at pin 19 (average)	$I_{19(AV)}$	max.	5	mA
at pin 26	I_{26}	max.	1	mA
Total power dissipation	P_{tot}	max.	2	W
Storage temperature range	T_{stg}		−20 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	37	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in a circuit similar to Fig. 4 at nominal settings (saturation, contrast, brightness), no beam current or peak drive limiting; all voltages with respect to pin 24 (ground) unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 6)					
Supply voltage range	$V_P = V_{6-24}$	10,8	–	13,2	V
Supply current	$I_P = I_6$	–	110	–	mA
Colour difference inputs (pins 17 and 18)					
–(R-Y) input signal at pin 17 (notes 1 and 2) (peak-to-peak value)	$V_{17-24(p-p)}$	–	1,05	–	V
–(B-Y) input signal at pin 18 (notes 1 and 2) (peak-to-peak value)	$V_{18-24(p-p)}$	–	1,33	–	V
Input current during scanning	$\|I_{17, 18}\|$	–	–	0,3	μA
Input resistance	$R_{17, 18}$	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	$V_{17, 18-24}$	–	7,5	–	V
Luminance input (pin 15; note 2)					
Composite video input signal (VBS) (peak-to-peak value)	$V_{15-24(p-p)}$	–	0,45	–	V
Input current during scanning	$\|I_{15}\|$	–	–	0,3	μA
Input resistance	R_{15}	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	V_{15-24}	–	7,4	–	V
Signal switch 1 input (pin 11)					
Input voltage level for insertion of Y and CD signals	V_{11-24}	–	–	0,4	V
RGB1 signals	V_{11-24}	0,9	–	3,0	V
Internal resistor to ground	R_{11}	–	10	–	kΩ
RGB1 inputs (R1 pin 14, G1 pin 13, B1 pin 12; note 2) (signals controlled by saturation, contrast and brightness)					
Input signal (black to white value)	$V_{12, 13, 14-24}$	–	0,7	–	V
Input current during scanning	$\|I_{12, 13, 14}\|$	–	–	0,3	μA
Input resistance	$R_{12, 13, 14}$	5	–	–	MΩ
Internal d.c. bias voltage during clamping time	$V_{12, 13, 14-24}$	–	8,2	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB/Y, (R-Y), (B-Y) – Matrix					
Matrixed according to the equations $V_{(R-Y)} = 0{,}7\ V_R - 0{,}59\ V_G - 0{,}11\ V_B$ $V_{(B-Y)} = -0{,}3\ V_R - 0{,}59\ V_G + 0{,}89\ V_B$ $V_{(Y)} = 0{,}3\ V_R + 0{,}59\ V_G + 0{,}11\ V_B$					
Contrast control input (pin 19; note 3) (contrast control acts on Y and CD signals or RGB1 signals respectively)					
Maximum contrast	V_{19-24}	–	4	–	V
Nominal contrast (6 dB below max.)	V_{19-24}	–	3	–	V
Attenuation of contrast at V_{19-24} = 2 V (related to max.)		–	22	–	dB
Input current at V_{19-24} = 2 to 4 V	$-I_{19}$	–	–	3	μA
Peak drive limiting input (pin 9; note 4)					
Internal d.c. bias voltage	V_{9-24}	–	9	–	V
Input resistance at $V_{9-24} > 9$ V	R_9	–	10	–	kΩ
Control current into contrast input (pin 19) during peak drive $V_{1,\ 2\ or\ 3-24} > V_{9-24}$	I_{19}	–	20	–	mA
Average beam current limiting input (pin 25; note 5)					
Start of contrast reduction at maximum contrast setting	V_{25-24}	–	8,5	–	V
Input range for full contrast reduction	ΔV_{25-24}	–	1,0	–	V
Input resistance at $V_{25-24} < 6$ V	R_{25}	–	2,2	–	kΩ
Saturation control input (pin 16) (saturation control acts on CD signals or RGB1 signals respectively)					
Maximum saturation	V_{16-24}	–	4	–	V
Nominal saturation (6 dB below max.)	V_{16-24}	–	3	–	V
Attenuation of saturation at V_{16-24} = 1,8 V (related to max. at 100 kHz)		50	–	–	dB
Input current at V_{16-24} = 1,8 to 4 V	I_{16}	–	–	10	μA

parameter	symbol	min.	typ.	max.	unit
Brightness control input (pin 20; note 6 and 7)					
Control voltage range	V_{20-24}	1	–	3	V
Input current at V_{20-24} = 1 to 3 V	$-I_{20}$	–	–	10	μA
Control voltage for nominal brightness	V_{20-24}	–	2,2	–	V
Change of black level in the control range related to the nominal output signal (black/white) for ΔV_{20-24} = 1 V		–	33	–	%
Signal switched off and black level equal to cut-off measuring level at	V_{20-24}	11,5	–	–	V
Y, (R-Y), (B-Y)/RGB – Matrix (note 8)					
PAL matrix (V_{8-24} = < 4,5 V)					
Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$					
NTSC matrix (V_{8-24} = > 5,5 V)					
(Adaption for NTSC-FCC primaries, nominal hue control set on −5°)					
Matrixed according to the equation $V_{(G-Y)}^* = -0{,}43\ V_{(R-Y)} - 0{,}11\ V_{(B-Y)}$ $V_{(R-Y)}^* = 1{,}57\ V_{(R-Y)} - 0{,}41\ V_{(B-Y)}$ $V_{(B-Y)}^* = V_{(B-Y)}$					
RGB2 inputs (Teletext) (R2 pin 23, G2 pin 22, B2 pin 21; note 2)					
(RGB signals controlled by brightness control)					
Input signal for 100% output signals (black to white value)	$V_{21, 22, 23-24}$	–	1	–	V
Input current during scanning	$I_{21, 22, 23}$	–	–	0,3	μA
Input resistance	$R_{21, 22, 23}$	5	–	–	MΩ
Signal switch 2 input (pin 28)					
Input voltage level for insertion of Y, CD signals or RGB1 signals respectively RGB signals from matrix (note 9)	V_{28-24}	–	–	0,4	V
RGB2 signals (note 9)	V_{28-24}	0,9	–	3,0	V
Internal resistor to ground	R_{28-24}	–	10	–	kΩ

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Automatic cut-off control input (pin 26; note 10) (leakage current measuring time and insertion of RGB cut-off measuring lines see Fig. 5; types of ultra-black level see Fig. 3)					
Allowed maximum external D.C. bias voltage	$V_{26\text{-}24}$	5,5	–	–	V
Voltage difference between cut-off current measurement and leakage current measurement	$\Delta V_{26\text{-}24}$	–	0,5	–	V
Warm-up test pulse	$V_{1,\ 3,\ 5\text{-}24}$	–	$V_{9\text{-}24}$*	–	V
Threshold for warm-up detector	$V_{26\text{-}24}$	–	8	–	V
Storage input for leakage current (pin 27)					
Internal resistance during leakage current measuring time (current limiting at $I_{27} = 0{,}2$ mA)	R_{27}	–	400	–	Ω
Input current except during cut-off control cycle	$\lvert I_{27}\rvert$	–	–	0,5	μA
Storage inputs for automatic cut-off control (pins 2, 4, 7)					
Charge and discharge currents	$\lvert I_{2,\ 4,\ 7}\rvert$	–	0,3	–	mA
Input currents of storage inputs out of control time	$\lvert I_{2,\ 4,\ 7}\rvert$	–	–	0,1	μA
Switch input for PAL/NTSC matrix and vertical blanking time (pin 8; note 11)					
Switching voltage input for					
PAL matrix and vertical blanking period of					
25 lines	$V_{8\text{-}24}$	–	0	0,5	V
22 lines	$V_{8\text{-}24}$	1,5	2	2,5	V
18 lines	$V_{8\text{-}24}$	3,5	4	4,5	V
NTSC matrix and vertical blanking period of					
18 lines	$V_{8\text{-}24}$	5,5	6	12	V
Input current	I_8	–	–	50	μA

* Maximum 8 V.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (pin 10; note 12)					
The following amplitudes are required for separating the various pulses:					
horizontal and vertical blanking pulses	V_{10-24}	2,0	2,5	3,0	V
horizontal pulses for counter logic	V_{10-24}	4,0	4,5	5,0	V
clamping pulses	V_{10-24}	7,5	–	–	V
delay of leading edge of clamping pulse	t_d	–	1	–	μs
Input current at V_{10-24} = 0 V	$-I_{10}$	–	–	100	μA
Outputs for positive RGB signals (R0 pin 1, G0 pin 3, B0 pin 5; note 13)					
Nominal signal amplitude (black/white)	$V_{1, 3, 5-24}$	–	3	–	V
Spreads between channels		–	–	10	%
Maximum signal amplitude (black/white)	$V_{1, 3, 5-24}$	4	–	–	V
Internal current source	$I_{1, 3, 5}$	–	3	–	mA
Output resistance	$R_{1, 3, 5}$	–	160	220	Ω
Minimum output voltage	$V_{1, 3, 5-24}$	–	1	–	V
Maximum output voltage	$V_{1, 3, 5-24}$	–	10	–	V
Horizontal and vertical blanking to ultra-black level 2 related to nominal signal black level in percentage of nominal signal amplitude		45	55	–	%
Vertical blanking to ultra-black level 1 related to cut-off measuring level in percentage of nominal signal amplitude		25	35	–	%
Recommendation:					
Range for cut-off measuring level 1,5 to 5,0 V; nominal value at 3 V (note 14)					
Gain data (note 15)					
Frequency response of Y path (0 to 8 MHz) pins 1, 3 and 5 to pin 15	d	–	–	3	dB
Frequency response of CD path (0 to 8 MHz) pin 1 to pin 17 = pin 5 to pin 18	d	–	–	3	dB
Frequency response of RGB1 path (0 to 8 MHz) pin 1 to pin 14 = pin 3 to pin 13 = pin 5 to pin 12	d	–	–	3	dB
Frequency response of RGB2 path (0 to 10 MHz) pin 1 to pin 23 = pin 3 to pin 22 = pin 5 to pin 21	d	–	–	3	dB

Notes to the characteristics

1. The value of the colour difference input signals, −(B-Y) and −(R-Y), is given for saturated colour bar with 75% of maximum amplitude.
2. Capacitive coupled to a low ohmic source; recommended value 600 Ω (max.).
3. At pin 19 for $V_{19-24} \leqslant 2{,}0$ V, no further decrease of contrast is possible.
4. The peak drive limiting of output signals is achieved by contrast reduction. The limiting level of the output signals is equal to the voltage V_{9-24}, adjustable in the range 5 to 11 V. After exceeding the adjusted limiting level at peak drive limiter will not be active during the first line.
5. The average beam current limiting acts on contrast and at minimum contrast on brightness (the external contrast voltage at pin 19 is not affected).
6. At nominal brightness the black level at the output is 0,3 V ($\triangleq$ −10% of nominal signal amplitude) below the measuring level.
7. The internal control voltage can never be more positive than 0,7 V above the internal contrast voltage.
8. Matrix equation

   $V_{(R-Y)}$, $V_{(B-Y)}$: output of NTSC decoder of PAL type demodulating axis and amplitudes

   $V_{(G-Y)}{}^*$, $V_{(R-Y)}{}^*$, $V_{(B-Y)}{}^*$: for NTSC modified CD signals; equivalent to demodulation with the following axes and amplification factors:−

(B-Y)* demodulator axis	0°	
(R-Y)* demodulator axis	115°	(PAL 90°)
(R-Y)* amplification factor	1,97	(PAL 1,14)
(B-Y)* amplification factor	2,03	(PAL 2,03)

   $V_{(G-Y)}{}^* = -0{,}27\ V_{(R-Y)}{}^* - 0{,}22\ V_{(B-Y)}{}^*$.
9. During clamping time, in each channel the black level of the inserted signal is clamped on the black level of the internal signal behind the matrix (dependent on brightness control).
10. During warm-up time of the picture tube, the RGB outputs (pins 1, 3 and 5) are blanked to minimum output voltage. An inserted white pulse during the vertical flyback is used for beam current detection. If the beam current exceeds the threshold of the warm-up detector at pin 26, the cut-off current control starts operating, but the video signal is still blanked. After run-in of the cut-off current control loop, the video signal will be released.
    The first measuring pulse occurs in the first complete line after the end of the vertical part of the sandcastle pulse. The absolute minimum vertical part must contain 9 line-pulses. The cycle time of the counter is 63 lines. When the vertical pulse is longer than 61 lines, the IC is reset to the switch-on condition. In this event the video signal is blanked and the RGB-outputs are blanked to minimum output voltage as during warm-up time.
    During leakage current measurement, all three channels are blanked to ultra-black level 1. With the measuring level only in the controlled channel, the other two channels are blanked to ultra-black level 1. The brightness control shifts both the signal black level and the ultra-black level 2. The brightness control is disabled from line 4 to the end of the last measuring line (see Fig. 3).
    With the most adverse conditions (maximum brightness and minimum black level 2) the blanking level is located 30% of nominal signal amplitude below the cut-off measuring level.

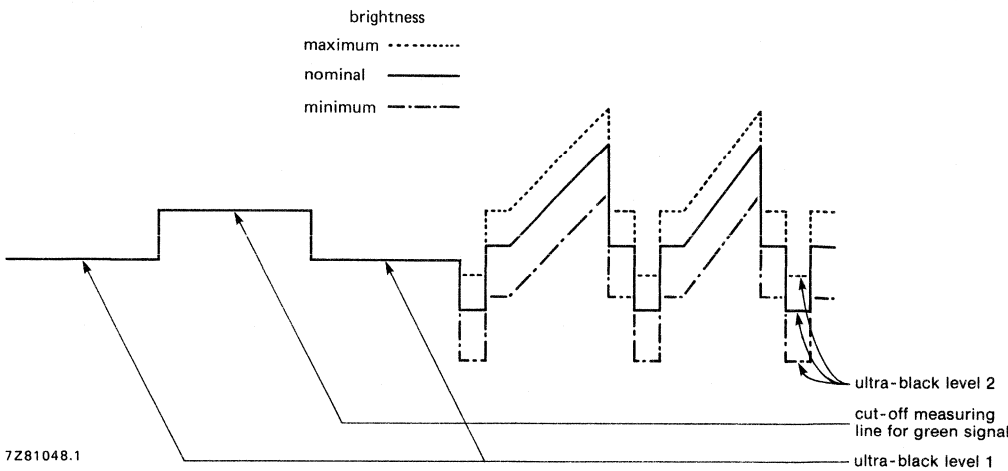
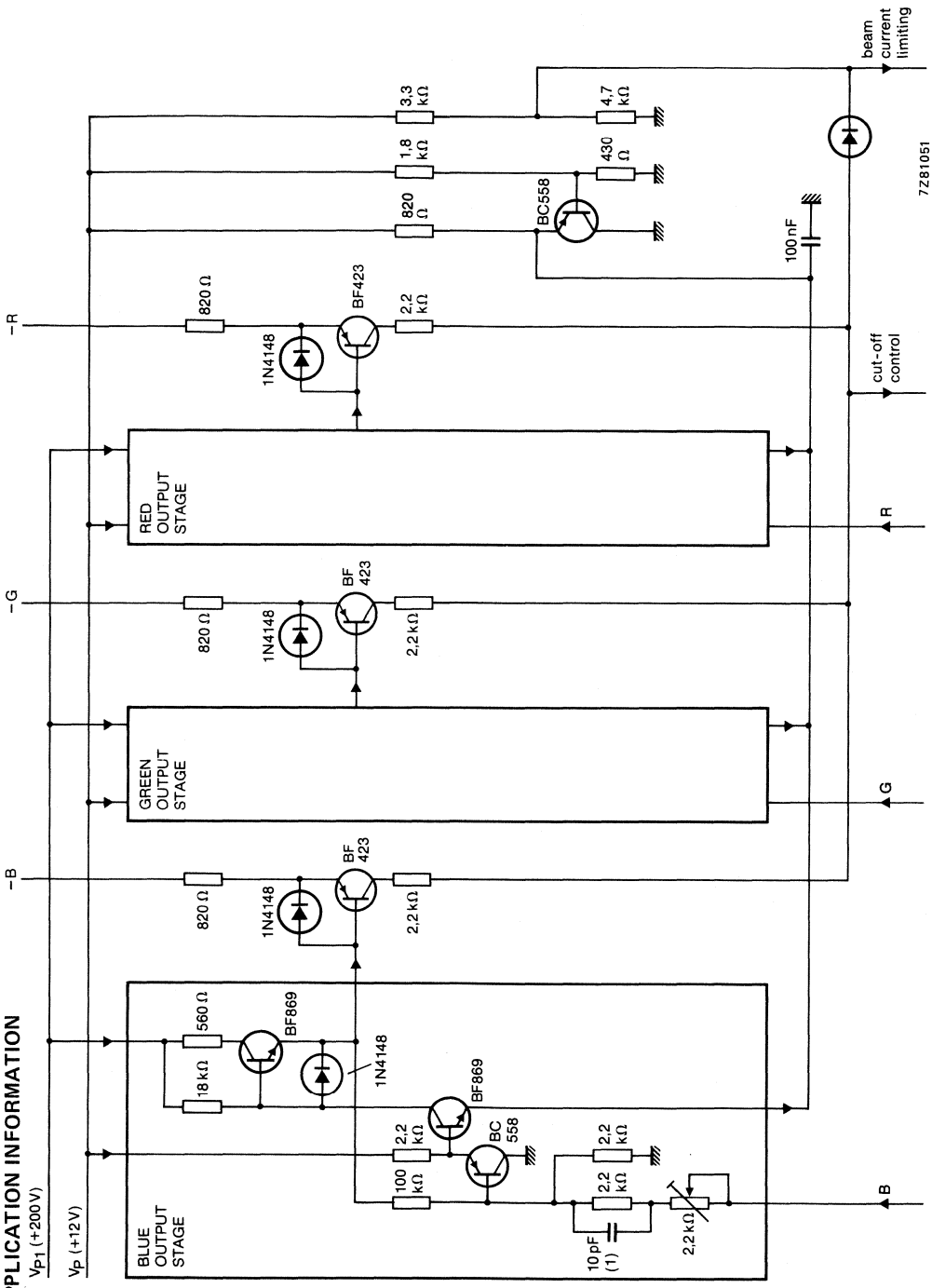


Fig. 3 Types of ultra-black levels.

11. The given blanking times are valid for the vertical part of the sandcastle pulse of 9 to 15 lines. If the vertical part is longer and the cut-off lines are outside the vertical blanking period of 18, 22 or 25 lines respectively, the blanking of the signal ends with the end of last of the three cut-off measuring pulses as shown in Fig. 5.
12. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) to separate the various pulses. The internal pulses are generated when the input pulse at pin 10 exceeds the thresholds. The thresholds are for:
    - Horizontal and vertical blanking $V_{10\text{-}24} = 1{,}5$ V
    - Horizontal pulse $V_{10\text{-}24} = 3{,}5$ V
    - Clamping pulse $V_{10\text{-}24} = 7{,}0$ V
13. The outputs at pins 1, 3 and 5 are emitter followers with current sources and emitter protection resistors.
14. The value of the cut-off control range for the positive RGB output signals is given for a nominal output signal. If the signal amplitude is reduced, the cut-off range can be increased.
15. The gain data is given for a nominal setting of the contrast and saturation controls, measured without load at the RGB outputs (pins 1, 3 and 5).

APPLICATION INFORMATION



(1) Capacitor value depends on circuit layout.

Fig. 4a Part of typical application circuit diagram using the TDA4580; continued in Fig. 4b.

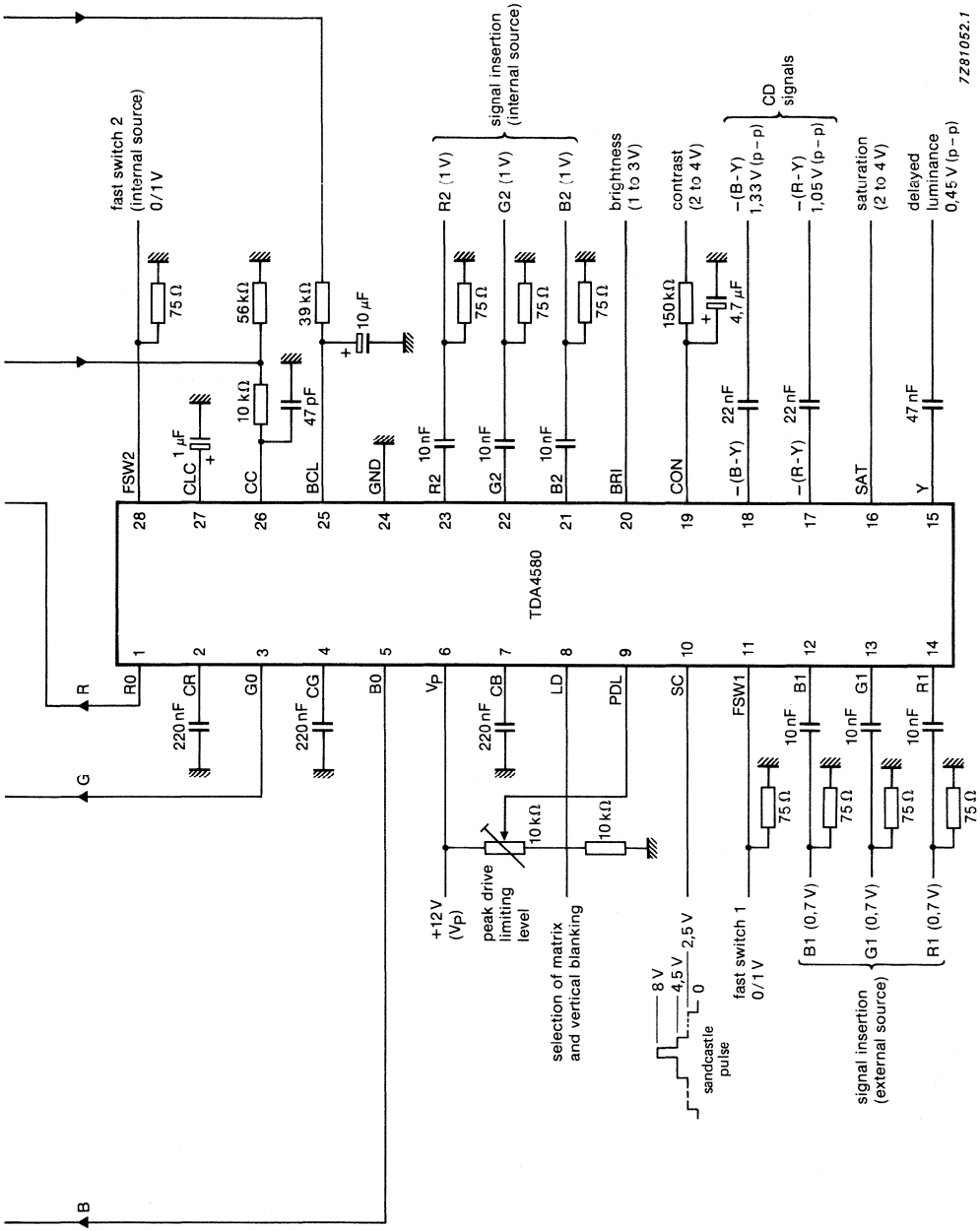
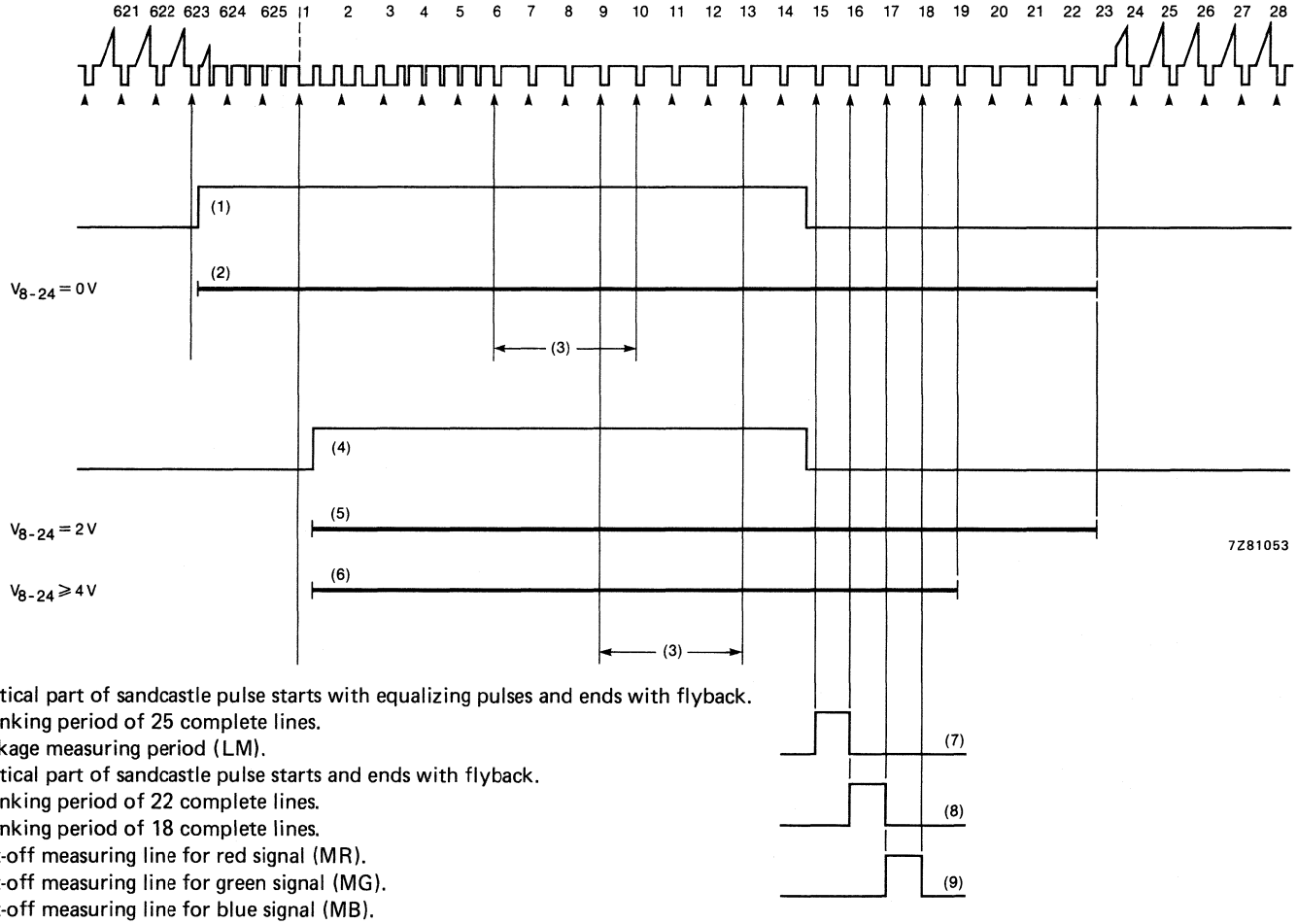


Fig. 4b Part of typical application circuit diagram using the TDA4580; continued from Fig. 4a.

APPLICATION INFORMATION (continued)



(1) vertical part of sandcastle pulse starts with equalizing pulses and ends with flyback.
(2) blanking period of 25 complete lines.
(3) leakage measuring period (LM).
(4) vertical part of sandcastle pulse starts and ends with flyback.
(5) blanking period of 22 complete lines.
(6) blanking period of 18 complete lines.
(7) cut-off measuring line for red signal (MR).
(8) cut-off measuring line for green signal (MG).
(9) cut-off measuring line for blue signal (MB).

Fig. 5 Blanking and measuring lines.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA4650

Multistandard colour decoder, with negative colour difference output signals

FEATURES

Identifies and demodulates PAL, SECAM, NTSC 3.58 and NTSC 4.43 chrominance signals with:

- Identification
  - automatic standard identification by sequential inquiry
  - secure SECAM identification at 50 Hz only, with PAL priority
  - four switched outputs for chrominance filter selection and display control
  - external service switch for oscillator adjustment
- PAL / NTSC demodulation
  - H (burst) and V blanking
  - PAL switch (disabled for NTSC)
  - NTSC phase shift (disabled for PAL)
  - PLL-controlled reference oscillator
  - two reference oscillator crystals on separate pins with automatic switching
  - quadrature demodulator with subcarrier reference
- SECAM demodulation
  - limiter-amplifier
  - quadrature-demodulator with a single external reference tuned circuit
  - alternate line blanking, H and V blanking
  - de-emphasis
- Gain controlled chrominance amplifier
- ACC demodulation controlled by system scanning
- Internal colour-difference signal output filters to remove the residual subcarrier

GENERAL DESCRIPTION

The TDA4650 is a monolitic integrated multistandard colour decoder for PAL, SECAM and NTSC (3.58 and 4.43 MHz) with negative colour difference output signals. The colour-difference output signals are fed to the TDA4660/TDA4661, Switched capacitor delay line.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 13)		10.8	12.0	13.2	V
I_P	supply current (pin 13)		–	60	–	mA
$V_{i(p-p)}$	chrominance input voltage (pin 15) (peak-to-peak value)		20	100	400	mV
$V_{o(p-p)}$	colour-difference output voltage (pin 1) (peak-to-peak value)	PAL/NTSC	0.42	0.525	0.66	V
	colour-difference output voltage (pin 3) (peak-to-peak value)	PAL/NTSC	0.53	0.665	0.84	V
	colour-difference output voltage (pin 1) (peak-to-peak value)	SECAM	0.83	1.05	1.32	V
	colour-difference output voltage (pin 3) (peak-to-peak value)	SECAM	1.06	1.33	1.67	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4650	28	DIL	plastic	SOT117
TDA4650WP	28	PLCC	plastic	SOT261

Multistandard colour decoder, with negative colour difference output signals

TDA4650

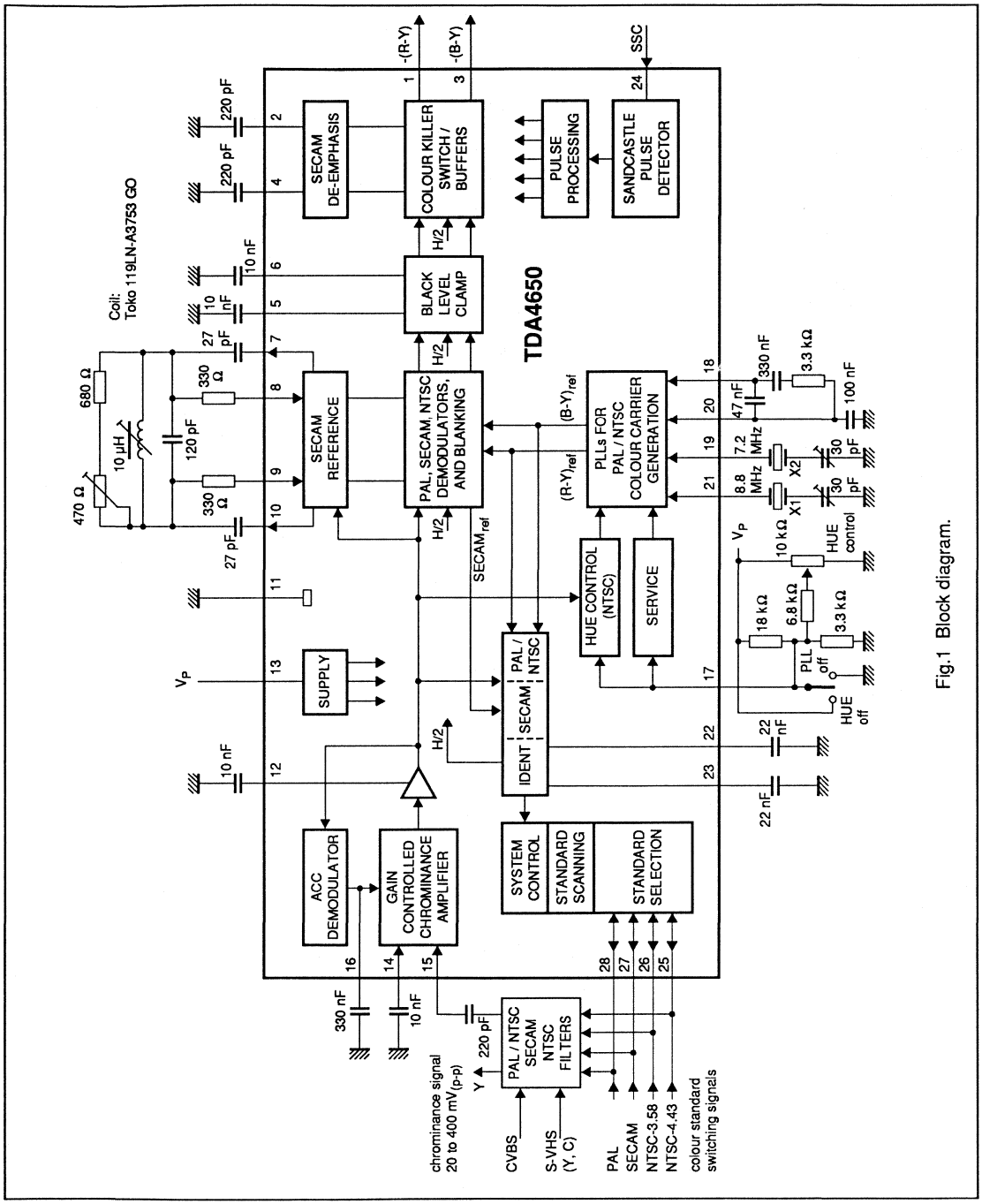


Fig.1 Block diagram.

Multistandard colour decoder, with negative colour difference output signals

TDA4650

PINNING

SYMBOL	PIN	DESCRIPTION
$-(R\text{-}Y)_O$	1	-(R-Y) output
$-(R\text{-}Y)_{DE}$	2	(R-Y) de-emphasis
$-(B\text{-}Y)_O$	3	-(B-Y) output
$-(B\text{-}Y)_{DE}$	4	(B-Y) de-emphasis
$-(B\text{-}Y)_{CL}$	5	(B-Y) clamping
$-(R\text{-}Y)_{CL}$	6	(R-Y) clamping
SEC_{REF}	7	SECAM reference tuned circuit
SEC_{REF}	8	
SEC_{REF}	9	
SEC_{REF}	10	
GND	11	ground
C_D	12	DC for demodulators
V_P	13	supply voltage
C_{DC}	14	DC feedback

SYMBOL	PIN	DESCRIPTION
CHR_I	15	chrominance input
C_{ACC}	16	automatic colour control
HUE	17	hue control
PLL	18	PLL time constant
OSC1	19	input for 7.15 MHz oscillator
C_{PLL}	20	PLL DC reference
OSC2	21	input for 8.86 MHz oscillator
N_{IDENT}	22	NTSC identification
P_{IDENT}	23	PAL/SECAM identification
SSC	24	super sandcastle pulse input
N_{O1}	25	NTSC (4.43 MHz) identification
N_{O2}	26	NTSC (3.58 MHz) identification
SEC_O	27	SECAM identification
PAL_O	28	PAL identification

PIN CONFIGURATIONS

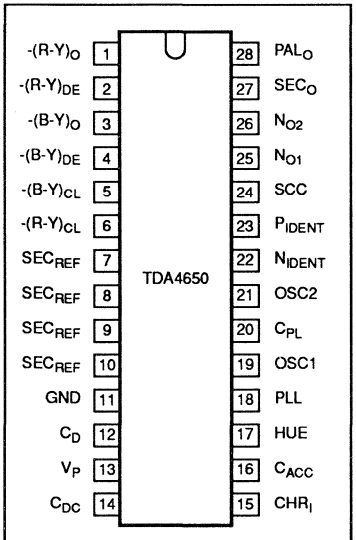


Fig.2(a) Pin configuration for DIL package.

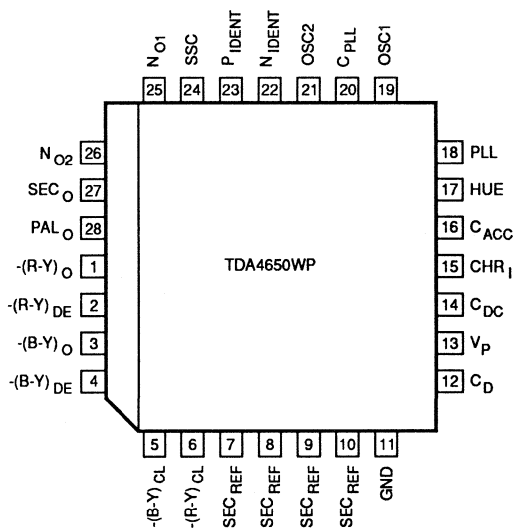


Fig.2(b) Pin configuration for PLCC package.

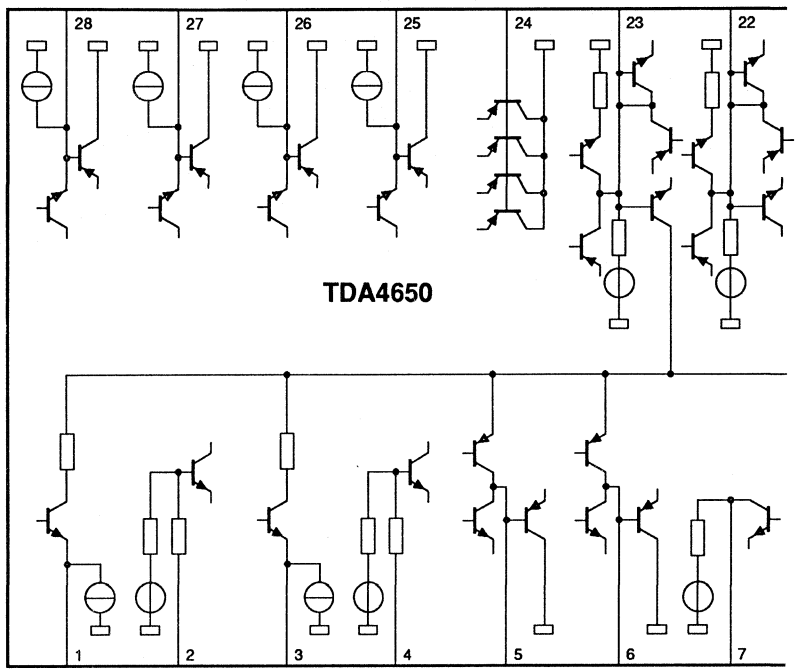


Fig.3a Internal circuits (continued in Fig.3b).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 13) –	13.2	V	
V_I	voltage range at pins 1, 3, 17 and 24 to 28	0	V_P	V
I_o	output current (pins 1 and 3)	–	–5	mA
$I_{i/o}$	input/output current (pins 25 to 28)	–	–5	μA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
$R_{th\ j\text{-}a}$	from junction to ambient in free air:			
	SOT117	–	37	K/W
	SOT261	–	70	K/W
P_{tot}	total power dissipation (SOT117)	–	1.4	W
	total power dissipation (SOT261)	–	1.1	W

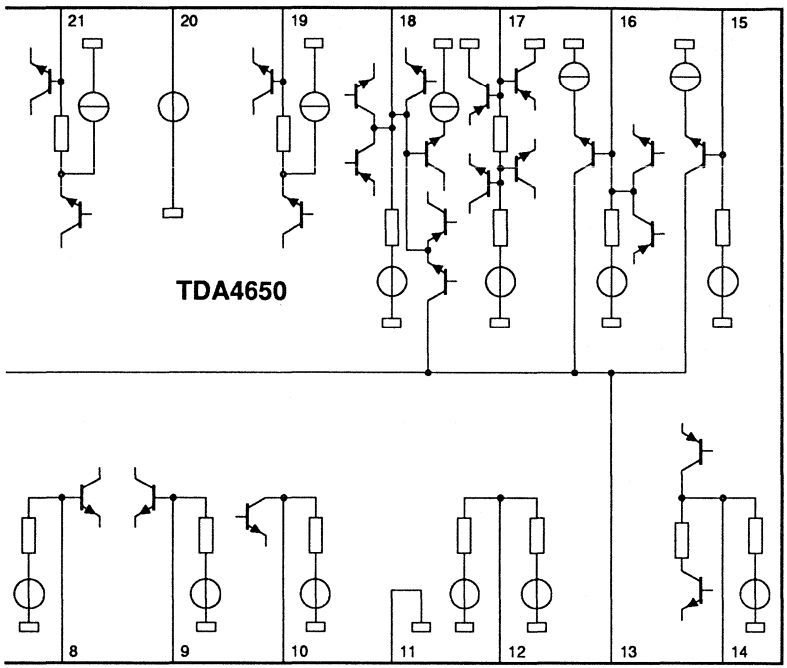


Fig.3b Internal circuits (continued from Fig.3a).

Multistandard colour decoder, with negative colour difference output signals

TDA4650

CHARACTERISTICS

All voltages are measured to GND (pin 11); V_P = 12 V; chrominance input signal $V_{15(p-p)}$ = 100 mV (with 75 % colour bar signal); 4 µs burst-blanking pulse and vertical blanking superimposed on super sandcastle pulse; T_{amb} = 25 °C; measured in test circuit of Fig. 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		10.8	12.0	13.2	V
I_P	supply current		50	60	80	mA
Chrominance part						
$V_{i(p-p)}$	input signal (pin 15) (peak-to-peak value)		20	100	400	mV
R_i	input resistance (pin 15)		7	10	13	kΩ
C_i	input capacitance (pin 15)		–	4	5	pF
Demodulator part (PAL/NTSC)						
$V_{1(p-p)}$	colour difference -(R-Y) output signal (peak-to-peak value)	at nominal phase of hue control	0.42	0.525	0.66	V
$V_{3(p-p)}$	colour difference -(B-Y) output signal (peak-to-peak value)	at nominal phase of hue control	0.53	0.665	0.84	V
V_1/V_3	ratio of colour difference signals (R-Y)/(B-Y) for NTSC	at nominal phase of hue control	0.75	0.79	0.83	
V_1/V_1	ratio of PAL/NTSC signals $(R-Y)_{PAL}/(R-Y)_{NTSC}$	at nominal phase of hue control	–	–	1	dB
m	signal linearity	$V_{1(p-p)}$ = 0.8 V – (R-Y)	0.8	–	–	
		$V_{3(p-p)}$ = 1.0 V – (B-Y)	0.8	–	–	
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars	–	–	10	mV
$V_{1,3(p-p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	10	mV
		8.87 MHz	–	–	30	mV
$Z_{1,3}$	output impedance		–	–	200	Ω
Demodulator part (SECAM); note 1						
$V_{1(p-p)}$	colour difference -(R-Y) output signal (peak-to-peak value)	every second line blanked	0.83	1.05	1.32	V
$V_{3(p-p)}$	colour difference -(B-Y) output signal (peak-to-peak value)	every second line blanked	1.06	1.33	1.67	V
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars; every second line blanked	–	–	10	mV
$V_{1,3(p-p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	30	mV
		8.87 MHz	–	–	30	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Demodulator part (SECAM) (continued); note 1						
$\Delta V_{1,3}/\Delta V_P$	shift of blanking levels relative to demodulated f_o levels		–	–	3	mV/V
$\Delta V_1/\Delta T$			–	0.16	–	mV/K
$\Delta V_3/\Delta T$			–	–0.25	–	mV/K
Hue control part						
ϕ	phase shift of reference carrier relative to phase at V_{17} = 3 V	V_{17} = 2 V	–30	–40	–	deg
	phase shift of reference carrier	V_{17} = 3 V	–	0	± 5	deg
	phase shift of reference carrier relative to phase at V_{17} = 3 V	V_{17} = 4 V	30	40	–	deg
V_{17}	internal bias voltage		–	3	–	V
	switching voltage for oscillator adjustment	burst OFF; colour ON	0	–	0.5	V
	switching voltage for forced colour ON	burst ON; colour ON	5.5	–	V_P	V
R_{17}	input resistance		3.8	5.0	6.2	kΩ
Reference oscillator (PLL); note 2						
$R_{19,21}$	input resistance		–	350	–	Ω
$C_{19,21}$	input resistance		–	–	10	pF
f_c	catching range	at 4.43 MHz	± 400	–	–	Hz
		at 3.57 MHz	± 330	–	–	Hz
Identification part switching voltages for chrominance filters and crystals: at pin 28 for PAL at pin 27 for SECAM at pin 26 for NTSC (3.58 MHz) at pin 25 for NTSC (4.43 MHz)						
$V_{28 \text{ to } 25}$	switching voltages	control voltage OFF state	–	0.05	0.5	V
		control voltage ON state; during scanning	2.35	2.45	2.55	V
		control voltage ON state; internal forced	5.6	5.8	6.0	V
		control voltage ON state; external forced	9.0	–	V_P	V
$I_{28 \text{ to } 25}$	output currents		–	–	–3	mA
t_d	delay time for system hold		2	–	3	cycles
	delay time for colour ON		2	–	3	cycles
	delay time for colour OFF		0	–	1	cycles
t_s	scanning time for each standard	note 3	–	4	–	cycles

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Super sandcastle pulse detector (note 4)						
V_{24}	input voltage pulse levels to separate V and H blanking pulses	pulse ON	1.3	1.6	1.9	V
		pulse OFF	1.1	1.4	1.7	V
	voltage pulse amplitude		2.0	2.5	3.0	V
	input voltage pulse levels to separate H blanking pulse	pulse ON	3.3	3.6	3.9	V
		pulse OFF	3.1	3.4	3.7	V
	voltage pulse amplitude		4.1	4.5	4.9	V
	input voltage pulse levels to separate burst gating pulse	pulse ON	6.2	6.6	7.0	V
		pulse OFF	6.0	6.4	6.8	V
	voltage pulse amplitude		7.7	–	V_P	V
	input voltage	during line scan	–	–	1.0	V
I_{24}	input current	during line scan	–	–	–100	µA

Notes to the characteristics

1. For the SECAM standard, amplitude and H/2 ripple content of the CD signals (R-Y) and (B-Y) depend on the characteristics of the external tuned circuit at pins 7 to 10. The resonant frequency of the external tuned circuit must be adjusted such that the demodulated f_o voltage level is zero in the -(B-Y) output channel at pin 3.
   Now it is possible to adjust the quality of the external circuit such that the demodulated f_o voltage level is zero in the -(R-Y) output channel at pin 1. If necessary, the f_o voltage level in the -(B-Y) output channel must be readjusted to zero by the coil of the tuned circuit.
   The external capacitors at the pins 2 and 4 (220 pF each) are matched to the internal resistances of the de-emphasis network such that every alternate scanned line is blanked.
2. The f_o frequencies of the 8.8 MHz crystal at pin 21, and the 7.2 MHz crystal at pin 19, can be adjusted when the voltage at pin 17 is less than 0.5 V (burst OFF), thus providing double subcarrier frequencies of the chrominance signal.
3. The inquiry sequence for the standard is:
   PAL – SECAM – NTSC (3.58 MHz) – NTSC (4.43 MHz).
   PAL has priority with respect to SECAM, etc.
4. The super sandcastle pulse is compared with three internal threshold levels which are proportional to V_P.

Multistandard colour decoder, with negative colour difference output signals

TDA4650

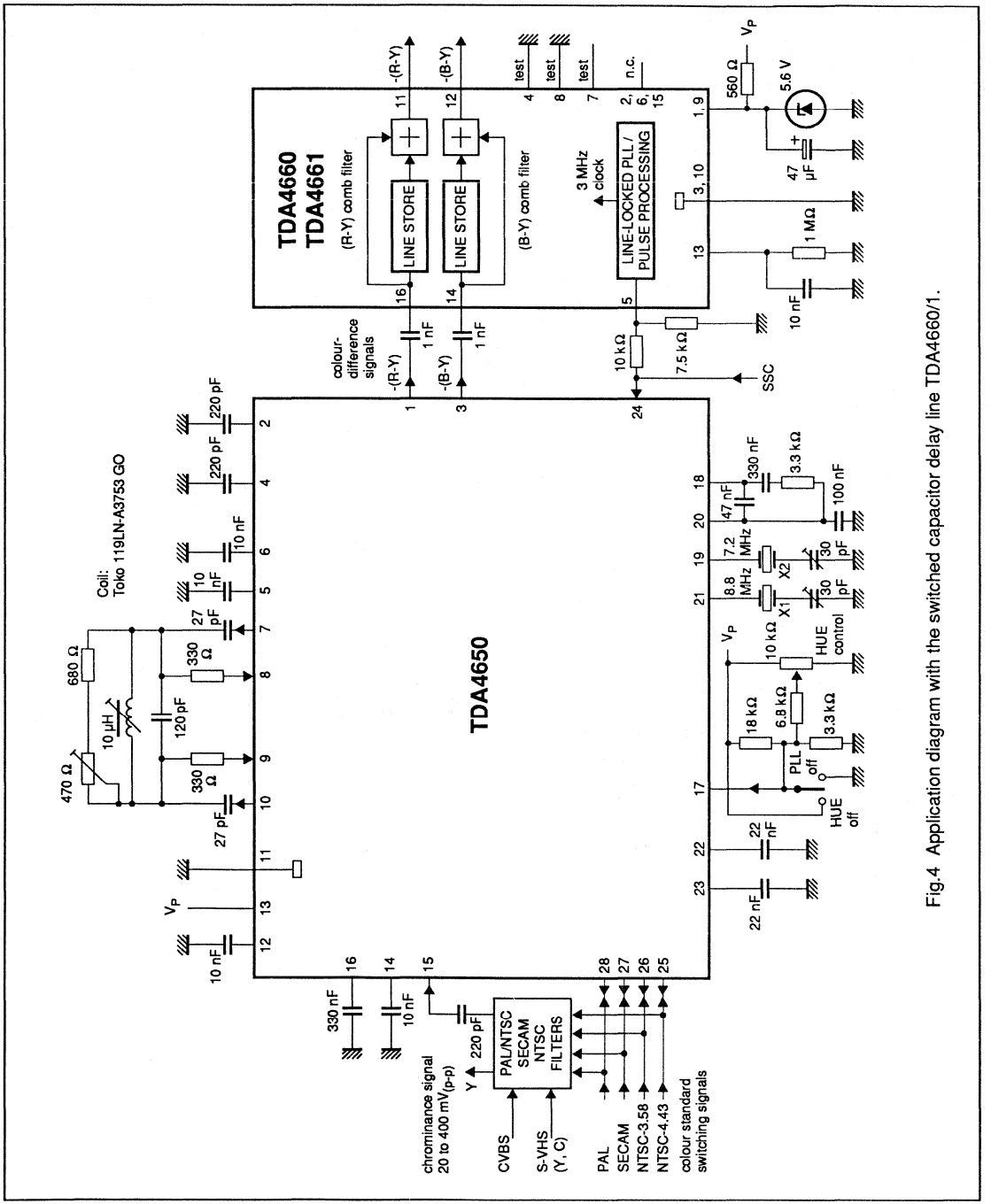


Fig.4 Application diagram with the switched capacitor delay line TDA4660/1.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1991

TDA4661
baseband delay line

FEATURES

- Two comb filters, using the switched-capacitor technique, for one line delay time (64 µs)
- Adjustment-free application
- No crosstalk between SECAM colour carriers (diaphoty)
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals (±(R–Y) and ±(B–Y))
- VCO without external components
- 3 MHz internal clock signal derived from a 6 MHz VCO, line-locked by the sandcastle pulse (64 µs line)
- Sample-and-hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Addition of delayed and non-delayed output signals
- Output buffer amplifiers
- comb filtering functions for NTSC colour-difference signals to suppress cross-colour

GENERAL DESCRIPTION

The TDA4660 is an integrated baseband delay line circuit with one line delay. It is suitable for decoders with colour-difference signal outputs ±(R–Y) and ±(B–Y).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)	4.5	5	6	V
V_{P2}	digital supply voltage (pin 1)	4.5	5	6	V
$I_{P\,tot}$	total supply current	-	4.7	9.4	mA
V_i	±(R–Y) input signal PAL/NTSC (peak-to-peak value, pin 16)	-	525	-	mV
	±(B–Y) input signal PAL/NTSC (peak-to-peak value, pin 14)	-	665	-	mV
	±(R–Y) input signal SECAM (peak-to-peak value, pin 16)	-	1.05	-	V
	±(B–Y) input signal SECAM (peak-to-peak value, pin 14)	-	1.33	-	V
G_v	gain V_o / V_i of colour-difference output signals				
	V_{11} / V_{16} for PAL and NTSC	5.5	6.0	6.5	dB
	V_{12} / V_{14} for PAL and NTSC	5.5	6.0	6.5	dB
	V_{11} / V_{16} for SECAM	–0.5	0	+0.5	dB
	V_{12} / V_{14} for SECAM	–0.5	0	+0.5	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4661	16	DIL (IDF)	plastic	SOT38-4
TDA4661T	16	mini-pack	plastic	SOT109A

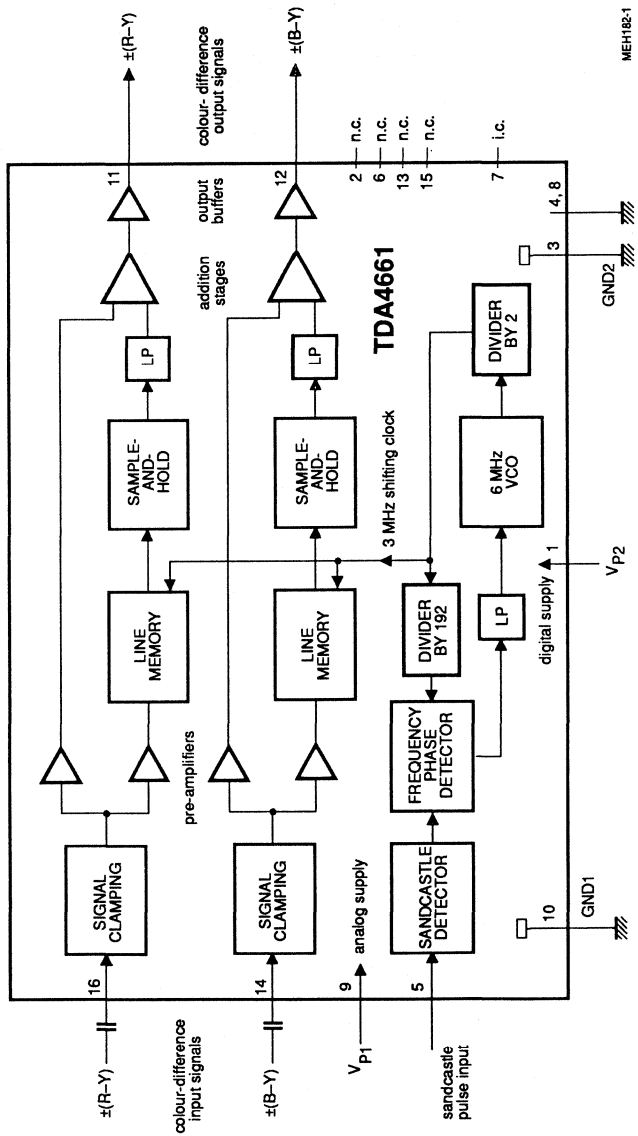


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P2}	1	+5 V supply voltage for digital part
n.c.	2	not connected
GND2	3	ground for digital part (0 V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
i.c.	7	internally connected
i.c.	8	internally connected
V_{P1}	9	+5 V supply voltage for analog part
GND1	10	ground for analog part (0 V)
$V_{o\ (R-Y)}$	11	±(R–Y) output signal
$V_{o\ (B-Y)}$	12	±(B–Y) output signal
n.c.	13	not connected
$V_{i\ (B-Y)}$	14	±(B–Y) input signal
n.c.	15	not connected
$V_{i\ (R-Y)}$	16	±(R–Y) input signal

PIN CONFIGURATION

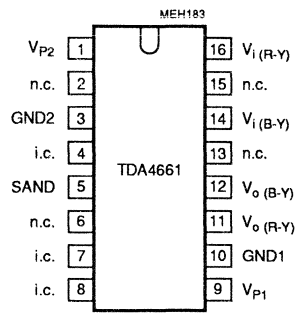


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 9)	–0.5	+7	V
V_{P2}	supply voltage (pin 1)	–0.5	+7	V
V_n	voltage on pins 5, 11, 12,14 and 16	–0.5	V_P	V
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±500	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j-a}$	from junction-to-ambient in free air			
	for DIL16	-	80	K/W
	for SO16	-	220	K/W

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 5.0 V; input signals as specified in characteristics with 75% colour bar; super-sandcastle frequency of 15.625 kHz; T_{amb} = 25 °C, and measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (analog part, pin 9)		4.5	5	6	V
V_{P2}	supply voltage (digital part, pin 1)		4.5	5	6	V
I_{P1}	supply current		-	0.7	1.4	mA
I_{P2}	supply current		-	4	8	mA
Colour-difference input signals						
V_i	input signal (peak-to-peak value)					
	±(R–Y) PAL and NTSC (pin 16)		-	525	-	mV
	±(B–Y) PAL and NTSC (pin 14)		-	665	-	mV
	±(R–Y) SECAM (pin 16)	note 1	-	1.05	-	V
	±(B–Y) SECAM (pin 14)	note 1	-	1.33	-	V
$V_{i\,max}$	maximum symmetrical input signal (peak-to-peak value)	before clipping				
	±(R–Y) or ±(B–Y) for PAL and NTSC		1	-	-	V
	±(R–Y) or ±(B–Y) for SECAM		2	-	-	V
$R_{14,16}$	input resistance		-	-	40	kΩ
$C_{14,16}$	input capacitance		-	-	10	pF
$V_{14,16}$	input clamping voltage	proportional to V_P	1.4	1.5	1.6	V
Colour-difference output signals						
V_o	output signal (peak-to-peak value)	all standards				
	±(R–Y) on pin 11		-	1.05	-	V
	±(B–Y) on pin 12)		-	1.33	-	V
V_{11}/V_{12}	ratio of output amplitudes at equal input signals	$V_{i\,14,16}$ = 1.33 V (p-p)	–0.4	0	+0.4	dB
$V_{11,12}$	DC output voltage	proportional to V_P	2.55	2.75	3.10	V
$R_{11,12}$	output resistance		-	330	400	Ω
G_v	gain for PAL and NTSC	ratio V_o / V_i	5.5	6.0	6.5	dB
	gain for SECAM (ratio V_o / V_i)	ratio V_o / V_i	–0.5	0	+0.5	dB
V_n/V_{n+1}	ratio of output signals on pins 11 and 12 for adjacent time samples at constant input signals	$V_{i\,14,16}$= 1.33 V (p-p) SECAM signals	–0.1	0	+0.1	dB
V_n	noise voltage (RMS value, pins 11 and 12)	$V_{i\,14,16}$ = 0; note 2	-	-	1.2	mV
S/N(W)	weighted signal-to-noise ratio	V_o = 1 V (p-p); f = tbf	-	54	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_d	delay of delayed signals		63.94	64.0	64.06	µs
	delay of non-delayed signals		20	40	60	ns
t_{tr}	transient time of delayed signal on pins 11 respectivily 12	300 ns transient of SECAM signal	-	350	-	ns
	transient time of non-delayed signal on pins 11 respectivily 12	300 ns transient of SECAM signal	-	320	-	ns
Sandcastle pulse input (pin 5)						
f_{BK}	burst-key frequency		14.2	15.625	17.0	kHz
V_5	top pulse voltage	note 3	3	-	7	V
V_{slice}	internal slicing level		V_5 –1.0	-	V_5 –0.5	V
I_5	input current		-	-	10	µA
C_5	input capacitance		-	-	10	pF

Notes to the characteristics

1. The signal must be blanked line-sequentially. The blanking level must be equal to the non-colour signal.
2. Noise voltage at f = 10 kHz to 1 MHz; $V_{i\ 14,16} = 0$ ($R_S < 300\ \Omega$)
3. The leading edge of the burst-key pulse is used for timing.

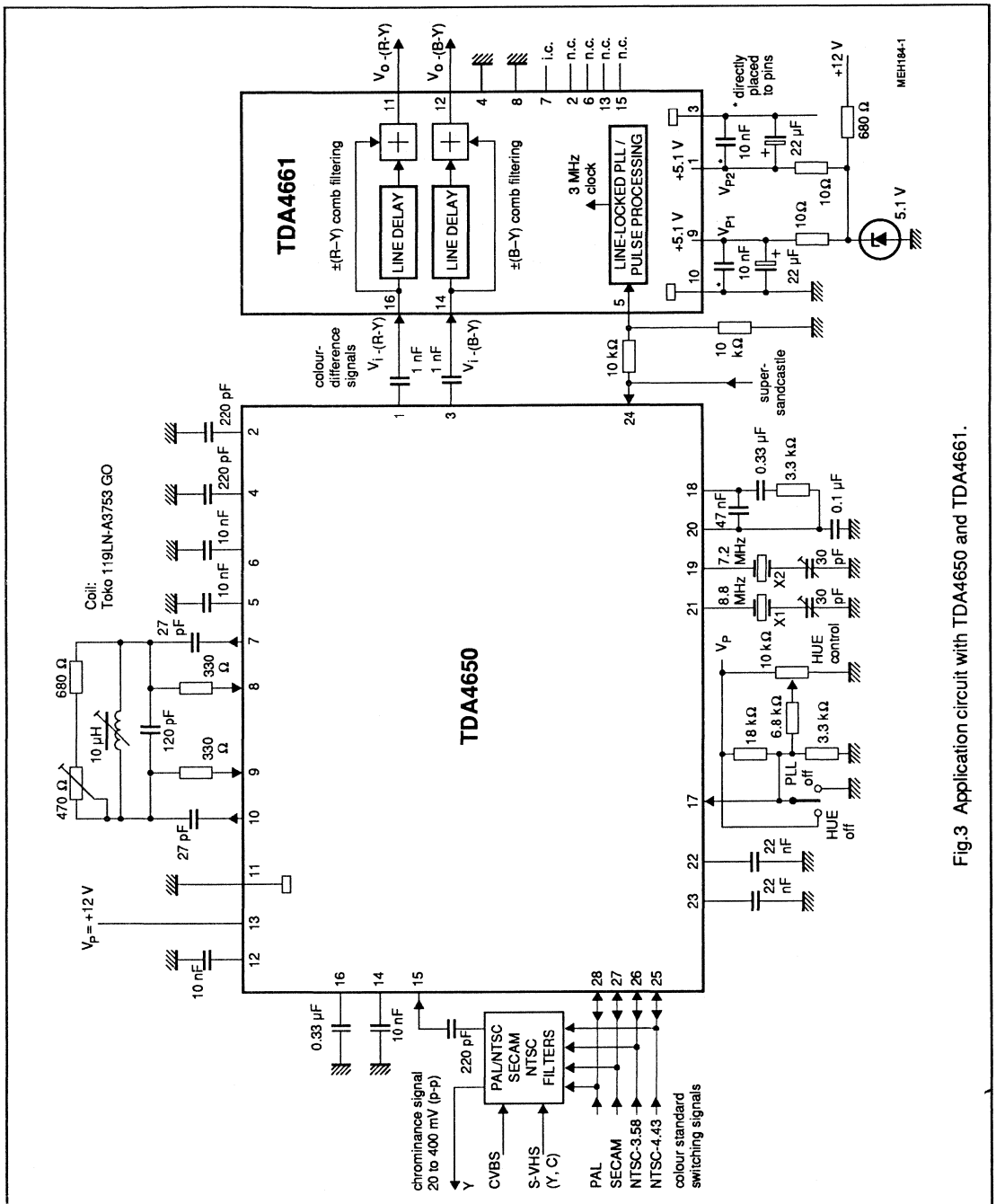


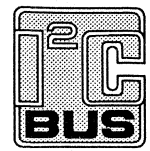
Fig.3 Application circuit with TDA4650 and TDA4661.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1991
supersedes data of August 1990	

TDA4670

Picture signal improvement (PSI) circuit



FEATURES

- Luminance signal delay from 20 ns up to 1100 ns (minimum step 45 ns)
- Luminance signal peaking with symmetrical overshoots selectable
- 2.6 or 5 MHz peaking centre frequency and degree of peaking selectable (–3, 0, +3 and +6 dB)
- Noise reduction by coring selectable
- Handles negative as well as positive colour-difference signals
- Colour transient improvement (CTI) selectable to decrease the colour-difference signal transient times to those of the high frequency luminance signals
- 5 or 12 V sandcastle input voltage selectable
- All controls selected via the I²C-bus
- Timing pulse generation for clamping and delay time control synchronized by sandcastle pulse
- Automatic luminance signal delay correction using a control loop
- Luminance and colour-difference input signal clamping with coupling-capacitor
- +4.5 to 8.8 V supply voltage range
- Minimum of external components

GENERAL DESCRIPTION

The TDA4670 delays the luminance signal and improves colour-difference signal transients. Additional, the luminance signal can be improved by peaking and noise reduction (coring).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 1 and 5)	4.5	5	8.8	V
I_P	total supply current	31	41	52	mA
$t_{d\,Y}$	Y signal delay time	20	-	1130	ns
$V_{i\,VBS}$	composite Y input signal (peak-to-peak value, pin 16)	-	450	640	mV
$V_{i\,CD}$	colour-difference input signal (peak-to-peak value)				
	±(R–Y) on pin 3	-	1.05	1.48	V
	±(B–Y) on pin 7	-	1.33	1.88	V
G_Y	gain of Y channel	-	–1	-	dB
G_{CD}	gain of colour-difference channel	-	0	-	dB
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4670	18	DIL	plastic	SOT102

Picture signal improvement (PSI) circuit

TDA4670

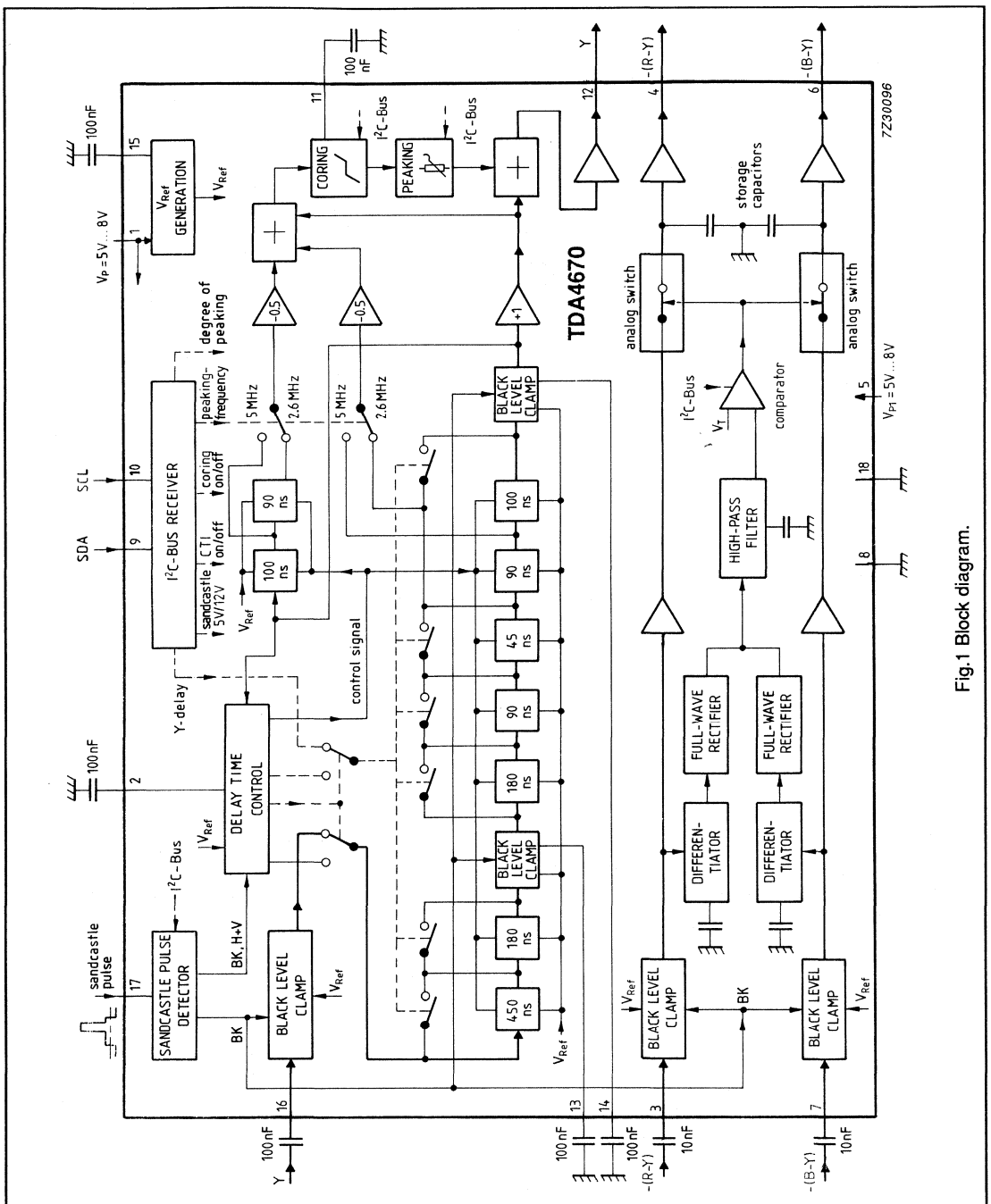


Fig.1 Block diagram.

Picture signal improvement (PSI) circuit

TDA4670

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	positive supply voltage 1
C_{DL}	2	capacitor of delay time control
$V_{i\,(R-Y)}$	3	±(R–Y) colour-difference input signal
$V_{o\,(R-Y)}$	4	±(R–Y) colour-difference output signal
V_{P2}	5	positive supply voltage 2
$V_{o\,(B-Y)}$	6	±(B–Y) colour-difference output signal
$V_{i\,(B-Y)}$	7	±(B–Y) colour-difference input signal
GND2	8	ground 2 (0 V)
SDA	9	I²C-bus data line
SCL	10	I²C-bus clock line
C_{COR}	11	coring capacitor
$V_{o\,Y}$	12	delayed luminance output signal
C_{CLP1}	13	black level clamping capacitor 1
C_{CLP2}	14	black level clamping capacitor 2
C_{ref}	15	capacitor of reference voltage
$V_{i\,Y}$	16	luminance input signal
SAND	17	sandcastle pulse input
GND1	18	ground 1 (0 V)

PIN CONFIGURATION

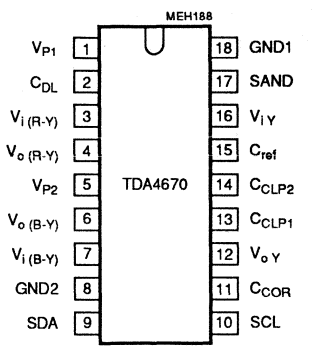


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA4670 contains luminance signal processing and colour-difference signal processing.The luminance signal section comprises a variable, integrated luminance delay line with luminance signal peaking and a noise reduction by coring.
The colour-difference section consists of a transient improvement circuit to decreases the rise and fall times of the colour-difference signal transients.
All functions and parameters are controlled via the I²C-bus.

Y-signal path

The video and blanking signal is AC-coupled to the input pin 16. Its black porch is clamped to a DC reference voltage to ensure fitting to the operating range of the luminance delay stage.
The luminance delay line consists of all-pass filter sections with delay times of 45, 90, 100, 180 and 450 ns (Fig.1). The luminance signal delay is controlled via the I²C-bus in steps of 45 ns in the range of 20 to 1100 ns, this ensures that the maximum delay difference between the luminance and colour-difference signals is ±22.5 ns.
An automatic luminance delay time adjustment in an internal control loop (with the horizontal frequency as a reference) is used to correct changes in the delay time, due to component tolerances. The control loop is automatically enabled between the burst-key pulses of lines 16 (330) and 17 (331) during the vertical blanking interval. The control voltage is stored in the capacitor C_{DL} at pin 2.
The peaking section is using a transversal filter circuit with selectable centre frequencies of 2.6 and 5.0 MHz.
It provides selectable degrees of peaking of –3, 0, +3 and +6 dB and a noise reduction by coring, which attenuates the high-frequency noise introduced by peaking.
The output buffer stage ensures a low-ohmic VBS output signal on pin 12 (< 160 Ω). The gain of the luminance signal path from pin 16 to pin 12 is unity.

An oscillation signal of the delay time control loop is present on output pin 12 instead of the VBS signal during the vertical blanking interval in lines 16 (330) to 18 (332). Therefore, this output signal should not be applied for synchronization.

Colour-difference signal paths

The colour-difference input signals (on pins 3 and 7) are clamped to a reference voltage.

Each colour-difference signal is fed to a transient detector and to an analog signal switch with an attached voltage storage stage.
The transient detectors consist of differentiators and full-wave rectifiers. The output voltages of both transient detectors are added and then compared in a comparator. This comparator controls both following analog signal switches simultaneously. The analog signal switches are in open position at a certain value of transient time; then the held value (held by storage capacitors) is applied to the outputs. The switches close to accept rapidly the actual signal levels at the end of these transients. The improved transient time is approximately 100 ns long independent of the input signal transient time.

Colour-difference paths are independent of the input signal polarity and have a gain of unity .

The CTI functions are switched on and off via the I^2C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134). V_{P1} and V_{P2} as well as GND1 and GND 2 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 1)	0	8.8	V
V_{P2}	supply voltage (pin 5)	0	8.8	V
P_{tot}	total power dissipation	0	0.97	W
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for pins 9 and 10	- -	+300 –500	V V
	for other pins	-	±500	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	-	82	K/W

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; nominal video amplitude $V_{VB} = 315$ mV; $t_H = 64$ µs; $t_{BK} = 4$ µs (burst key); $T_{amb} = 25$ °C and measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage range (pin 1)		4.5	5	8.8	V
V_{P2}	supply voltage range (pin 5)		4.5	5	8.8	V
I_P	total supply current		31	41	52	mA
Y-signal path						
$V_{i\,Y}$	VBS input signal on pin 16 (peak-to-peak value)		-	450	640	mV
V_{16}	black level clamping voltage		-	3.1	-	V
I_{16}	input current	during clamping	±95	-	±190	µA
		outside clamping	-	-	±0.1	µA
R_{16}	input resistance	outside clamping	5	-	-	MΩ
C_{16}	input capacitance		-	3	10	pF
$t_{d\,Y}$	maximum Y delay time	set via I²C-bus	1070	1100	1130	ns
	minimum Y delay time		-	20	-	ns
$\Delta t_{d\,Y}$	minimum delay step	set via I²C-bus	40	45	50	ns
	group delay time difference	f = 0.5 to 5 MHz maximum delay	-	0	±25	ns
	delay time difference between Y and colour-difference signals	Y delay; CTI and peaking off	70	100	130	ns
$t_{d\,peak}$	minimum delay time for peaking		185	215	245	ns
G_Y	VBS signal gain measured on output pin 12 (composite signal, peak-to-peak value)	V_o / V_i; f = 500 kHz; maximum delay	–2	–1	0	dB
I_{12}	output current (emitter-follower with constant current source)	source current	–1	-	-	mA
		sink current	0.4	-	-	mA
R_{12}	output resistance		-	-	160	Ω
f	frequency response for	maximum delay				
	f = 0.5 to 3 MHz		–2	–1	0	dB
	f = 0.5 to 5 MHz		–4	–3	–1	dB
LIN	signal linearity for	a_{min} / a_{max}				
	video contents of 315 mV (p-p)	V_{VBS} = 450 mV (p-p)	0.85	-	-	-
	video contents of 450 mV (p-p)	V_{VBS} = 640 mV (p-p)	0.60	-	-	-

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Luminance peaking, selected via I²C-bus						
f_{peak}	peaking frequency	f_{C1}; LCF-bit = 0	4.5	5	5.5	MHz
		f_{C2}; LCF-bit = 1	2.3	2.6	2.9	MHz
V_{peak}	peaking amplitude for grade of peaking (f_C amplitude over 0.5 MHz amplitude)					
	selectable values		-	–3	-	dB
			-	0	-	dB
			-	+3	-	dB
			-	+6	-	dB
	limitation of peaking (positive amplitude of correction signal referred to 315 mV)		-	20	-	%
V_n	noise voltage on pin 12 (RMS value)	without peaking f = 0 to 5 MHz	-	-	1	mV
COR	coring of peaking (coring part referred to 315 mV)	COR-bit = 1	-	20	-	%
Colour-difference paths measured with transient times $t_r = t_f = 1$ µs; $t_{p\,H} \geq 1$ µs; V_i = 1.33 V (p-p) on pins 3 and 7 and with burst key pulse t_{BK} = 4 µs.						
$V_{i\,CD}$	±(R–Y) input signal (peak-to-peak values, pin 3)	75% colour bar;	-	1.05	1.48	V
	±(B–Y) input signal (peak-to-peak values, pin 7)	75% colour bar	-	1.33	1.88	V
	input transient sensitivity	$V_{3,7}$ /dt	0.15	-	-	V/µs
$V_{3,7}$	internal clamping voltage level		-	2.45	-	V
$I_{3,7}$	input current	outside clamping	-	-	±1	µA
		during clamping	±100	-	±190	µA
$C_{3,7}$	input capacitance		-	6	12	pF
$V_{4,6}$	DC output voltage		-	2	-	V
$\Delta V_{4,6}$	output offset voltage	$R_S \leq 300\ \Omega$; note 1	-	-	±5	mV
		during and after storage time	-	-	±18	mV
V_{spike}	spurious spike signals on pins 4 and 6	$R_S \leq 300\ \Omega$; note 1	-	-	±30	mV
$I_{4,6}$	output current (emitter-follower with constant current source)	source current	–1	-	-	mA
		sink current	0.4	-	-	mA
$R_{4,6}$	output resistance		-	-	100	Ω
G_v	signal gain in each path	V_o / V_i	–1	0	+1	dB
ΔG_v	gain difference –(R–Y) / –(B–Y)		-	0	±0.3	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LIN	signal linearity	a_{min} / a_{max}				
	for nominal signal	V_i = 1.33 V (p-p)	0.90	-	-	
	for +3 dB signal	V_i = 1.88 V (p-p)	0.65	-	-	
ΔV_o	signal reduction at higher frequency (output signal ratio V_i / V_o)	signal with t_{pH} = 50 ns; $t_r = t_f$ = 1 µs	−1.5	-	-	dB
Sandcastle pulse, input voltage selectable via I²C-bus						
V_{17}	input voltage threshold for H and V sync	SC5-bit = 0 (12 V)	1.1	1.5	1.9	V
	input voltage threshold for burst	SC5-bit = 0 (12 V)	5.5	6.5	7.5	V
	input voltage threshold for H and V sync	SC5-bit = 1 (5 V)	1.1	1.5	1.9	V
	input voltage threshold for burst	SC5-bit = 1 (5 V)	3.0	3.5	4.0	V
R_{17}	input resistance	12 V input level	30	40	50	kΩ
		5 V input level	15	20	25	kΩ
C_{17}	input capacitance		-	4	8	pF
t_{BK}	burst-key pulse width		3.0	4.0	4.6	µs
t_d	leading edge delay for clamping pulse	referred to t_{BK}	-	1	-	µs
n_p	number of required burst-key pulses vertical blanking interval	note 2	4	-	31	
I²C-bus control, SDA and SCL						
V_{IH}	input voltage HIGH on pins 9 and 10		3	-	5	V
V_{IL}	input voltage LOW		0	-	1.5	V
$I_{9,10}$	input current		-	-	±10	µA
V_9	output voltage at acknowledge on pin 9	I_9 = 3 mA	-	-	0.4	V
I_{ACK}	output current at acknowledge on pin 9	sink current	3	-	-	mA

Notes to the characteristics

1. Crosstalk on output, measured in the unused channel when the other channel is provided with a nominal input signal (CTI active).
2. A number of more than 31 burst-key pulses repeats the counter cycle of delay time control.

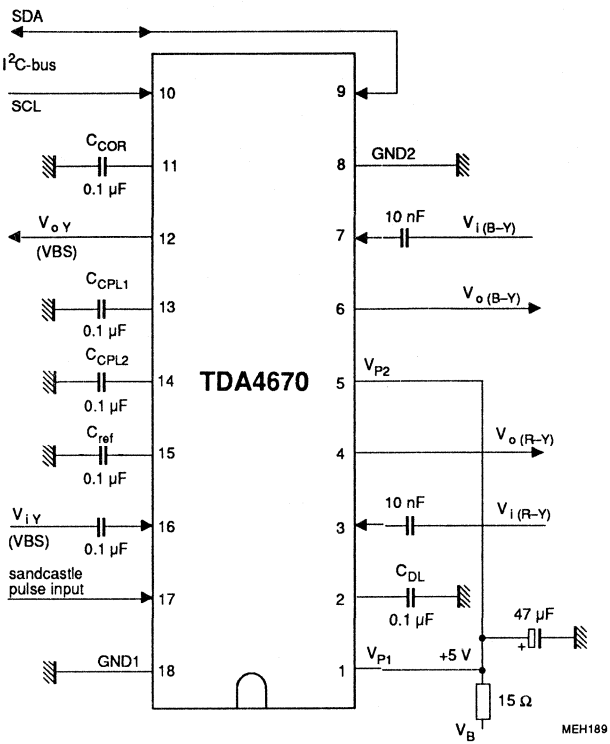


Fig.3 Test and application circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S	=	start condition
SLAVE ADDRESS	=	**1000 100X**
A	=	acknowledge, generated by the slave
SUBADDRESS	=	subadress byte, Table 1
DATA	=	data byte, Table 1
P	=	stop condition
X	=	read/write control bit X = 0, to write (the circuit is slave receiver only)

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus transmission

function	subaddress byte	data byte D7	D6	D5	D4	D3	D2	D1	D0
Y delay / CTI / SC peaking and coring	0 0 0 1 0 0 0 0	0	SC5	CTI	DL4	DL3	DL2	DL1	DL0
	0 0 0 1 0 0 0 1	COR	PEAK	LCF	0	0	0	PCON1	PCON0

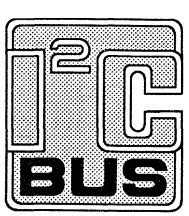
Function of the bits:

DL0	set delay in luminance channel:	1 = 45 ns;	0 = 0 ns
DL1		1 = 90 ns;	0 = 0 ns
DL2		1 = 180 ns;	0 = 0 ns
DL3		1 = 180 ns;	0 = 0 ns
DL4		1 = 450 ns;	0 = 0 ns
CTI	set colour transient improvement:	1 = active	0 = inactive
SC5	select sandcastle pulse voltage:	1 = 5 V	0 = 12 V
LCF	set peaking frequency response:	1 = 2.6 MHz	0 = 5.0 MHz
PEAK	set peaking delay:	1 = active	0 = inactive
COR	set coring control:	1 = active	0 = inactive

PCON — set peaking amplification:

PCON1	PCON0	grade of peaking
0	0	–3 dB
0	1	0 dB
1	0	+3 dB
1	1	+6 dB

Remarks to the subaddress bytes
Hex subaddresses 00 to 0F are reserved for colour decoders and RGB processors.
Subaddresses 10 and 11 only are acknowledged .
General call address is not acknowledged.
Power-on reset: D7 to D1 bits of data bytes are set to 0 , D0 bit is set to 1.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

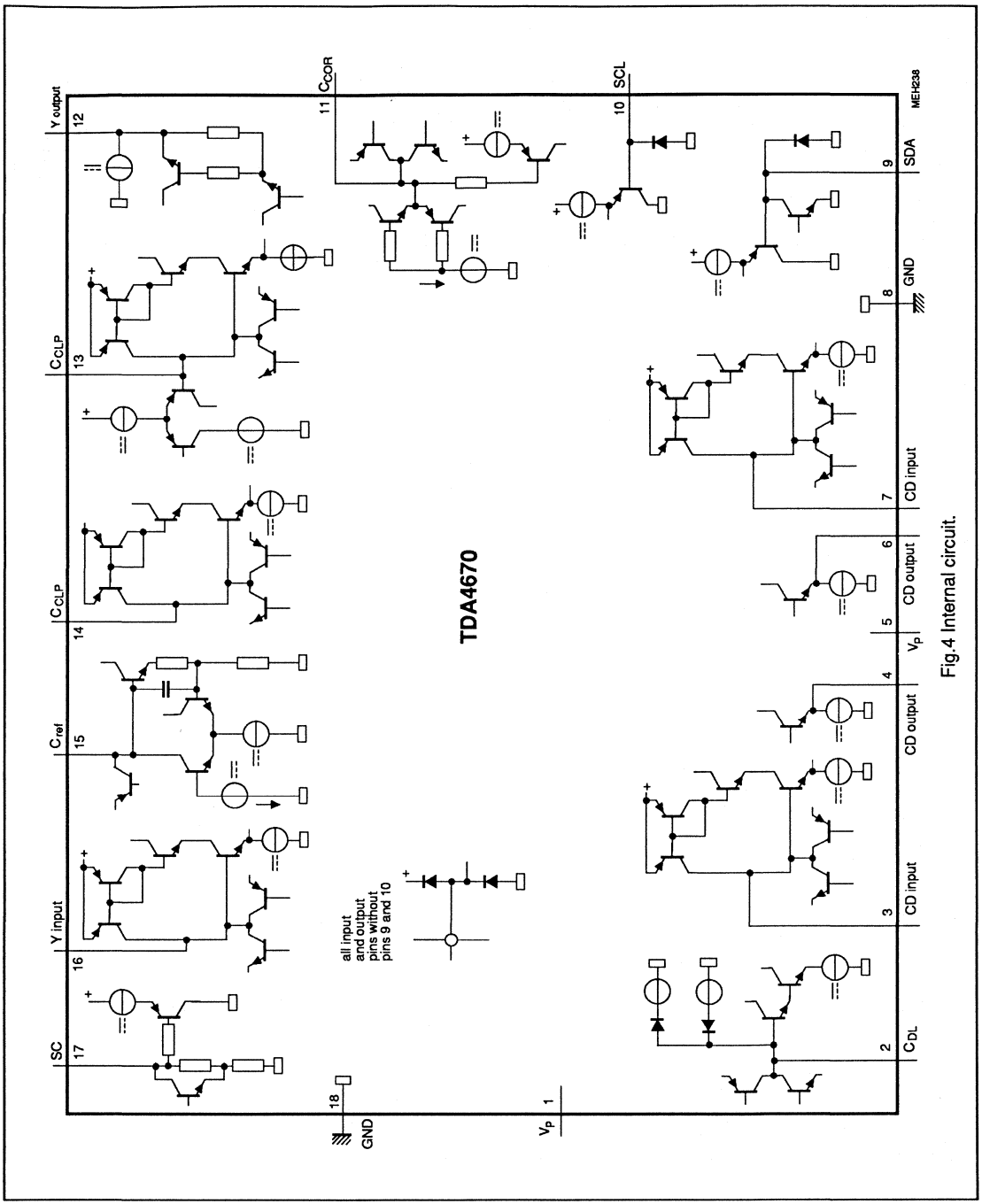


Fig.4 Internal circuit.

Data sheet	
status	Preliminary specification
date of issue	March 1991

TDA4680

Video processor, with automatic cut-off and white level control

FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour-difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two fully-controlled, analog RGB inputs, selected either by fast switch signals or via I²C-bus
- Saturation, contrast and brightness adjustment via I²C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, horizontal and vertical synchronization, cut-off and white level timing pulses
- Automatic cut-off control with picture tube leakage current compensation
- Software-based automatic white level control or fixed white levels via I²C-bus
- Cut-off and white level measurement pulses in the last 4 lines of the vertical blanking interval (I²C-bus selection for PAL, SECAM, or NTSC, PAL-M)
- Increased RGB signal bandwidths for progressive scan and 100 Hz operation (selected via I²C-bus)
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting

(continued)

DESCRIPTION

The TDA4680 is a monolithic, integrated circuit with a colour-difference interface for video processing in TV receivers.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	85	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse: H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse: H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24,22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature range	0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4680	28	DIL	plastic	SOT117
TDA4680WP	28	PLCC	plastic	SOT261

Video processor, with automatic cut-off and white level control

TDA4680

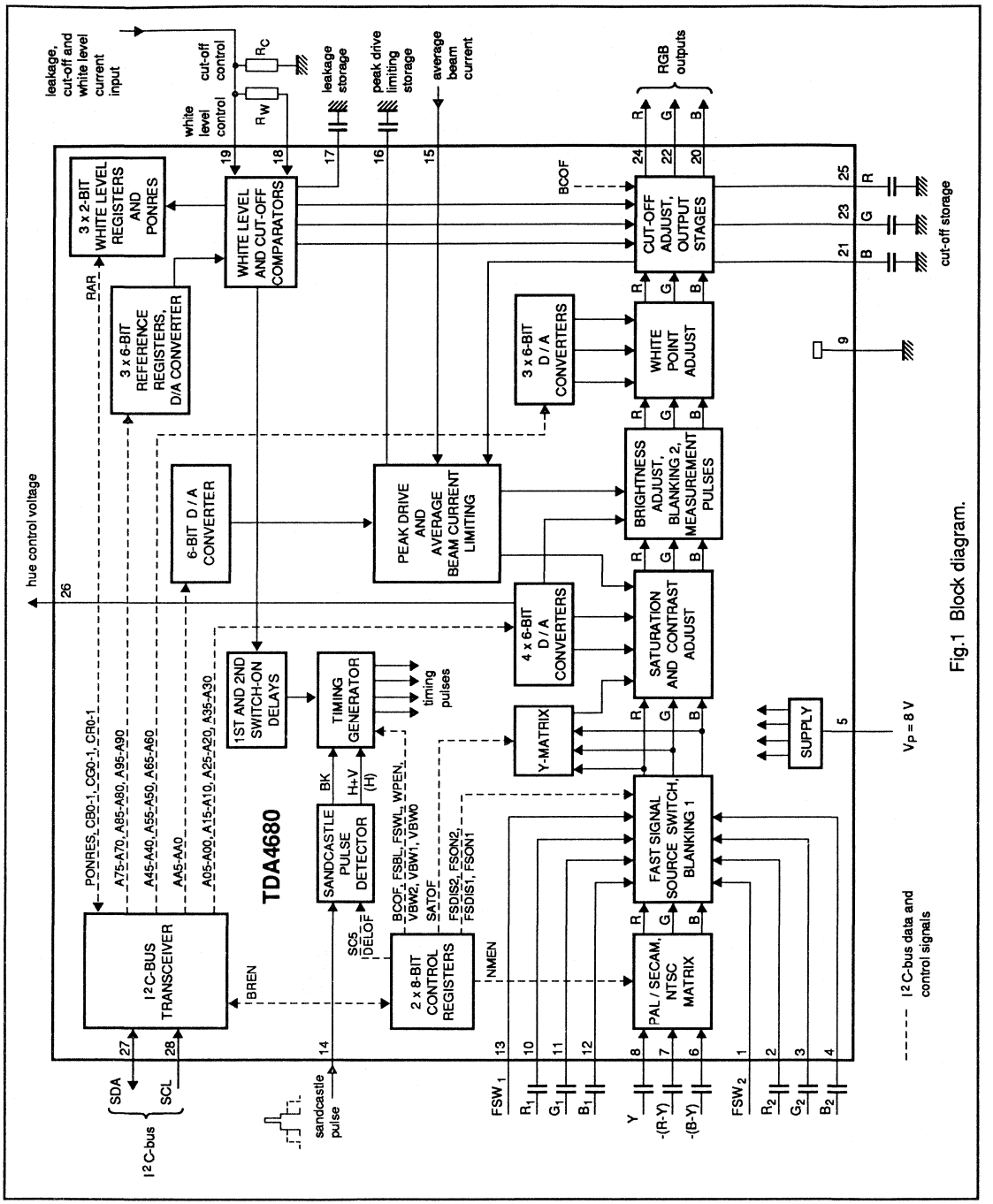


Fig.1 Block diagram.

Video processor, with automatic cut-off and white level control

TDA4680

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
-(B-Y)	6	colour difference input -(B-Y)
-(R-Y)	7	colour difference input -(R-Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input

SYMBOL	PIN	DESCRIPTION
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
WI	18	white level measurement input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input/output
SCL	28	I^2C-bus serial clock input

PIN CONFIGURATIONS

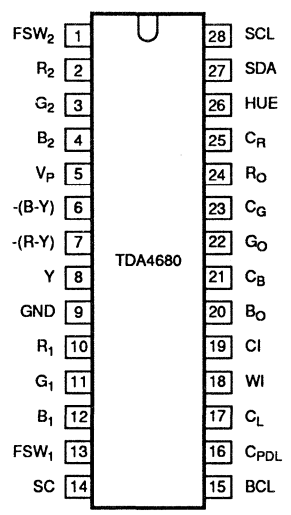


Fig.2(a) Pin configuration for DIL package.

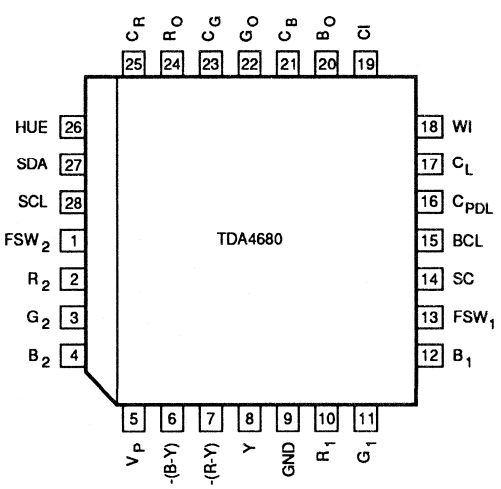


Fig.2(b) Pin configuration for PLCC package.

Video processor, with automatic cut-off and white level control

TDA4680

FEATURES (continued)

- PAL/SECAM or NTSC matrix selection via I²C-bus
- Three adjustable reference voltage levels (via I²C-bus) for automatic cut-off and white level control
- Emitter-follower RGB output stages to drive the video output stages
- Hue control output for the TDA4555 or TDA4650

DESCRIPTION (continued)

Its primary function is to process the luminance and colour-difference signals from multistandard colour decoders, TDA4650/TDA4660 or TDA4555, Colour Transient Improvement (CTI) IC, TDA4565, Picture Signal Improvement (PSI) IC, TDA4670, or from a Feature Module.

The required input signals are:

- luminance and negative colour-difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I²C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator; both inputs are fully-controlled internally . The TDA4680 includes full I²C-bus control of all parameters and functions with automatic cut-off and white level control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

I²C-BUS CONTROL

The I²C-bus transmitter/receiver provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- RGB reference voltage levels
- peak drive limiting
- selection of the vertical blanking interval and measurement lines for cut-off and white level control according to transmission standard
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables/disables input clamping pulse delay
- enables/disables white level control
- enables cut-off control/ enables output clamping
- enables/disables full screen white level
- enables/disables full screen black level
- selects either PAL/SECAM or NTSC matrix
- enables saturation adjust/ enables nominal saturation
- enables/disables synchronization of the execution of I²C-bus commands with the vertical blanking interval
- reads the result of the comparison of the nominal and actual RGB signal levels for automatic white level control.

I²C-BUS TRANSMITTER / RECEIVER AND DATA TRANSFER

I²C-bus specification

The I²C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits/receives data from the I²C-bus transceiver in the TDA4680 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit. A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I²C-bus receiver

(microcontroller write mode)

Each transmission to/from the I²C-bus transceiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This consists of the module address, 1000100_2 for the TDA4680, plus the R/WN bit (see Fig.3). When the TDA4680 is a slave receiver

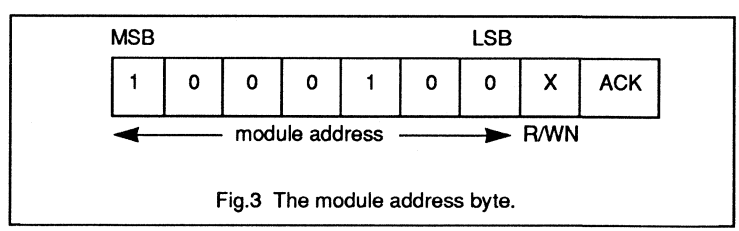


Fig.3 The module address byte.

Table 1 Sub-address (SAD) and data bytes

FUNCTION	SAD	MSB			DATA BYTE				LSB
	(Hex)	7	6	5	4	3	2	1	0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Red level reference	07	0	0	A75	A74	A73	A72	A71	A70
Green level reference	08	0	0	A85	A84	A83	A82	A81	A80
Blue level reference	09	0	0	A95	A94	A93	A92	A91	A90
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control Register 1	0C	SC5	DELOF	BREN	WPEN	NMEN	VBW2	VBW1	VBW0
Control Register 2	0D	SATOF	FSWL	FSBL	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

(R/WN = 0) the module address byte is 10001000_2 (88 Hex). When the TDA4680 is a slave transmitter (R/WN = 1) the module address byte is 10001001_2 (89 Hex).

The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.4 and Fig.5. *Without auto-increment* (BREN = 0 or 1) the module address (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.4).

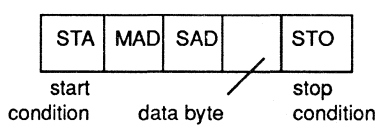


Fig.4 Data transmission without auto-increment (BREN = 0 or 1).

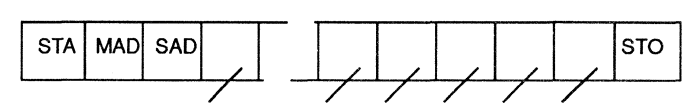


Fig.5 Data transmission with auto-increment (BREN = 0).

Auto-Increment

The auto-increment format enables quick slave receiver initialization by one transmission, when the I^2C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.

If the auto-increment format is

selected, the MAD byte is followed by a SAD byte and by the data bytes of consectutive sub-addresses (Fig.5).

All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 0B, 0E and 0F are treated as legal but have no effect. Sub-addresses outside the range 00 and 0F are acknowledged by the device but neither auto-increment nor any other internal operation takes place.

Sub-addresses are stored in the TDA4680 to address the following parameters and functions, see Table 1:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- RGB reference voltage levels
- peak drive limitting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control Register 1

VBWx (Vertical Blanking Window):
x = 0, 1 or 2. VBWx selects the vertical blanking interval and positions the measurement lines for cut-off and white level control.

The actual lines in the vertical blanking interval after the start of the V-pulses selected as measurement lines for cut-off and white level control are shown in Table 2.

The standards marked with (*) are for progressive line scan at double the line frequency ($2F_L$), i.e. approximately 31 kHz.

NMEN (NTSC - Matrix ENable):
0 = PAL/SECAM matrix
1 = NTSC matrix.

WPEN (White Pulse ENable):
0 = white measuring pulse disabled
1 = white measuring pulse enabled.

BREN (Buffer Register ENable):
0 = new data is executed as soon as it is received
1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval. The I²C-bus transceiver does not accept any new data until this data is transferred into the data registers.

DELOF (DELay OFf) delays the leading edge of clamping pulses:
0 = delay enabled
1 = delay disabled.

SC5 (SandCastle 5 V):
0 = 3-level sandcastle pulse
1 = 2-level (5 V) sandcastle pulse.

Control Register 2

FSON2 - Fast Switch 2 ON

FSDIS2 - Fast Switch 2 DISable

FSON1 - Fast Switch 1 ON

FSDIS1 - Fast Switch 1 DISable

The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:
- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 3).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

FSBL - Full Screen Black Level:
0 = normal mode
1 = full screen black level (cut-off measurement level during full field).

FSWL - Full Screen White Level:
0 = normal mode
1 = full screen white level (white measurement level during full field).

SATOF - SATuration control OFf
0 = saturation control enabled
1 = saturation control disabled, nominal saturation enabled.

Table 2 Cut-off and white level measurement lines

VWB2	VWB1	VWB0	R	G	B	WHITE	STANDARD
0	0	0	19	20	21	22	PAL/SECAM
0	0	1	16	17	18	19	NTSC/PAL M
0	1	0	22	23	24	25	PAL/SECAM (EB)
1	0	0	38, 39	40, 41	42, 43	44, 45	PAL*/SECAM*
1	0	1	32, 33	34, 35	36, 37	38, 39	NTSC*/PAL M*
1	1	0	44. 45	46, 47	48, 49	50, 51	PAL*/SECAM* (EB)

Notes to Table 2
1. The line numbers given are those of the horizontal pulse counts after the start of the vertical component of the sandcastle pulse.
2. * line frequency of approximately 31 kHz.
3. (EB) is extended blanking.

Table 3 Signal input selection by the fast source switches

I²C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 3

Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is "don't care", and ON is the selected signal input.

I²C-bus transmitter

(microcontroller read mode)

As an I²C-bus transmitter, R/WN = 1, the TDA4680 sends a data byte from the status register to the microcontroller. The data byte consists of following bits:

PONRES, CB1, CB0, CG1, CG0, CR1, CR0 and 0, where PONRES is the most significant bit.

PONRES (Power ON RESet) monitors the state of TDA4680's supply voltage:

0 = normal operation

1 = supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage was interrupted).

When PONRES changes state from a logic LOW to a logic HIGH all data and function bits are set to logic LOW.

Table 4 2-bit white level error signals, CX1 and CX0

CX1	CX0	INTERPRETATION
0	0	RAR (Reset-After-Read): no new measurements since last read
1	0	actual (measured) white level *less than* the tolerance range
1	1	actual (measured) white level *within* the tolerance range
0	1	actual (measured) white level *greater than* the tolerance range

2-bit white level error signal

(see Table 4).

CB1, CB0 = 2-bit white level of the *blue* channel.

CG1, CG0 = 2-bit white level of the *green* channel.

CR1, CR0 = 2-bit white level of the *red* channel.

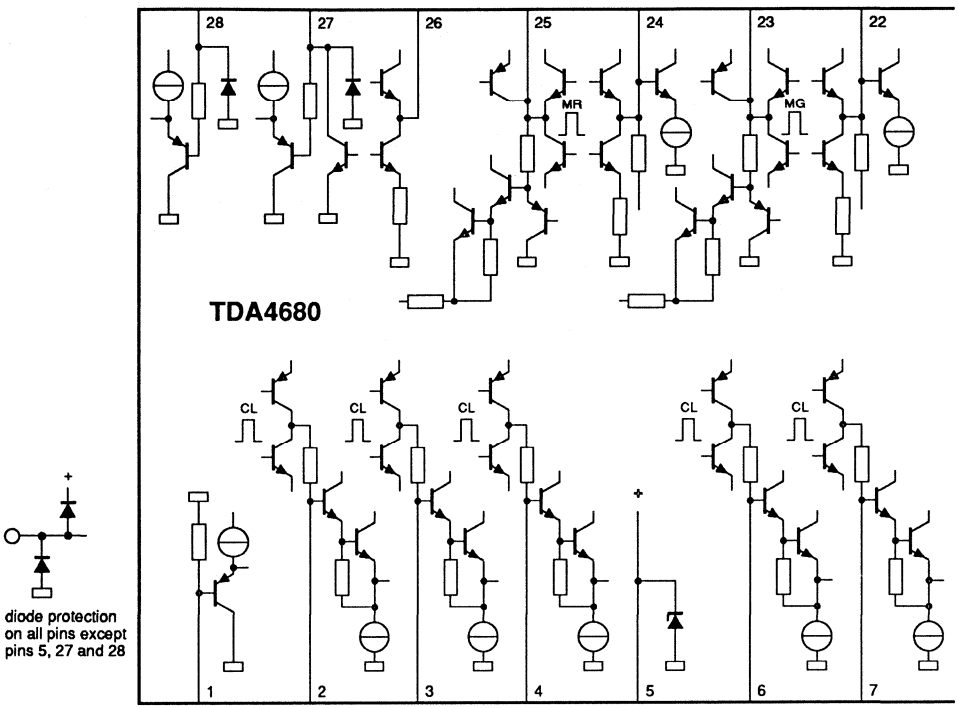


Fig.6(a) Internal circuits (continued in Fig.6b).

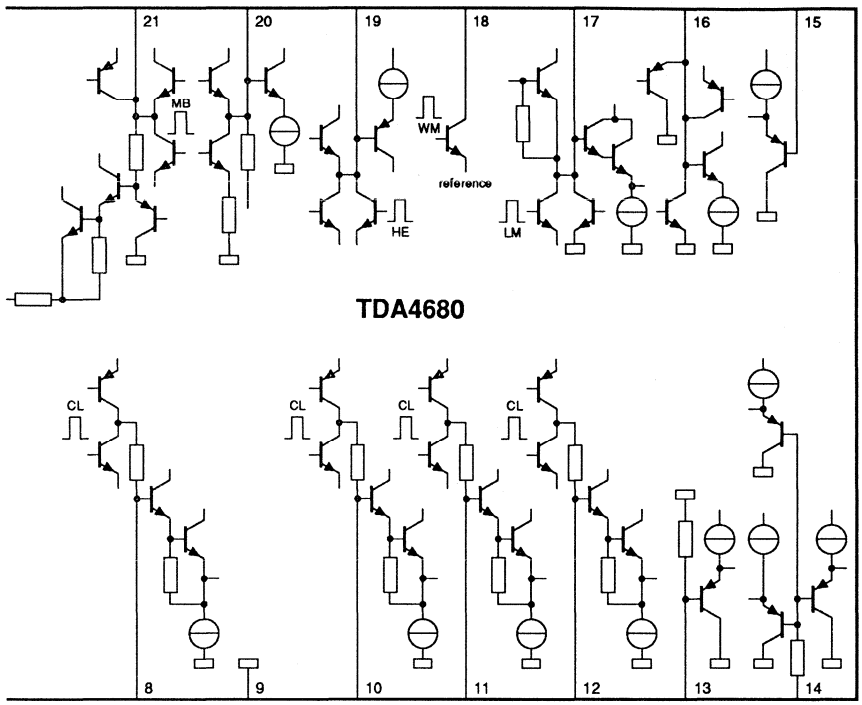


Fig.6(b) Internal circuits (continued from Fig.6a).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	voltage range (pins 1 to 8, 10 to 13, 16, 21, 23, 25, 27 and 28)	–0.1	V_P	V
	voltage range (pins 14, 15, 18 and 19)	–0.7	V_P + 0.7	V
I_{AV}	current range (pins 20, 22 and 24)	4	–10	mA
I_M	peak current range (pins 20, 22 and 24)	4	–20	mA
I_{18}	input current range	0	2	mA
I_{26}	output current range	0.5	–8	mA
T_{stg}	storage temperature range	–20	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	1.2	W

CHARACTERISTICS

All voltages are measured in test circuit of Fig.7 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = 25 °C:
- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	85	110	mA
Colour-difference inputs						
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	note 1 and note 2	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	note 1 and note 2	–	1.05	–	V
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	3.1	–	V
$I_{6,7}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{6,7}$	input resistance		10	–	–	MΩ
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	3.1	–	V
I_8	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	3.1	–	V
$I_{10/11/12}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	3.1	–	V
$I_{2/3/4}$	input current	during line scan	–	–	± 0.1	µA
		at black level clamping	± 100	–	–	µA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (notes 3 and 4)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_1 to select Y, CD or R_1, G_1, B_1 inputs (control bits: see table 3)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	3.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs (control bits: see table 3)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	3.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Saturation adjust acts on internal RGB signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5 % of maximum saturation); data byte $3F_{Hex}$ for maximum saturation; data byte 23_{Hex} for nominal saturation; data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5 % of maximum contrast); data byte $3F_{Hex}$ for maximum contrast; data byte $2C_{Hex}$ for nominal contrast; data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at $2C_{Hex}$	–	3	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5 % of brightness range); data byte $3F_{Hex}$ for maximum brightness; data byte 27_{Hex} for nominal brightness; data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
White potentiometers, under I²C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); see note 5. data byte $3F_{Hex}$ for maximum gain data byte 22_{Hex} for nominal gain data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain: increase of gain	at $3F_{Hex}$	–	60	–	%
	decrease of gain	at 00_{Hex}	–	60	–	%
RGB outputs pins 24, 22 and 20 (positive going output signals); see note 6.						
$V_{o(b-w)}$	nominal output signals (black-to-white value)		–	2	–	V
	maximum output signals (black-to-white value)		3.2	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line	output clamping (BCOF = 1)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	65	110	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 10 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 8 MHz;	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 10 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 10 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 7 and 8						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses		6.3	–	V_P + 0.7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse detector (control bit SC5 = 1) two level; note 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	burst key pulses		4.0	4.5	V_P + 0.7	V
Sandcastle pulse detector						
I_{14}	input current	V_{14} = 0 V	–	–	100	µA
t_d	leading edge delay of the clamping pulse	control bit DELOF = 0	–	1.5	–	µs
		control bit DELOF = 1	–	0	–	µs
t_{BK}	required burst key pulse time	control bit DELOF = 0; normally used with f_L	3	–	–	µs
		control bit DELOF = 1; normally used with $2f_L$	1.5	–	–	µs
n_{pulse}	required horizontal or burst key pulses during vertical blanking interval	e.g. at interlace scan (VWB2 = 0)	4	–	29	
		e.g. at progressive line scan (VWB2 = 1)	8	–	57	
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs under I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	6.5	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic cut-off and white level control (notes 11, 12 and 13) see Fig.9						
V_{19}	external measurement voltage		–	–	V_P –1.4	V
I_{19}	output current		–	–	–140	µA
	input current		150	–	–	µA
	additional input current	during monitor pulse	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I²C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1	–	V_{pdl} –0.7	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	5.0	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	3.0	–	V
data byte 07_{Hex} for red reference level data byte 08_{Hex} for green reference level data byte 09_{Hex} for blue reference level						
ΔV_{19}	difference between V_{MEAS} (cut-off or white level measurement voltage) and V_{REF}	$3F_{Hex}$ (maximum V_{MEAS})	1.5	–	–	V
		20_{Hex} (nominal V_{MEAS})	–	1.0	–	V
		00_{Hex} (minimum V_{MEAS})	–	–	0.5	V
I_{18}	input current	white level measurement	–	–	800	µA
R_{18}	internal resistance	to V_{REF}; $I_{18} \leq 800$ µA	–	100	–	Ω
ΔV_{19}	white level register (measured value within tolerance range)	white level measurement	–	250	–	mV
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	± 0.3	–	mA
	current	outside measurement	–	–	± 0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	± 0.4	–	mA
	current	outside measurement	–	–	± 0.1	µA
V_{17}	voltage for reset to switch-on below		–	< 3.0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Hue control (note 14) under I²C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.0	V
I_{int}	current of the internal current source at pin 26		500	–	–	μA
I²C-bus transceiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	input current LOW		–	–	–10	μA
I_{IH}	input current HIGH		–	–	10	μA
t_d	pulse time LOW		4.7	–	–	μs
	pulse time HIGH		4.0	–	–	μs
t_r	rise time		–	–	1.0	μs
t_f	fall time		–	–	0.3	μs
I²C-bus transceiver data input/output SDA (pin 27)						
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	input current LOW		–	–	–10	μA
I_{IH}	input current HIGH		–	–	10	μA
I_{OL}	output current LOW		3.0	–	–	mA
t_r	rise time		–	–	1.0	μs
t_f	fall time		–	–	0.3	μs
$t_{su;DAT}$	data set-up time		0.25	–	–	μs

Notes to the characteristics

1. The values of the -(B-Y) and -(R-Y) colour-difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation:

$$V_{G-Y} = -0.51\ V_{R-Y} - 0.19\ V_{B-Y}$$

NTSC signals are matrixed by the equations (hue phase shift of –5 degrees):

$$V_{R-Y}^* = 1.57\ V_{R-Y} - 0.41\ V_{B-Y}$$
$$V_{G-Y}^* = -0.43\ V_{R-Y} - 0.11\ V_{B-Y}$$
$$V_{B-Y}^* = V_{B-Y}$$

In the matrix equations:
V_{R-Y} and V_{B-Y} are for conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator.

V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour-difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B-Y)* demodulator axis	0°	0°
(R-Y)* demodulator axis	115°	90°
(R-Y)* amplification factor	1.97	1.14
(B-Y)* amplification factor	2.03	2.03

$$V_{G-Y}^* = -0.27\ V_{R-Y}^* - 0.22\ V_{B-Y}^*.$$

4. The vertical blanking interval is selected via the I²C-bus (see Table 2 and Fig.9). Vertical blanking is determined by the vertical component of the sandcastle pulse; this vertical component has priority when it is longer than the vertical blanking interval of the transmission standard.
5. The white potentiometers affect the amplitudes of the RGB output signals including the white measurement pulses.
6. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
7. Sandcastle pulses are compared with internal threshold voltages independent of V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.0 V for the burst key pulse.

   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
8. A sandcastle pulse with a maximum voltage equal to (V_P + 0.7 V) is obtained by limiting a 12 V sandcastle pulse.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I²C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. The vertical blanking interval is defined by a V pulse which contains 4 (8) or more H pulses; it begins with the start of the V pulse and ends with the end of the white measuring line. If the V pulse is longer than the selected vertical blanking window the blanking period ends with the end of the complete line after the end of the V pulse. The counter cycle time is 31 (63) H pulses if the V pulse contains more than 29 (57) H pulses. With more than 29 (57) H pulses, the black level storage capacitors will be discharged while all signals are blanked. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Fig.8 and Fig.9).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24,22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitor pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 5.0 V, the monitor pulse is switched off and cut-off and white level control are activated (second switch-on delay). As soon as cut-off control stabilize, RGB output blanking is removed.
13. Range of cut-off measurement level at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.

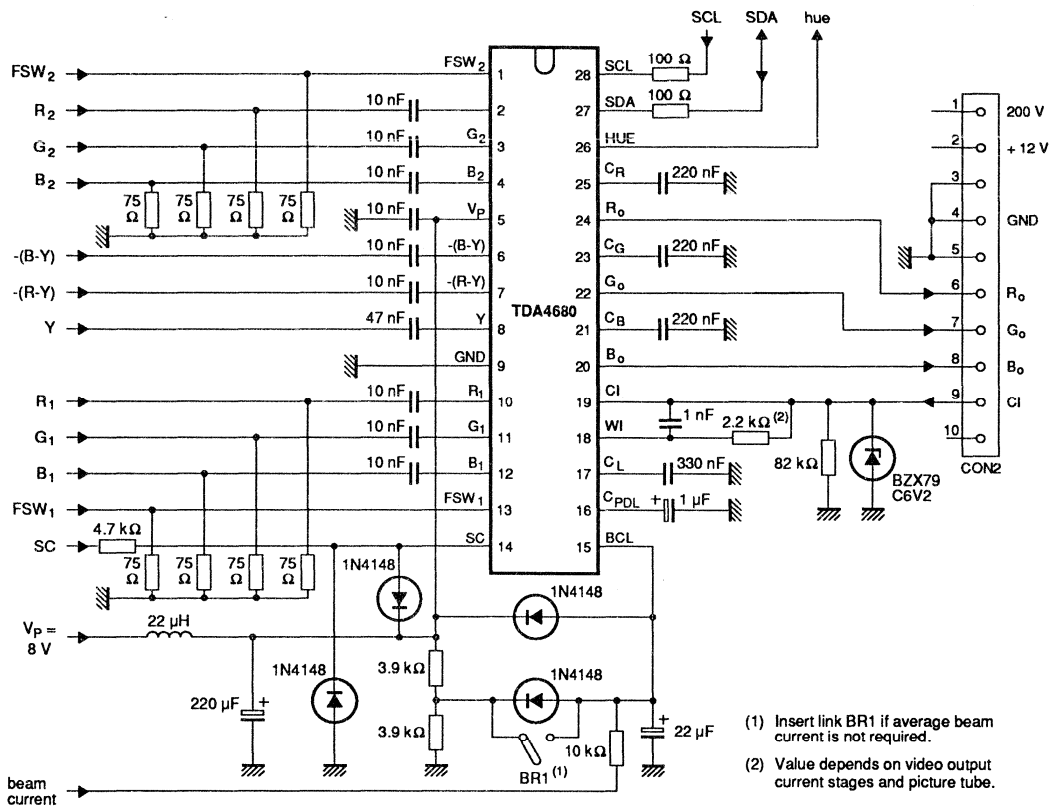


Fig.7 Test and application circuit.

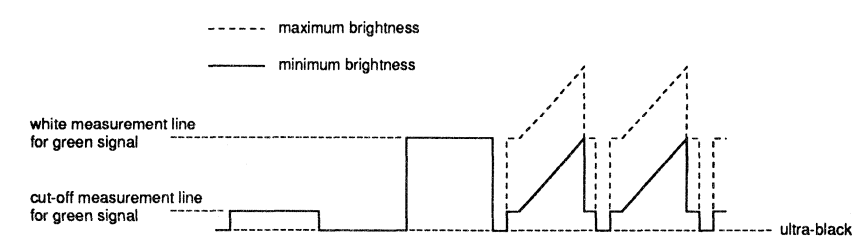


Fig.8 Cut-off and white level measurement pulses.

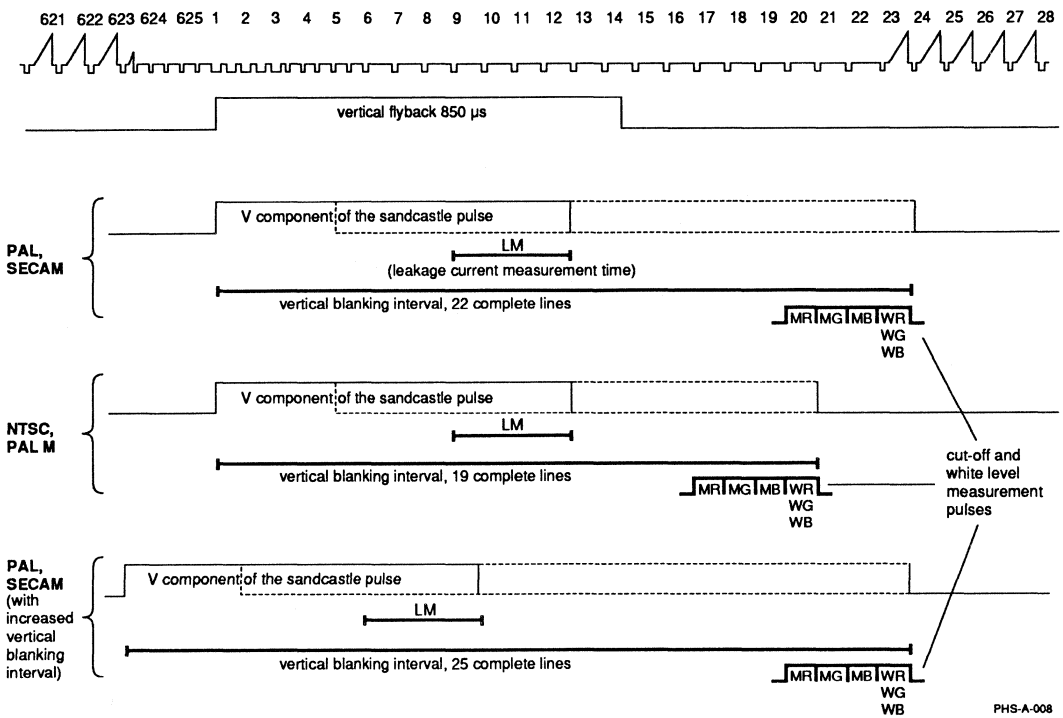


Fig.9 Leakage current, cut-off and white level current measurement timing diagram.

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